

## **TAS5508B Errata**

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### **1 Volume/Mute Operation With Remapped Output Mixer**

#### **1.1 Problem Description**

When the TAS5508B output mixer is used to mix several channels together or to route information from one DAP channel to a different PWM channel, then the TAS5508 can exhibit an unexpected response if one or more individual channels are set to mute. The mute can be performed with an individual channel mute or when the master volume plus individual volume is below  $-109$  dB (0x1FC).

The issue is that the PWM channels corresponding to muted DAP channels are not restarted when coming out of an all-channel shutdown. All-channel shutdowns happen as a response to master mute, mute-pin assertion, I<sup>2</sup>S clock error, or AM mode change. Using the pass-through output mixer configuration avoids this problem.

#### **1.2 System Impact**

If using the remapped output mixer configuration, then after resuming from an all-channel shutdown, the remapped output channels do not stream audio.

#### **1.3 Workaround**

Application software must ensure that combined master volume + channel volume does not go below  $-109$  dB for all channels.

<b>0xD0 Bit 30</b>	<b>Output Mixer Configuration</b>	<b>Mode</b>	<b>PWM (Speaker) Operation</b>
1	Pass-through	8-channel mode or 6-channel mode	Normal operation
0 (default)	Remapped	8-channel mode or 6-channel mode	Constraints are placed in setting the combined volume below $-109$ dB and in using individual channel mute.

When remapping or mixing DAP channels to different PWM output channels (remapped output mixer configuration), consider the following limitations:

- Individual channel mute should not be used.
- The sum of the minimum channel volume and master volume must not be below  $-109$  dB.
- 0xD0 bit 30 = 0

## 2 Headphone Operation With Remapped Output Mixer

### 2.1 Problem Description

When the TAS5508B output mixer is used to mix several channels together or to route information from one DAP channel to a different PWM channel, the TAS5508B headphone select control does not function as expected.

When  $\overline{\text{HP\_SEL}}$  is changed to the LOW state, the TAS5508B stops the audio output of the speakers but does not start outputting audio to the headphones. Similarly, when  $\overline{\text{HP\_SEL}}$  is changed to the HIGH state, the TAS5508B stops the audio output of the headphones but does not start outputting audio to the headphones.

### 2.2 System Impact

If using remapped output mixer configuration in the 6-channel mode, the  $\overline{\text{HP\_SEL}}$  control does not enable audio output from the headphones or loudspeakers.

### 2.3 Workaround

Whenever the state of  $\overline{\text{HP\_SEL}}$  is changed, the system controller must perform the following steps:

1. Wait for a duration that is equal to one volume adjustment time period as set by 0xD0 (default 100 ms).
2. Send a mute command.
3. Wait for a duration that is equal to one volume adjustment time period as set by 0xD0 (default 100 ms).
4. Send an unmute command.

The mute/unmute sequence enables the start of the headphones or speakers.

0xD0 Bit 30	Output Mixer Configuration	Mode	PWM (Speaker) Operation
1	Pass-through	8-channel mode or 6-channel mode	Normal operation
0 (default)	Remapped	8-channel mode	Normal operation
		6-channel mode	Following the assertion or de-assertion of headphone ( $\overline{\text{HP\_SEL}}$ pin), mute must be asserted and de-asserted using the MUTE pin.

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## 3 DRC Control Timing

### 3.1 Problem Description

Write operations to the DRC2 control register (0x97) can be missed if the values of the DRC1 control register (0x96) and DRC2 control register (0x97) are updated in successive I<sup>2</sup>C operations. The issue is that a DRC2 control register update can be missed if it occurs immediately following a DRC1 control register update.

### 3.2 System Impact

The DRC2 control register configuration is changed, but due to an internal timing error in the DRC2 control register, the requested change is not recognized.

### 3.3 Workaround

Provide a 10-ms delay between I<sup>2</sup>C writes to the DRC1 control register (0x96) and DRC2 control register (0x97).

## 4 PSVC Control when Using Subwoofer as Lineout

### 4.1 Problem Description

The problem occurs when the subwoofer is configured as lineout while PSVC is enabled.

One of the PSVC modes is called *subwoofer not part of PSVC calculation*. Normally, this mode is used when the subwoofer is configured as lineout. However, an audible problem occurs during volume changes. In this case, the subwoofer is always used for PSVC calculation even though it is configured not to do so (e.g., as lineout). So, during the volume ramp the transient values are not correct, thereby creating audible artifacts.

### 4.2 System Impact

When the subwoofer is configured as lineout with PSVC enabled, audible artifacts can occur during volume changes.

### 4.3 Workaround

The subwoofer cannot be used as lineout if PSVC is enabled.

## 5 Use of 5-V CMOS I<sup>2</sup>C Drivers

### 5.1 Problem Description

In systems using 5-V CMOS buffers for the I<sup>2</sup>C interface, special pullup resistors are required.

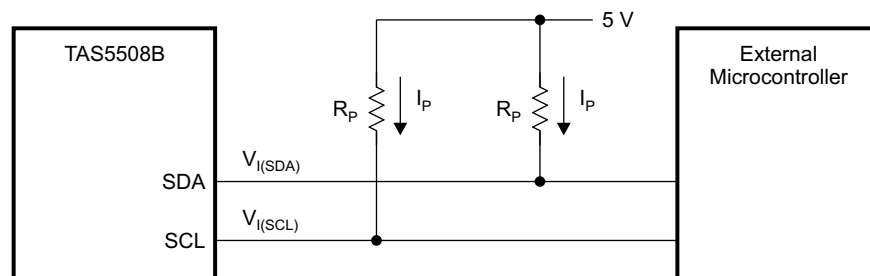
The I<sup>2</sup>C specification requires that  $V_{IH}$  is  $0.7 \times V_{DD} = 3.5$  V when  $V_{DD}$  is 5 V. In some 5-V CMOS systems, the normal value for the I<sup>2</sup>C pullup resistor is 4.7 k $\Omega$ . This could cause the voltage not to rise above 3.47 V, which violates the specification. The root cause has been identified as a TAS5508B 5-V tolerant buffer issue.

### 5.2 System Impact

1. No impact for 3.3-V operation
2. No impact for TTL operation
3. Impact only for 5-V CMOS operation where  $V_{IH}$  could be lower than the specification of 3.5 V.

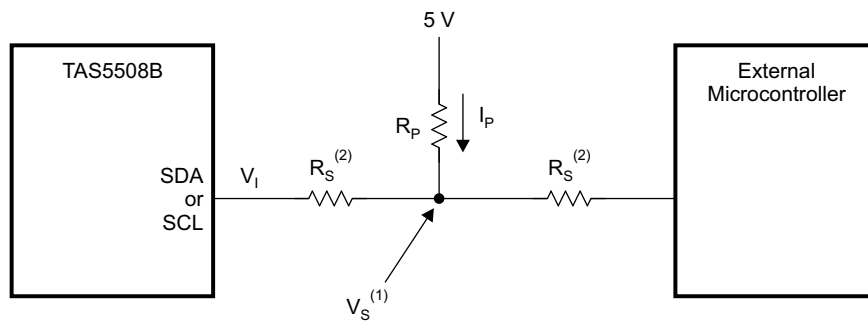
### 5.3 Workaround

It is recommended that the I<sup>2</sup>C pullup resistors,  $R_P$ , be 3.3 k $\Omega$  (see [Figure 1](#)). If a series resistor is in the circuit (see [Figure 2](#)), then the series resistors,  $R_S$ , should be less than or equal to 300  $\Omega$ .



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Figure 1. I<sup>2</sup>C Pullup Circuit (With No Series Resistor)



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- (1)  $V_S = 5 \times R_S / (R_S + R_P)$ . When driven low,  $V_S \ll V_{IL}$  requirements.
- (2)  $R_S \leq 300 \Omega$

**Figure 2. I<sup>2</sup>C Pullup Circuit (With Series Resistor)**

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