

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

T B 6 5 0 4 F

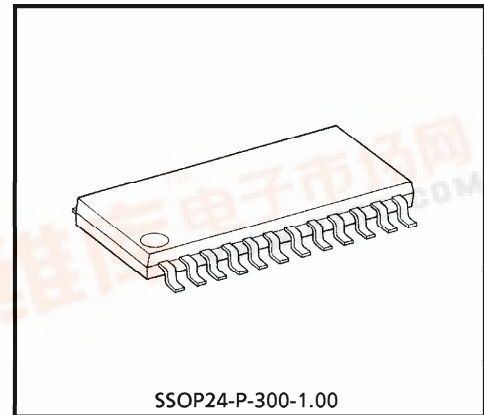
PWM CHOPPER TYPE BIPOLAR STEPPING MOTOR DRIVER.

The TB6504F is PWM chopper type sinusoidal micro step bipolar stepping motor driver.

Sinusoidal micro step operation is accomplished only a clock signal inputting by means of built-in hard ware.

FEATURES

- 1 chip bipolar sinusoidal micro step stepping motor driver.
- Output Current up to 150mA
- PWM chopper type.
- Structured by high voltage Bi-CMOS process technology.
- Forward and reverse rotation are available.
- 2, 1-2, W1-2, 2W1-2 phase 1 or 2 clock drives are selectable.
- Package : SSOP24-P-300-1.00
- Input Pull-Up Resistor equipped with RESET and ENABLE Terminal : R = 200kΩ (Typ.)
- Output Monitor available with \overline{MO} . $I_O(\overline{MO}) = \pm 2\text{mA MAX.}$
- Reset and Enable are available with $\overline{\text{RESET}}$ and $\overline{\text{ENABLE}}$.



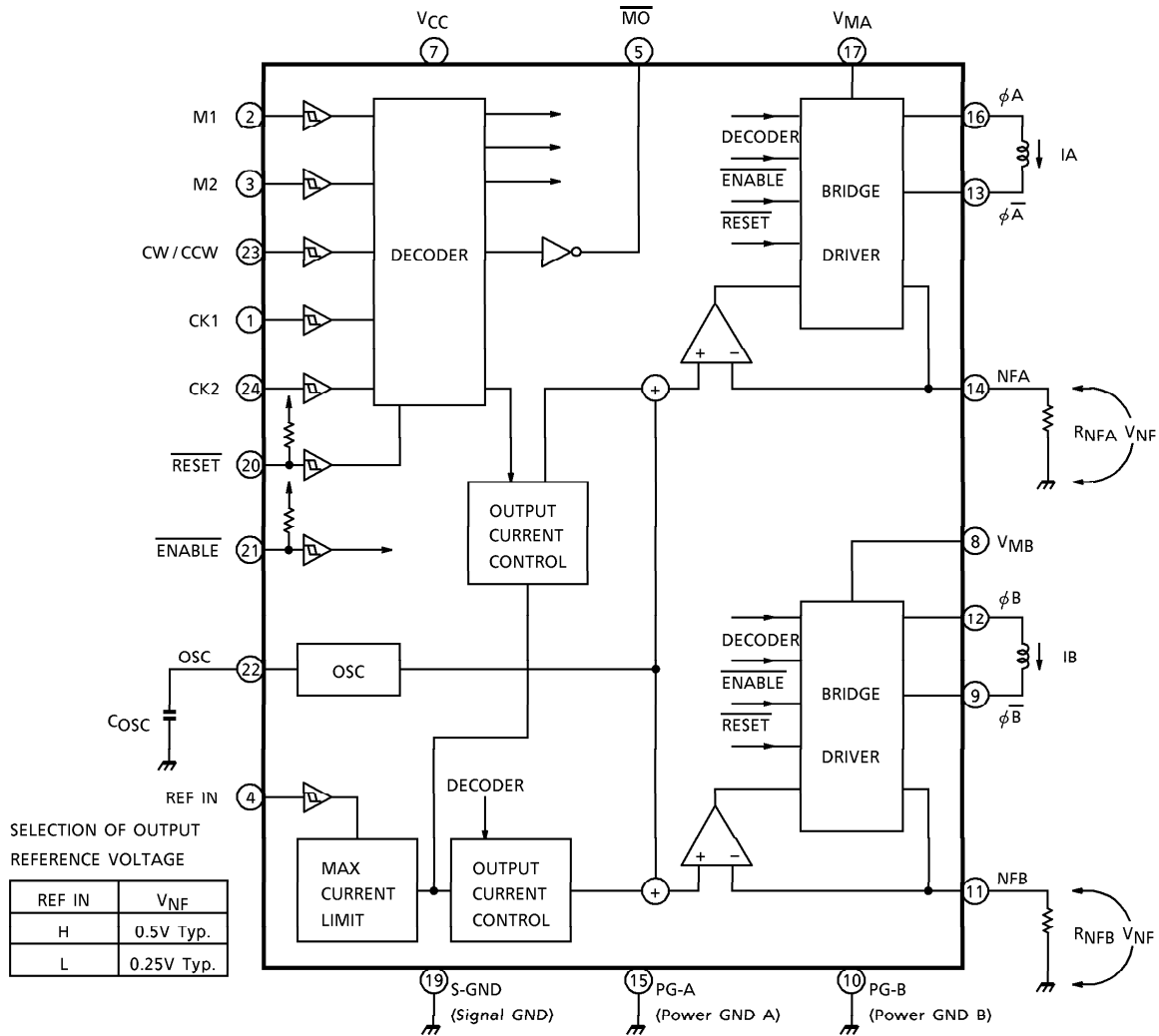
Weight : 0.32g (Typ.)

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BLOCK DIAGRAM

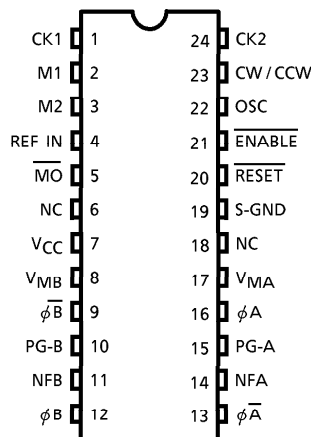


Pull-up Resistance pin⑳, ㉑ : 200kΩ (Typ.)
 pin㉒, ㉓ : Non Connection

PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION	
1	CK1	Clock signal input terminal.	TRUTH TABLE A
2	M1	Excitation control input.	TRUTH TABLE B
3	M2	Excitation control input.	
4	REF IN	V_{NF} control input. High Level ; $V_{NF} = 0.5V$, Low Level ; $V_{NF} = 0.25V$	
5	\overline{MO}	Monitor output.	
6	NC	No connection.	
7	V_{CC}	Supply voltage terminal for control circuit.	
8	V_{MB}	Supply voltage terminal for Motor Drive.	
9	ϕB	Output B	
10	PG-B	Power GND	
11	NFB	B-ch current detection terminal.	
12	ϕB	Output B	
13	$\phi \overline{A}$	Output A	
14	NFA	A-ch current detection terminal.	
15	PG-A	Power GND	
16	ϕA	Output A.	
17	V_{MA}	Supply voltage terminal for Motor Drive.	
18	NC	No connection.	
19	S-GND	Signal GND.	
20	\overline{RESET}	Reset signal input terminal.	TRUTH TABLE A
21	\overline{ENABLE}	Enable signal input terminal.	
22	OSC	Sawtooth oscillation terminal.	
23	CW/CCW	Forward rotation / Reverse rotation input terminal.	TRUTH TABLE A
24	CK2	Clock signal input terminal.	

PIN CONNECTION (Top view)



(Note) NC : No connection

TRUTH TABLE A

INPUT					MODE
CK1	CK2	CW/CCW	RESET	ENABLE	
	H	L	H	L	CW
	L	L	H	L	INHIBIT
H		L	H	L	CCW
L		L	H	L	INHIBIT
	H	H	H	L	CCW
	L	H	H	L	INHIBIT
H		H	H	L	CW
L		H	H	L	INHIBIT
X	X	X	L	L	INITIAL
X	X	X	X	H	Z

Z : High impedance
X : Don't Care

TRUTH TABLE B

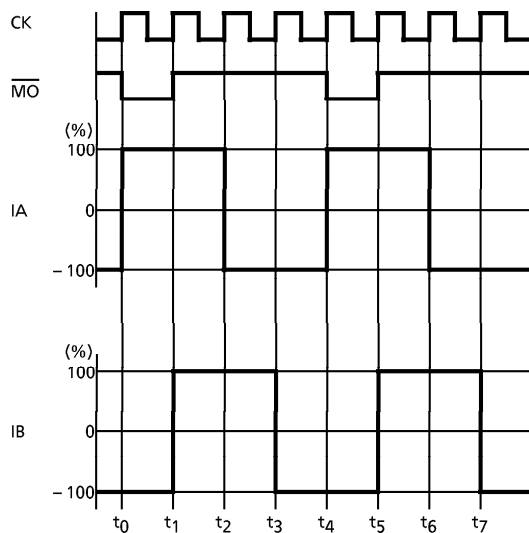
INPUT		MODE (EXCITATION)
M1	M2	
L	L	2 Phase
H	L	1-2 Phase
L	H	W1-2 Phase
H	H	2W1-2 Phase

INITIAL MODE

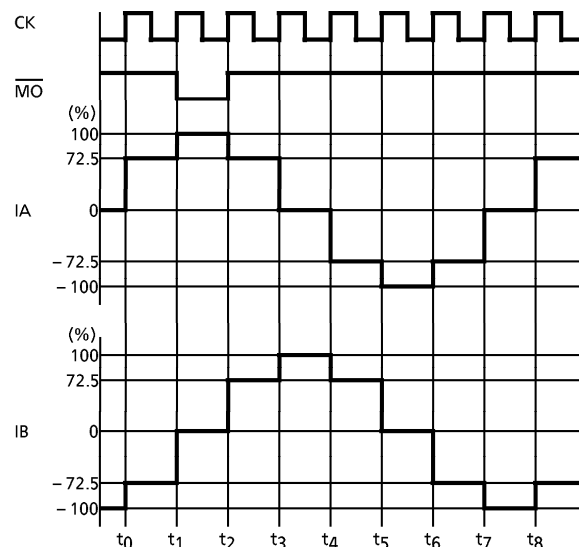
MODE	I _{OUT} (A)	I _{OUT} (B)
2 Phase	100%	- 100%
1-2 Phase	100%	0%
W1-2 Phase	100%	0%
2W1-2 Phase	100%	0%

EXCITATION

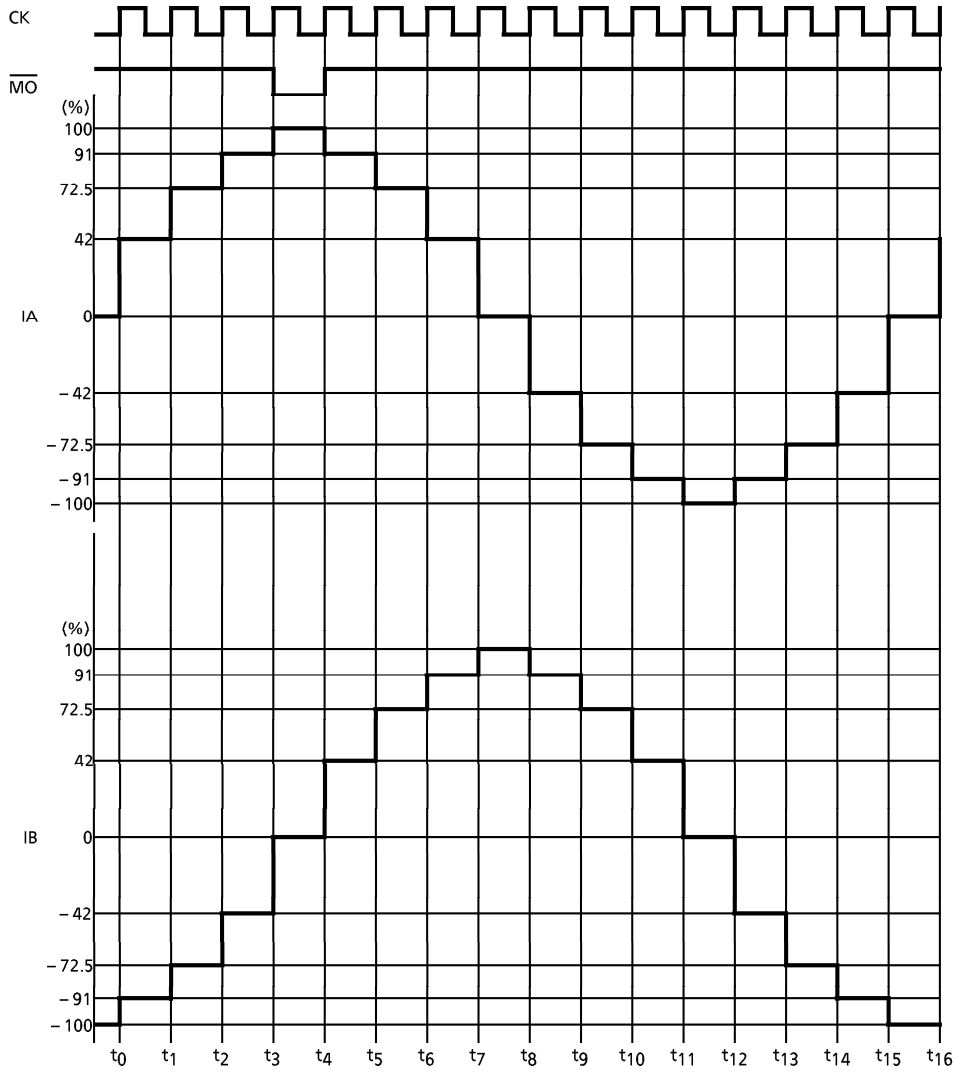
2 Phase excitation (M1 : L, M2 : L, CW MODE)



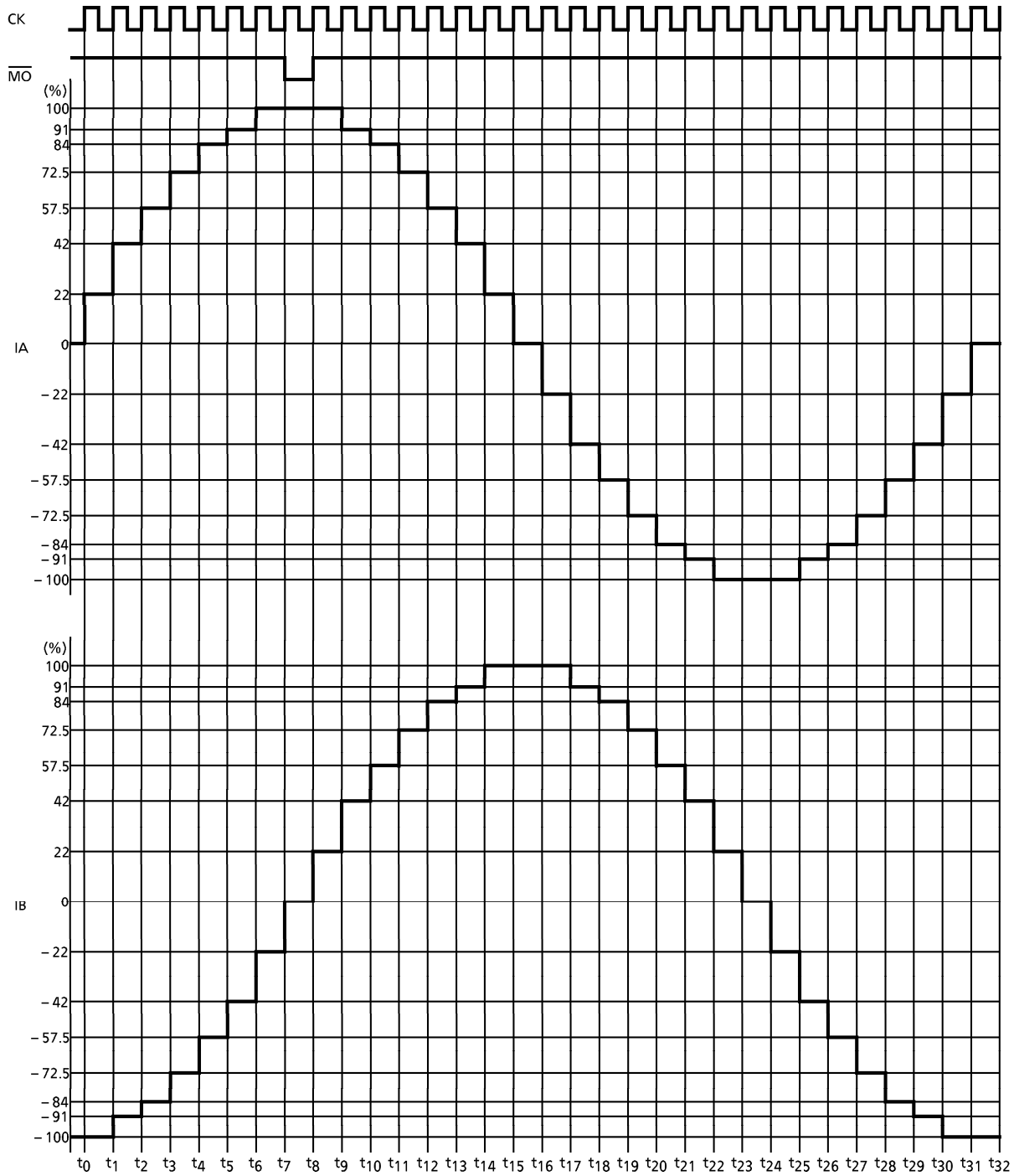
1-2 Phase excitation (M1 : H, M2 : L, CW MODE)



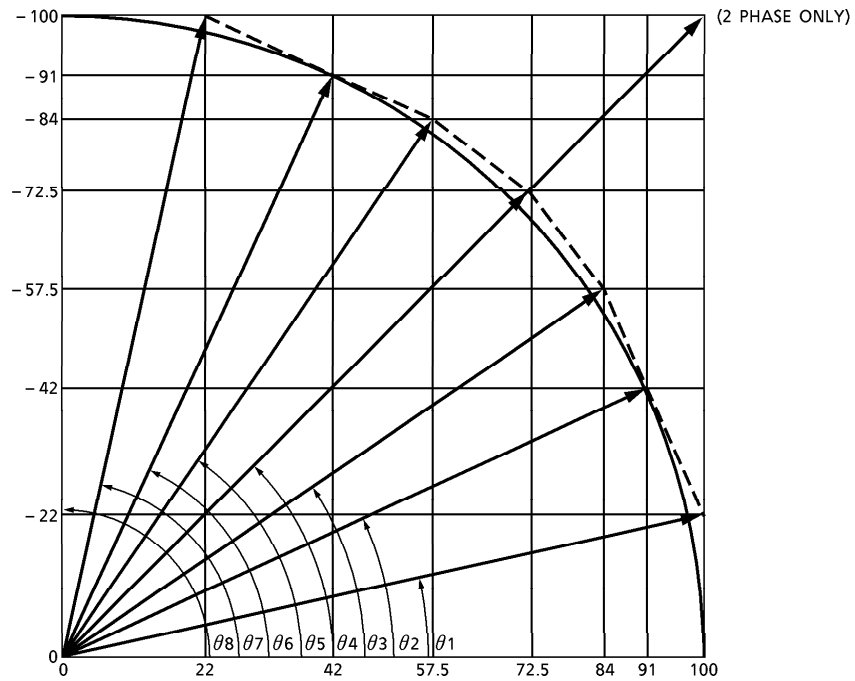
W1-2 Phase excitation (M1 : L, M2 : H, CW MODE)



2W1-2 Phase excitation (M1 : H, M2 : H, CW MODE)

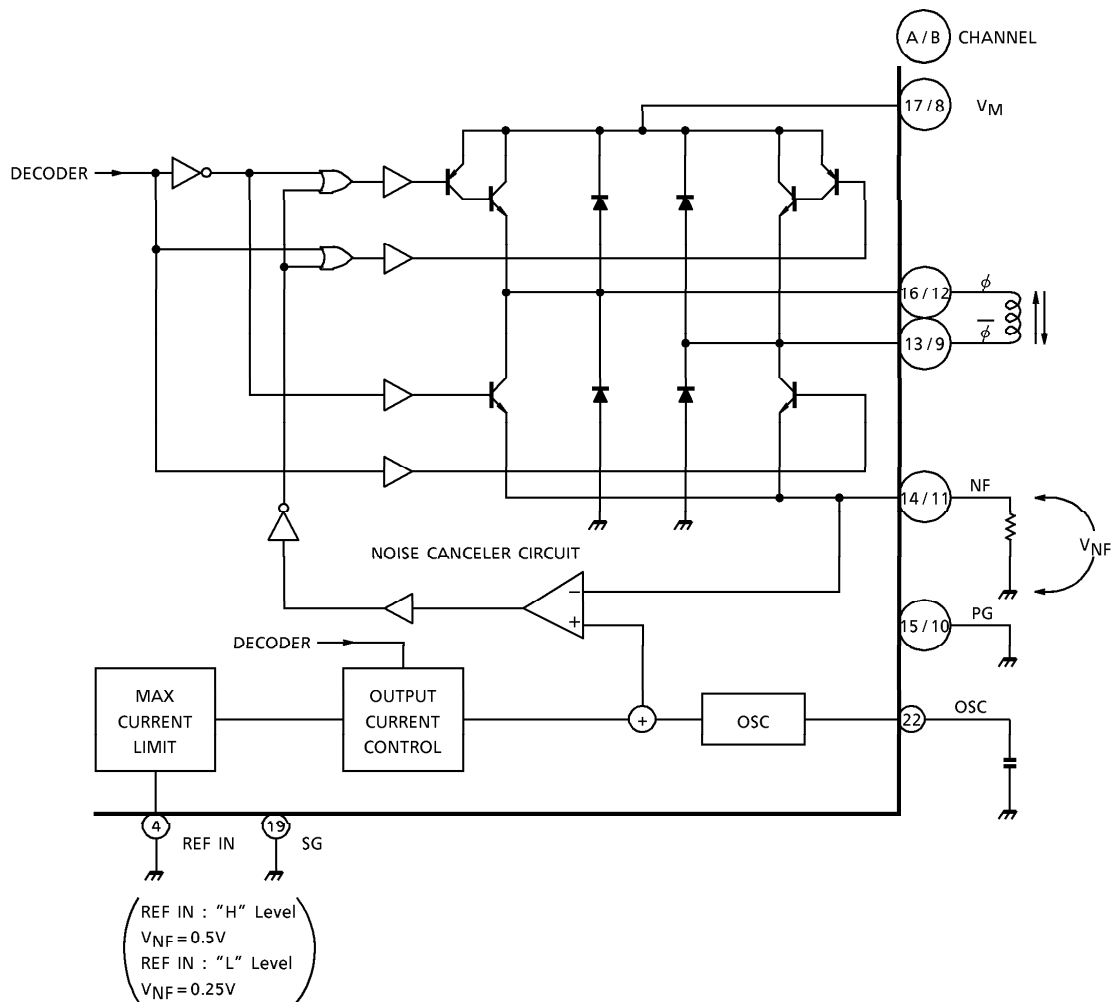


OUTPUT CURRENT VECTOR ORBIT (Normalize to 90° for each one step)



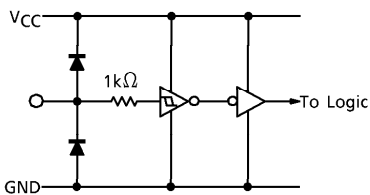
θ	ROTATION ANGLE		VECTOR LENGTH		
	IDEAL	TB6504F	IDEAL	TB6504F	
θ_0	0°	0°	100	100.00	—
θ_1	11.25°	12.41°	100	102.39	—
θ_2	22.5°	27.78°	100	100.22	—
θ_3	33.75°	34.39°	100	101.80	—
θ_4	45°	45°	100	102.53	141.42
θ_5	56.25°	55.61°	100	101.81	—
θ_6	67.5°	65.22°	100	100.22	—
θ_7	78.75°	77.59°	100	102.39	—
θ_8	90°	90°	100	100.00	—
1-2, W1-2, 2W1-2 Phase					2 Phase

OUTPUT CIRCUIT

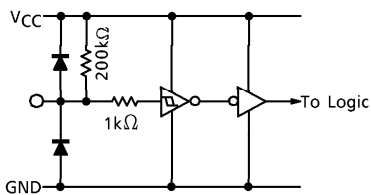


INPUT CIRCUIT

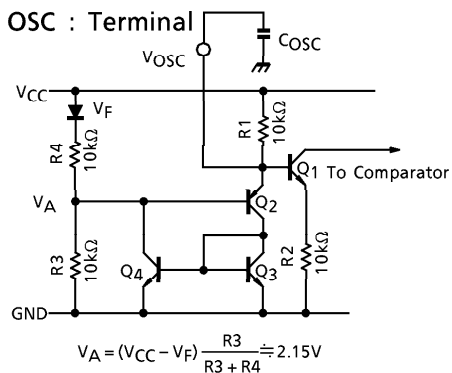
CK1, CK2, CW/CCW, M1,
M2, REF IN : Terminals



RESET, ENABLE : Terminal



OSC : Terminal



OSC FREQUENCY CALCULATION

Sawtooth OSC circuit consists of Q₁ through Q₄ and R1 through R4.

Q₂ is turned "off" when V_{OSC} is less than the voltage of 2.5V + V_{BE} Q₂ approximately equal to 2.85V.

V_{OSC} is increased by C_{OSC} charging through R1.

Q₃ and Q₄ are turned "on" when V_{OSC} becomes 2.85V (Higher level.)

Lower level of V[Ⓜ] pin is equal to V_{BE} Q₂ + V_{SAT} Q₄ approximately equal to 1.4V.

V_{OSC} is calculated by following equation.

$$V_{OSC} = 5 \cdot [1 - \exp(-\frac{t}{C_{OSC} \cdot R1})] \dots\dots\dots \textcircled{1}$$

Assuming that V_{OSC} = 1.4V (t = t₁) and = 2.85V (t = t₂)

C_{OSC} is external capacitance connected to pin[Ⓜ] and R1 is on-chip 10kΩ resistor.

Therefore, OSC frequency is calculated as follows.

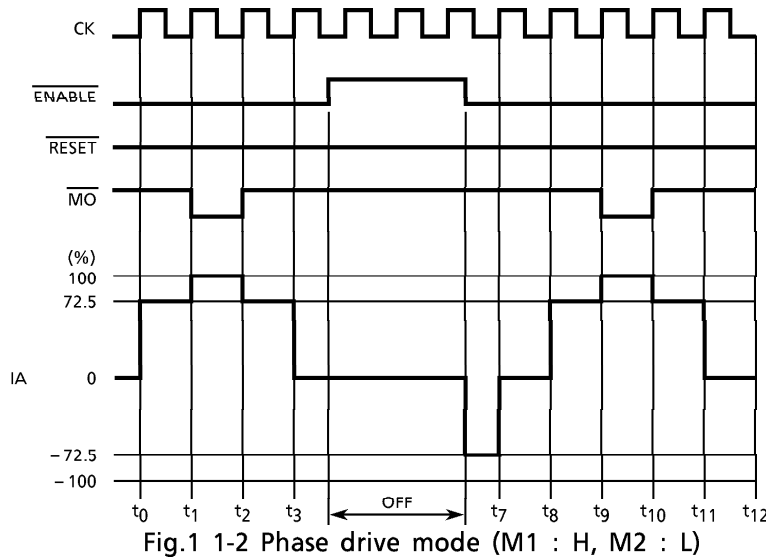
$$t_1 = -C_{OSC} \cdot R1 \cdot \ln(1 - \frac{1.4}{5}) \dots\dots\dots \textcircled{2}$$

$$t_2 = -C_{OSC} \cdot R1 \cdot \ln(1 - \frac{2.85}{5}) \dots\dots\dots \textcircled{3}$$

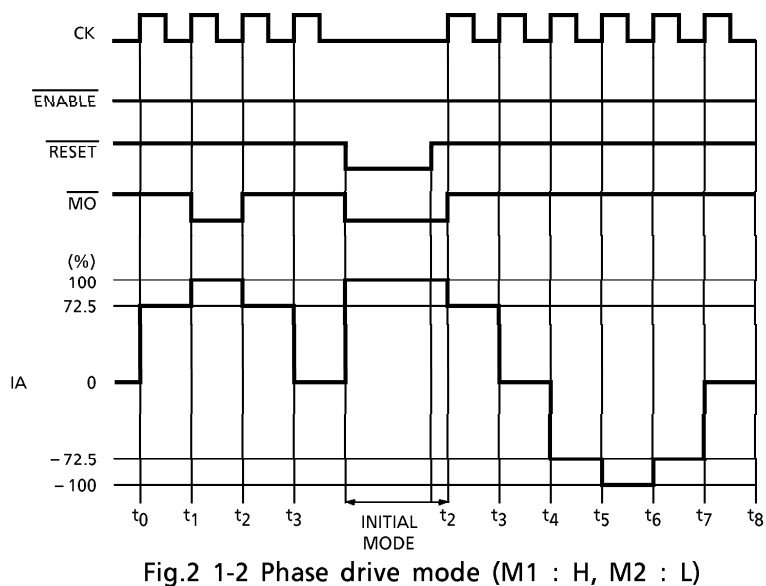
$$f_{OSC} = \frac{1}{t_2 - t_1} = \frac{1}{C_{OSC} (R1 \cdot \ln(1 - \frac{1.4}{5}) - R1 \cdot \ln(1 - \frac{2.85}{5}))}$$

$$= \frac{1}{5.15 \cdot C_{OSC}} \text{ (kHz) } (C_{OSC} : \mu\text{F})$$

ENABLE AND RESET FUNCTION AND MO SIGNAL



ENABLE Signal disables only Output Signal.
 Internal logic functions are proceeded by CK signal without regard to ENABLE signal.
 Therefore, Output Current is initiated from the proceeded timing point of internal logic circuit after release of disable mode.
 Fig.1 shows the ENABLE functions, when the system is selected in 1-2 Phase drive mode.
 As RESET is low, the decoder is initialized and MO is low.
 After RESET is high, the motion is resumed from next clock as shown in Fig.2.



MO (Monitor Output) Signals is used as rotation and initial signal for stable rotation checking.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	5.5	V
	V _{M (opr)}	V _{CC} - 0.3~10	
	V _{M (MAX)}	18	
Output Current	I _{O (MAX)}	150	mA
	I _{O (MO)}	± 2	
Input Voltage	V _{IN}	~V _{CC}	V
Power Dissipation	P _D	0.59 (Note 1)	W
		0.83 (Note 2)	
Operating Temperature	T _{opr}	- 10~70	°C
Storage Temperature	T _{stg}	- 55~150	°C
Feed Back Voltage	V _I	1.0	V

(Note 1) No heat sink

(Note 2) With heat sink (50×50×1.6mm Cu 10%)

RECOMMENDED OPERATING CONDITIONS (Ta = - 10~70°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{CC (opr)}	—	—	4.5	5.0	5.5	V
Output Voltage	V _{M (opr)}	—	—	5.5	—	8.0	V
Output Current	I _{OUT}	—	—	—	—	120	mA
Input Voltage	V _{IN}	—	—	—	—	V _{CC}	V
Clock Frequency	f _{CLOCK}	—	—	—	—	5	kHz
OSC Frequency	f _{OSC}	—	—	15	—	80	kHz

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, VCC = 5V, VM = 8V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	High	V _{IN} (H)	1	M1, M2, CW / CCW, REF IN ENABLE, CK1, CK2, RESET	3.5	—	V _{CC} + 0.4	V
	Low	V _{IN} (L)			GND - 0.4	—	1.5	
Input Hysteresis Voltage		V _H			—	600	—	mV
Input Current		I _{IN-1} (H)	1	M1, M2, REF IN, V _{IN} = 5.0V	—	—	100	nA
		I _{IN-1} (L)		RESET, V _{IN} = 0V, ENABLE INTERNAL PULL-UP RESISTOR	5	25	50	μA
		I _{IN-2} (L)		SOURCE TYPE, V _{IN} = 0V	—	—	100	nA
Quiescent Current V _{CC} Terminal	I _{CC1}		2	Output Open RESET : H ENABLE : L (2, 1-2 Phase excitation)	—	10	18	mA
	I _{CC2}			Output Open (W1-2, 2W1-2 Phase excitation) RESET : H ENABLE : L	—	10	18	
	I _{CC3}			RESET : L, ENABLE : H	—	5	—	
	I _{CC4}			RESET : H, ENABLE : H	—	5	—	
Comparator Reference Voltage	High	V _{NF} (H)	3	REF IN H R _{NF} = 5Ω, C _{OSC} = 0.0033μF	0.45	0.5	0.55	V
	Low	V _{NF} (L)		REF IN L R _{NF} = 2.5Ω, C _{OSC} = 0.0033μF	0.22	0.25	0.28	
Output Differential		ΔV _O	—	B / A, C _{OSC} = 0.0033μF R _{NF} = 2.5Ω, REF IN = L	- 10	—	10	%
V _{NP} (H) - V _{NF} (L)		ΔV _{NF}	—	V _{NF} (L) / V _{NF} (H) C _{OSC} = 0.0033μF	43	50	57	%
Maximum OSC Frequency		f _{OSC} (MAX.)	—	—	100	—	—	kHz
Minimum OSC Frequency		f _{OSC} (MIN.)	—	—	—	—	10	kHz
OSC Frequency		f _{OSC}	—	C _{OSC} = 0.0033μF	31	44	70	kHz
Output Voltage		V _{OH} (MO)	—	I _{OH} = - 40μA	4.5	4.9	V _{CC}	V
		V _{OL} (MO)	—	I _{OL} = 40μA	GND	0.1	0.5	

OUTPUT BLOCK

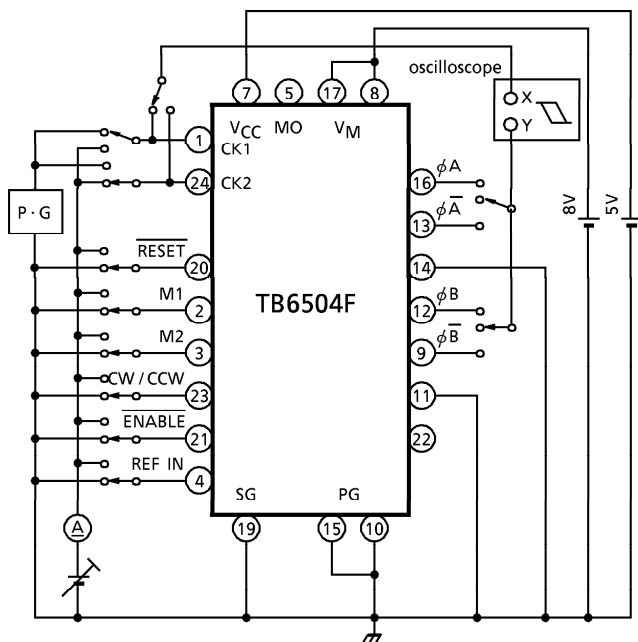
CHARACTERISTIC				SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Saturation Voltage	Upper Side		$V_{SAT\ U1}$	4	$I_{OUT} = 0.12A$	—	0.90	1.25	V	
	Lower Side		$V_{SAT\ L1}$			—	0.22	0.37		
	Upper Side		$V_{SAT\ U2}$		$I_{OUT} = 0.06A$	—	0.83	—		
	Lower Side		$V_{SAT\ L2}$			—	0.12	—		
Diode Forward Voltage	Upper Side		$V_F\ U1$	5	$I_{OUT} = 0.12A$	—	1.18	1.8	V	
	Lower Side		$V_F\ L1$			—	0.92	1.6		
Output Dark Current (A + B Channels)				I_{M1}	2	ENABLE : "H" Level RESET : "L" Level Output Open	—	—	50	μA
				I_{M2}		ENABLE : "L" Level RESET : "H" Level Output Open, 2 Phase excitation mode	—	8	28	mA
NF Terminal Current				I_{NF}	—	ENABLE : "L" Level RESET : "H" Level Output Open	1	2.5	7	
A-B Chopping Current (Note)	2W1-2 ϕ	W1-2 ϕ	1-2 ϕ	VECTOR	3	$\theta = 0$ $\theta = 1/8$ $\theta = 2/8$ $\theta = 3/8$ $\theta = 4/8$ $\theta = 5/8$ $\theta = 6/8$ $\theta = 7/8$ REF IN : L RNF = 2.5 Ω COSC = 0.0033 μF L = 10mH / R = 0.5 Ω	—	100	—	%
	2W1-2 ϕ	—	—				—	100	—	
	2W1-2 ϕ	W1-2 ϕ	—				86	91	96	
	2W1-2 ϕ	—	—				79	84	89	
	2W1-2 ϕ	W1-2 ϕ	1-2 ϕ				67.5	72.5	77.5	
	2W1-2 ϕ	—	—				52.5	57.5	62.5	
	2W1-2 ϕ	W1-2 ϕ	—				37	42	47	
	2W1-2 ϕ	—	—				17	22	27	
	2 Phase Excitation Mode VECTOR						—	—	—	

(Note) Maximum current ($\theta = 0$) : 100%
 2W1-2 ϕ : 2W1, 2 phase excitation mode
 W1-2 ϕ : W1, 2 phase excitation mode
 1-2 ϕ : 1, 2 phase excitation mode

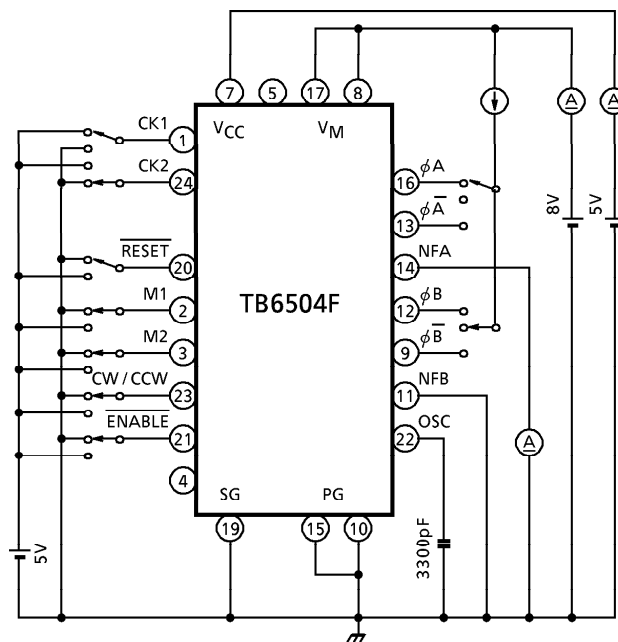
CHARACTERISTIC				SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT			
A-B Chopping Current (Note)	2W1-2 ϕ	W1-2 ϕ	1-2 ϕ	VECTOR	3	$\theta = 0$	REF IN : L RNF = 3.3 Ω COSC = 0.0033 μ F L = 20mH / R = 60 Ω	—	100	—	%		
	2W1-2 ϕ	—	—			$\theta = 1/8$		—	100	—			
	2W1-2 ϕ	W1-2 ϕ	—			$\theta = 2/8$		—	91.2	—			
	2W1-2 ϕ	—	—			$\theta = 3/8$		—	84.2	—			
	2W1-2 ϕ	W1-2 ϕ	1-2 ϕ			$\theta = 4/8$		—	73.6	—			
	2W1-2 ϕ	—	—			$\theta = 5/8$		—	59	—			
	2W1-2 ϕ	W1-2 ϕ	—			$\theta = 6/8$		—	44.6	—			
	2W1-2 ϕ	—	—			$\theta = 7/8$		—	25.6	—			
	2 Phase Excitation Mode VECTOR								—	—		100	—
Feed Back Voltage Step				ΔV_{NF}	—	$\Delta\theta = 0/8 - 1/8$	REF IN : L RNF = 2.5 Ω COSC = 0.0033 μ F	—	0	—	mV		
						$\Delta\theta = 1/8 - 2/8$		10	22.5	35			
						$\Delta\theta = 2/8 - 3/8$		5	17.5	30			
						$\Delta\theta = 3/8 - 4/8$		16.25	28.75	41.25			
						$\Delta\theta = 4/8 - 5/8$		25	37.5	50			
						$\Delta\theta = 5/8 - 6/8$		26.25	38.75	51.25			
						$\Delta\theta = 6/8 - 7/8$		37.5	50	62.5			
Output Tr Switching Characteristics				t_r	7	R _L = 2 Ω , V _{NF} = 0V, C _L = 15pF	—	0.3	—	μ S			
				t_f			—	2.2	—				
				t_{pLH}			CK~Output				—	1.5	—
				t_{pHL}			OSC~Output				—	2.7	—
				t_{pLH}			OSC~Output				—	5.4	—
				t_{pHL}			OSC~Output				—	6.3	—
				t_{pLH}			RESET~Output				—	2.0	—
				t_{pHL}			RESET~Output				—	2.5	—
				t_{pLH}			ENABLE~Output				—	5.0	—
t_{pHL}	ENABLE~Output			—	6.0	—							
Output Leakage Current	Upper Side	I _{OH}	6	V _M = 18V	—	—	50	μ A					
	Lower Side	I _{OL}			—	—	50						

(Note) Maximum current ($\theta = 0$) : 100%
 2W1-2 ϕ : 2W1, 2 phase excitation mode
 W1-2 ϕ : W1, 2 phase excitation mode
 1-2 ϕ : 1, 2 phase excitation mode

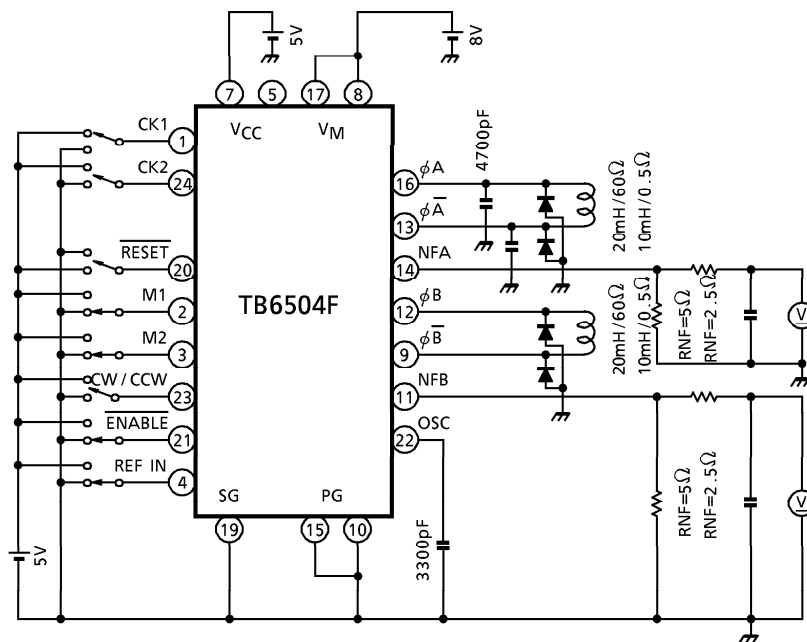
TEST CIRCUIT 1. : V_{IN} (H), (L), I_{IN} (H), (L)



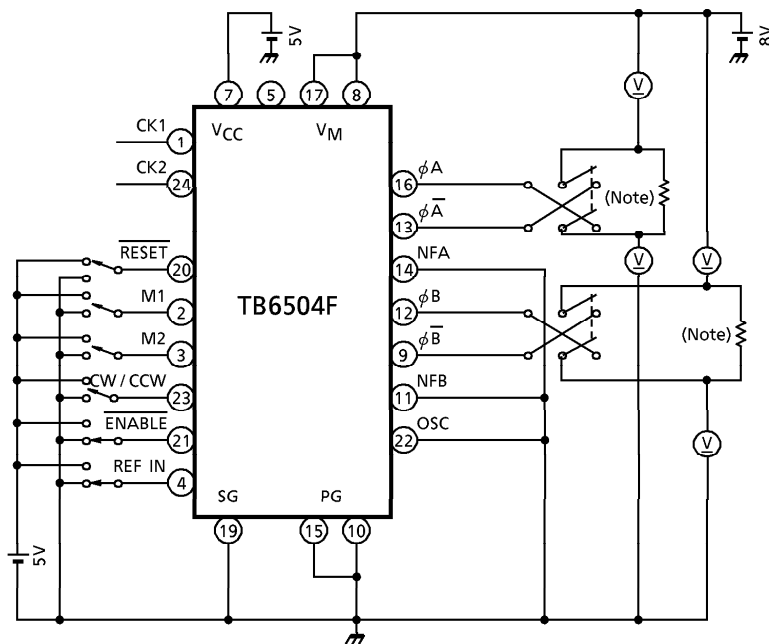
TEST CIRCUIT 2. : I_{CC} , I_M , I_{NF}



TEST CIRCUIT 3. : V_{NF} (H), (L)

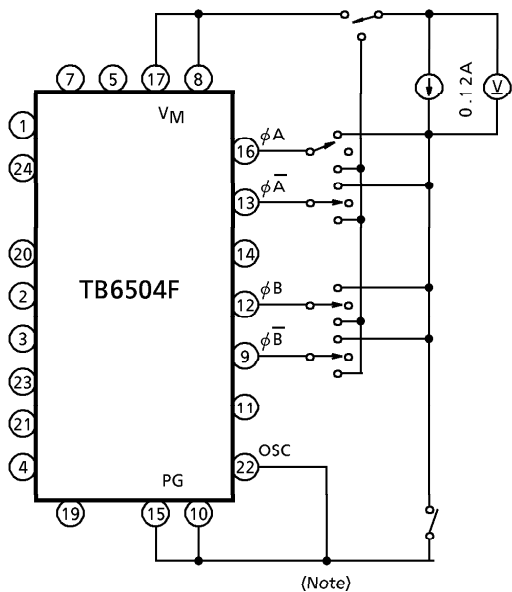


TEST CIRCUIT 4. : $V_{CE(SAT)}$ Upper, Lower

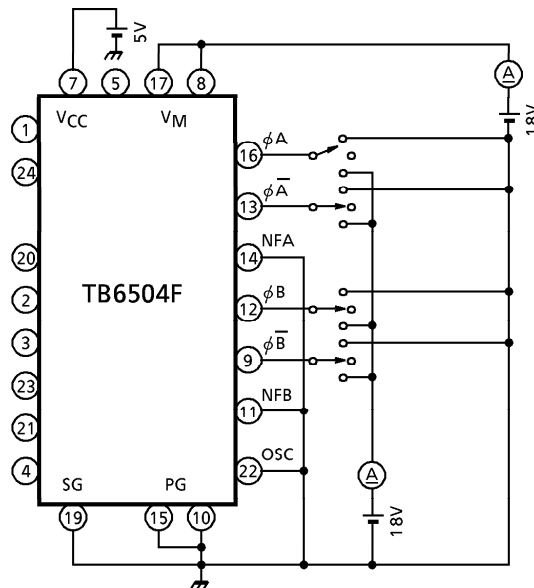


(Note) Calibrate Output Current becomes 0.06A (or 0.12A) with this resistor.

TEST CIRCUIT 5. : V_{F-U} , V_{F-L}

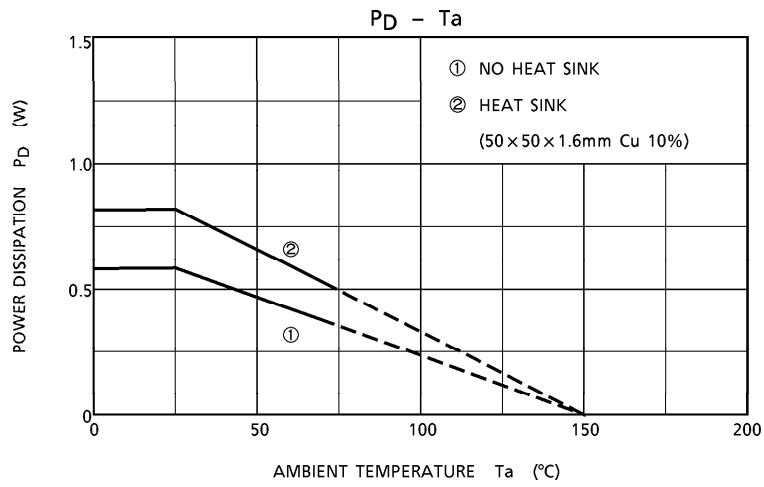
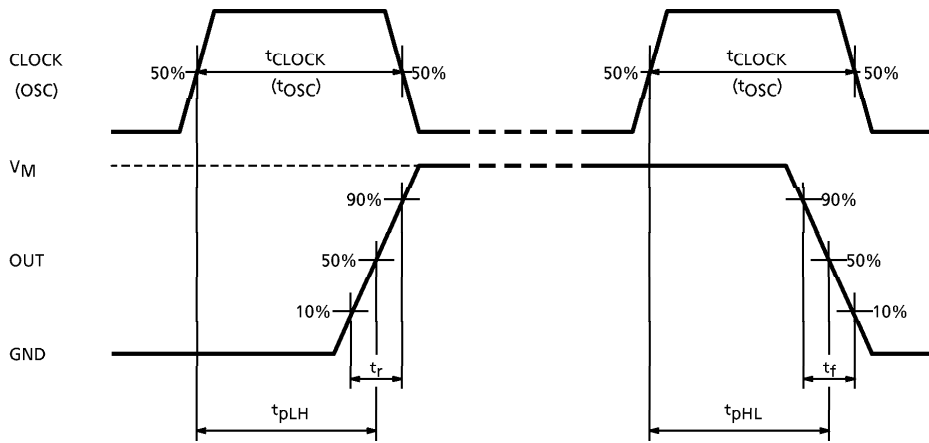


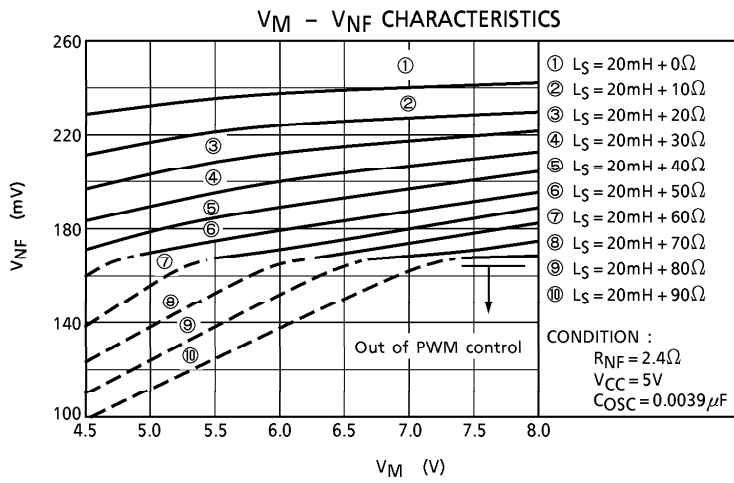
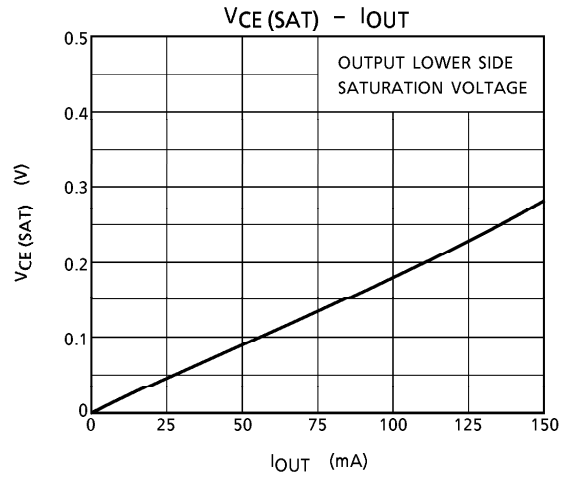
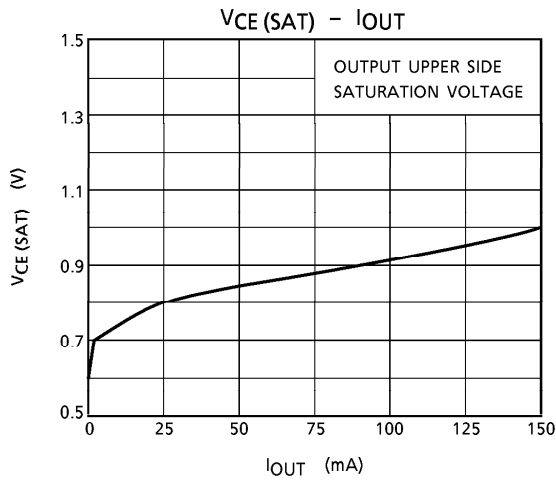
TEST CIRCUIT 6. : I_{OH} , I_{OL}



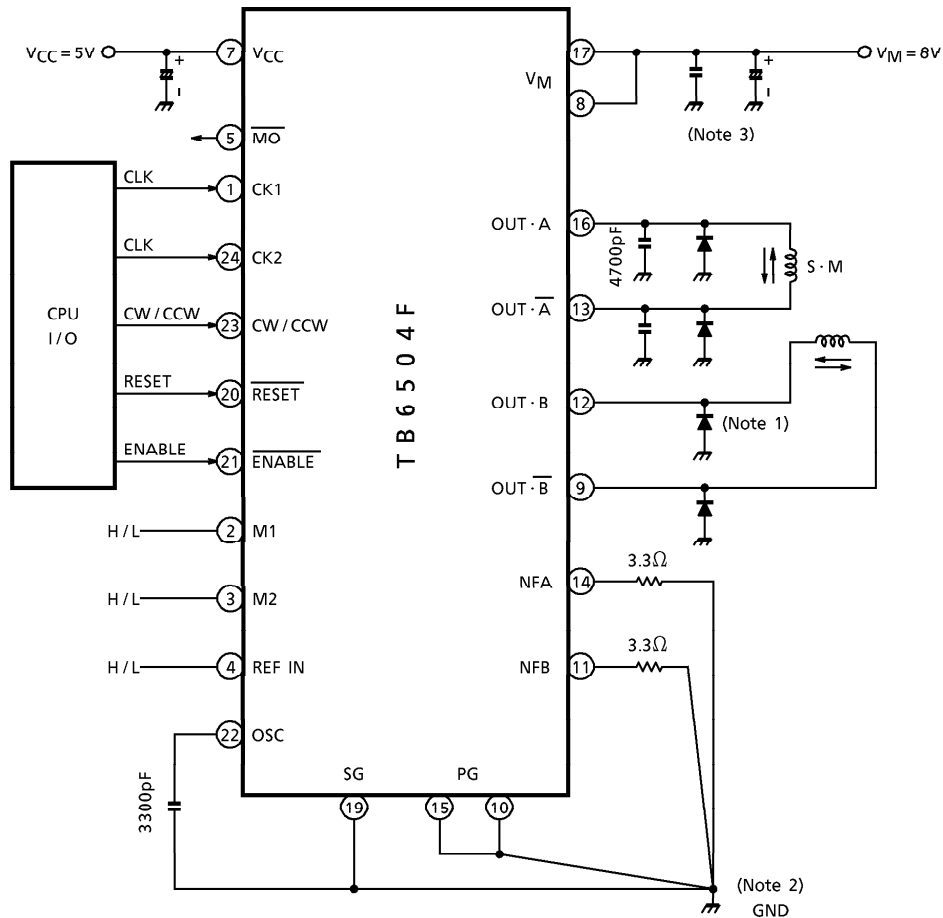
(Note) Not to take a GND with any non-connecting Pins.

AC ELECTRICAL CHARACTERISTIC, TEST CIRCUIT
CK (OSC)-OUT





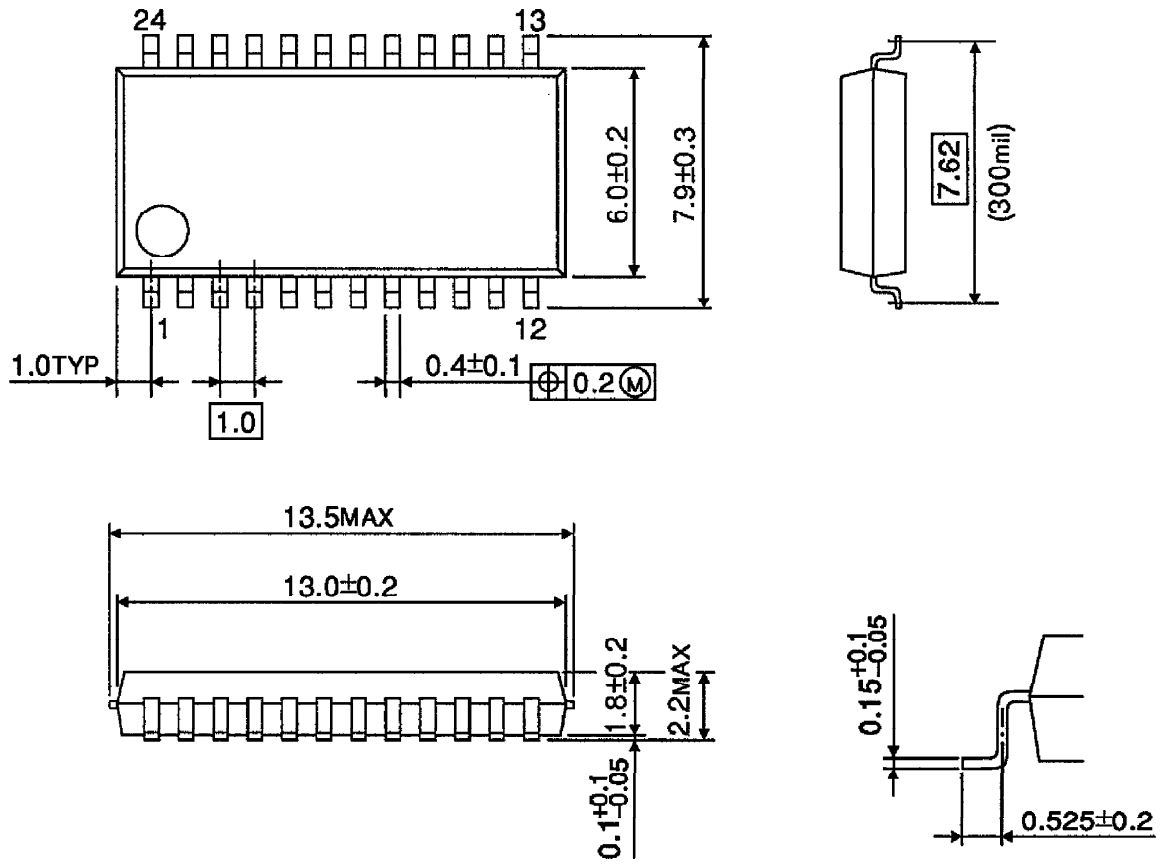
APPLICATION CIRCUIT



- (Note 1) Schottky diode (U1GWJ49) to be connected additionally between each output (pin 16/13/12/9) and GND for preventing Punch-through Current.
- (Note 2) GND pattern to be laid out at one point in order to prevent common impedance.
- (Note 3) Capacitor for noise suppression to be connected between the Power Supply (V_{CC} , V_M) and GND to stabilize the operation.
- (Note 4) Utmost care is necessary in the design of the output line, V_M and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING
SSOP24-P-300-1.00

Unit : mm



Weight : 0.32g (Typ.)