

TOSHIBA

TB6518F

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICONE MONOLITHIC

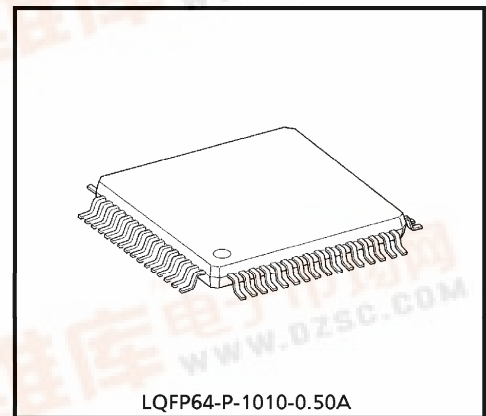
T B 6 5 1 8 F

VIDEO CAMERA CYLINDER MOTOR CONTROLLERS AND CAPSTAN MOTOR CONTROLLERS

The TB6518F is a single-chip IC for video camera cylinder motor controllers and capstan motor controllers. The cylinder section is a soft-switching pre-driver based on a 3-phase full-wave sensorless driver and 180° trapezoidal wave commutation control. The capstan section is a soft-switching pre-driver based on 3-phase full-wave drive and pseudo-sine wave commutation control.

FEATURES

- Output current : 10 mA (MIN.) (At $V_{CC} = 3.0\text{ V}$)
- Operating voltage : $V_{CC} = 2.7\sim 5.5\text{ V}$
- Motor voltage : $V_M = 2.7\sim 10\text{ V}$

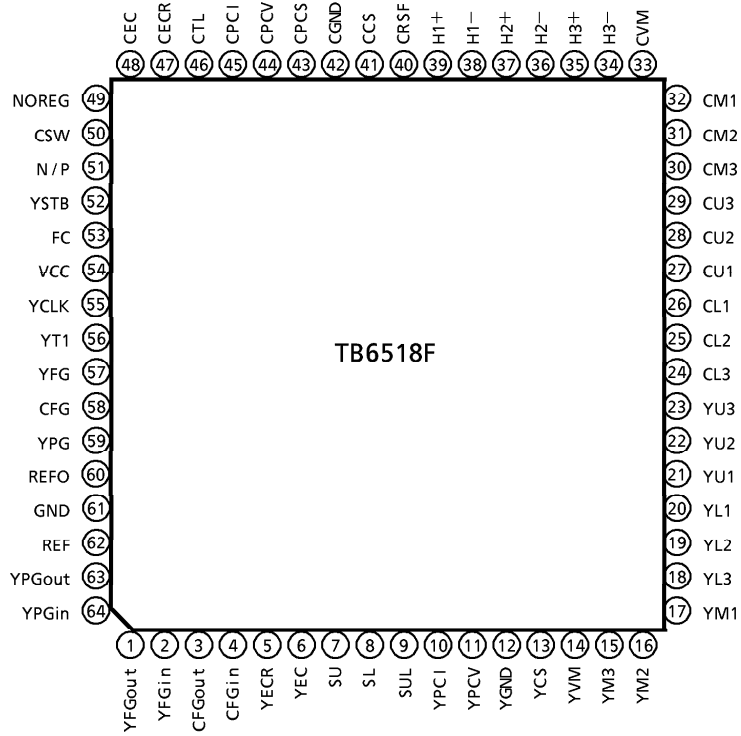


Weight : 0.34 g (Typ.)

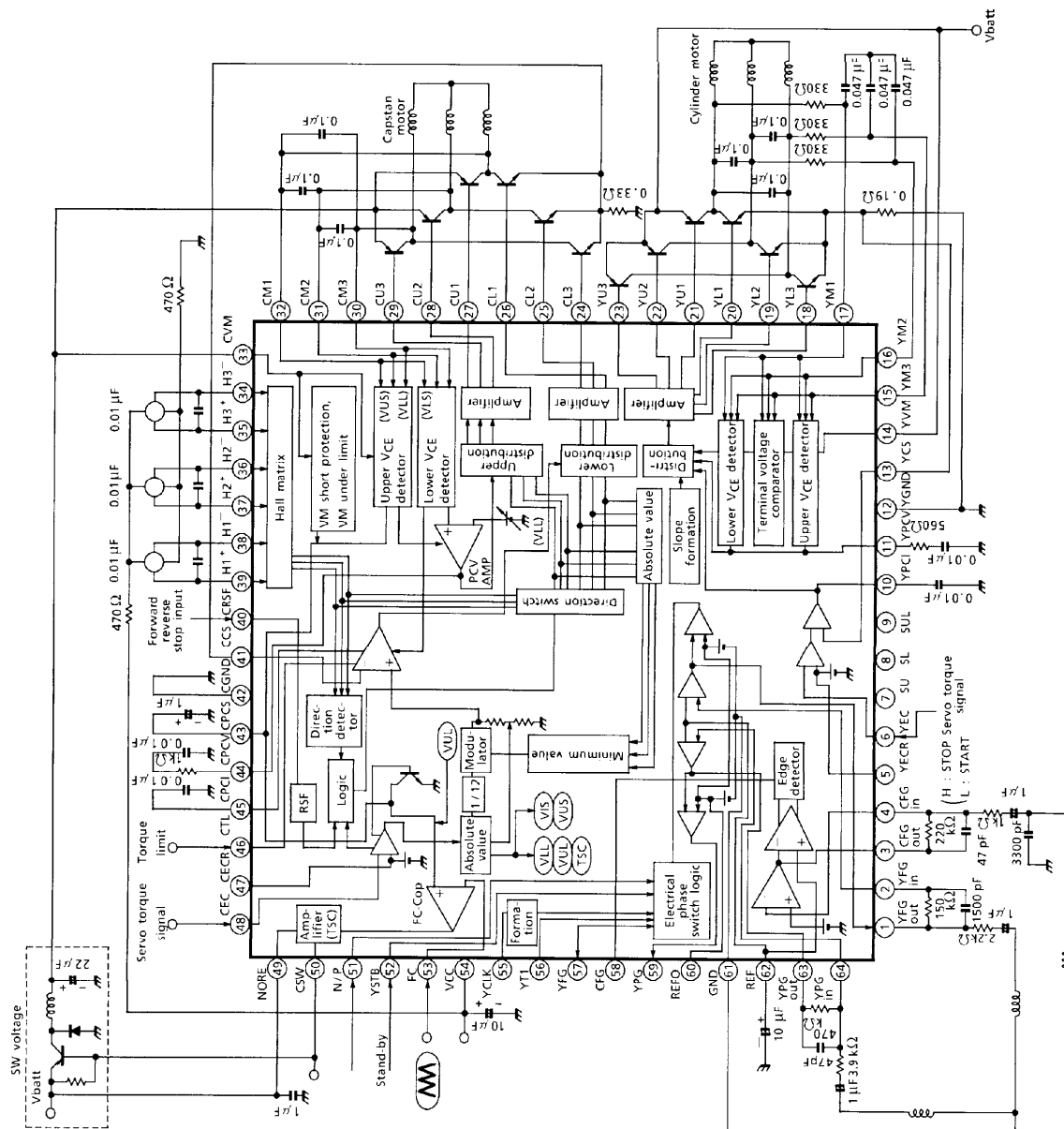
980910EBA1

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

PIN CONNECTION



BLOCK DIAGRAM



PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION	PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
1	YFGout	Cylinder part FG amplifier output terminal	38	H1-	Capstan motor hall element input terminal
2	YFGin	Cylinder part FG input terminal	39	H1+	∕
3	CFGout	Capstan part FG amplifier output terminal	40	CRSF	Capstan part directional control input terminal
4	CFGin	Capstan part FG input terminal	41	CCS	Capstan part current detection input terminal
5	YECR	Cylinder part torque control reference input terminal	42	CGND	Capstan part ground terminal
6	YEC	Cylinder part torque control input terminal	43	CPCS	Capstan part switching voltage control output
7	SU	Cylinder part upper slope voltage terminal	44	CPCV	Capstan part voltage feedback phase compensation
8	SL	Cylinder part lower slope voltage terminal	45	CPCI	Capstan part current feedback phase compensation
9	SUL	Cylinder part slope voltage terminal	46	CTL	Capstan part torque limit
10	YPCI	Cylinder part current feedback phase compensation	47	CECR	Capstan part torque control reference voltage
11	YPCV	Cylinder part voltage feedback phase compensation	48	CEC	Capstan part torque control input terminal
12	YGND	Cylinder part ground terminal	49	NOREG	SW Tr charge removal terminal
13	YCS	Cylinder part current detection input terminal	50	CSW	Capstan part switching pre-driver output terminal
14	YVM	Cylinder motor power voltage terminal	51	N/P	NTSC/PAL switch input
15	YM3	Cylinder motor coil terminal	52	YSTB	Cylinder part stand-by switch input
16	YM2	∕	53	FC	Switching comparator's triangular-wave input terminal
17	YM1	∕	54	VCC	Power voltage supply terminal for Logic
18	YL3	Cylinder motor lower side pre-drive output terminal	55	YCLK	Cylinder part clock input terminal
19	YL2	∕	56	YT1	Cylinder part test mode switch input terminal
20	YL1	∕	57	YFG	Cylinder part FG wave output terminal
21	YU1	Cylinder motor upper side pre-drive output terminal	58	CFG	Capstan part FG wave output terminal
22	YU2	∕	59	YPG	Cylinder part PG wave output terminal
23	YU3	∕	60	REFO	Amplifier part standard voltage
24	CL3	Capstan motor lower side pre-driver output terminal	61	GND	FG PG part ground terminal
25	CL2	∕	62	REF	FG and PG part reference voltage terminal
26	CL1	∕	63	YPGout	Cylinder part PG amplifier output terminal
27	CU1	Capstan motor upper side pre-driver output terminal	64	YPGin	Cylinder part PG input terminal
28	CU2	∕			
29	CU3	∕			
30	CM3	Capstan motor coil terminal			
31	CM2	∕			
32	CM1	∕			
33	CVM	Capstan motor power voltage terminal			
34	H3-	Capstan motor hall element input terminal			
35	H3+	∕			
36	H2-	∕			
37	H2+	∕			

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	6	V
Motor Supply Voltage (Note 1)	V _M	10	V
Supply Power I/O Voltage (Note 2)	V _{SWB}	10	V
Output Terminal Voltage (Note 3)	V _N	10	V
Input Terminal Voltage (Note 4)	V _I	-0.3~V _{CC} + 0.3	V
Power Dissipation	P _D	0.95 (Note 5)	W
Operating Temperature	T _{opr}	-20~75	°C
Storage Temperature	T _{stg}	-55~125	°C

(Note 1) Pin No. = 14, 33

(Note 2) Pin No. = 50

(Note 3) Pin No. = 15, 16, 17, 21, 22, 23, 27, 28, 29, 30, 31, 32

(Note 4) Pin No. = 2, 4, 5, 6, 13, 41, 46, 47, 48, 49, 51, 52, 53,
55, 56, 62, 64

(Note 5) Element

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{CC} = 3.0 V)
Cylinder part

No.	CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
1	Supply Current (1)	I _{CC} (1)	1	Shared use of the cylinder area and capstan area during operations	—	15	20	mA
2	Supply Current (2)	I _{CC} (2)	1	During STB, during STOP (CAP)	—	6.1	12	mA
3	ECR Voltage	V _{ECR}	1		1.3	1.5	1.7	V
4	Torque Control Input Current	Y _{IEC}	1	YEC = 0V	-5	-2	—	μA
5	Torque Control Input Offset Voltage	ΔEC	2		-100	50	100	mV
6	I/O Gain	Y _{Gio}	2		0.13	0.15	0.17	
7	Maximum Output Voltage	Y _{CSmax}	2	R _{YCS} = 0.27 Ω	145	168	183	mV
8	Lower Side Output Voltage (1)	V _L (1)	3	YCS = 54 mV	0.2	0.4	0.6	V
9	Lower Side Output Voltage (2)	V _L (2)	3	YECR = 1.5 V, YEC = 0 V	0.45	0.66	0.85	V
10	Upper Side Drive Current	I _U	4		—	—	-10	mA
11	Lower Side Drive Current	I _L	4		10	—	—	mA

Cylinder area

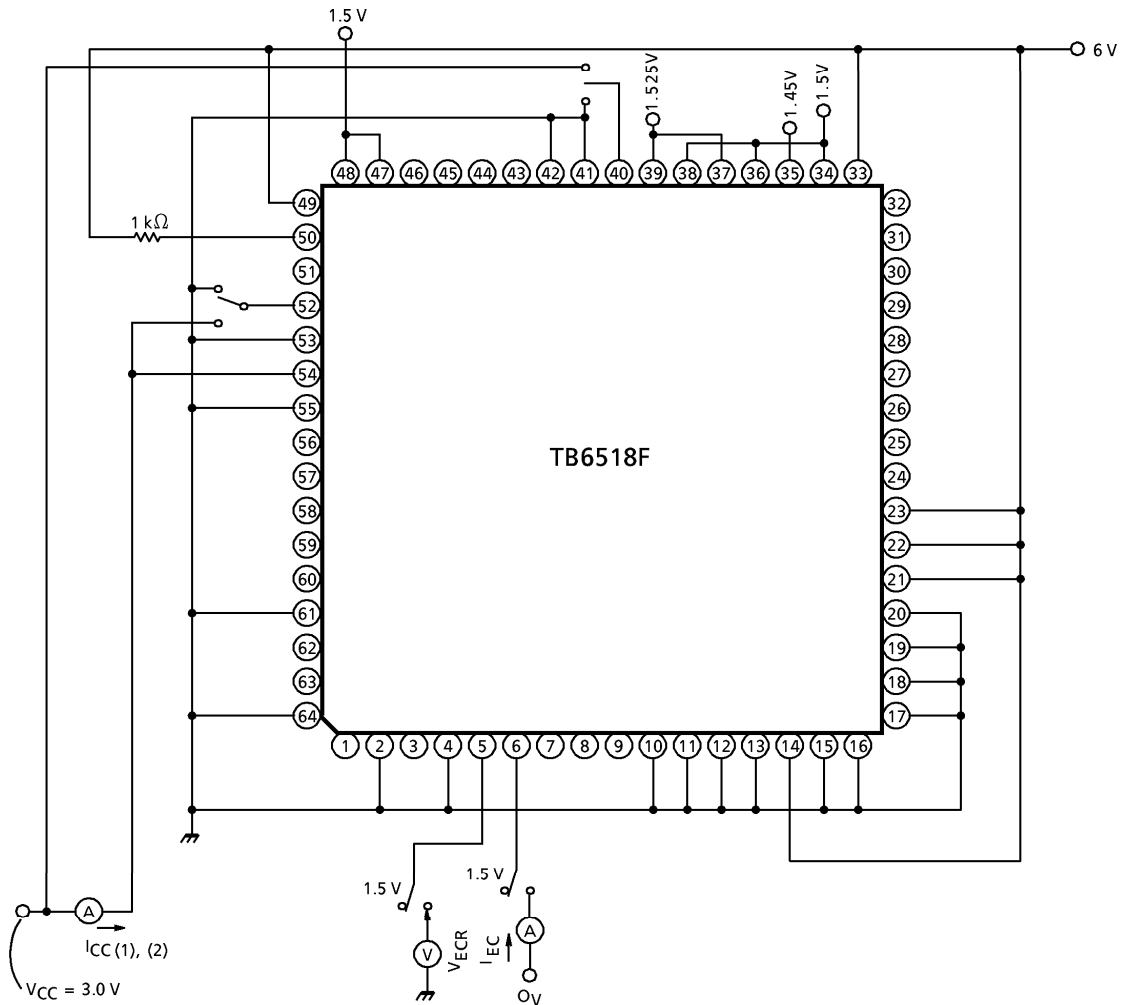
No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
12	FG Amplifier Gain	G _{FG}	5	V _{p-p} = 1.5 mV, f = 1 kHz	45	—	—	dB
13	YFG High Level	YFG (H)	6	I _{YFG} = -100 μA	1.0	2.8	—	V
14	YFG Low Level	YFG (L)	6	I _{YFG} = 100 μA	—	0.1	1.5	V
15	PG Amplifier Gain	G _{PG}	5	V _{p-p} = 1.5 mV, f = 1 kHz	45	—	—	dB
16	PG Amplifier Offset Voltage	ΔPG _{in}	6		0.4	0.5	0.6	V
17	YPG High Level	YPG (H)	6	I _{YPG} = -100 μA	1.0	2.8	—	V
18	YPG Low Level	YPG (L)	6	I _{YPG} = 100 μA	—	0.1	1.5	V
19	Stand-By Voltage	STB _{on}	7		2.0	—	—	V
20	Stand-By Release Voltage	STB _{off}	7		—	—	0.8	V
21	Stand-By Input Current	I _{STB}	7	V _{STB} = 0 V	-100	-30	—	μA
22	Amplifier Reference Voltage	V _{REF}	2		1.0	1.24	1.5	V
23	Current Leak when Mains Power Off	I _{ML}	8	YVM = 6 V	—	0.1	10	μA
24	Output Idle Voltage	YCS _{idle}	2	R _{YCS} = 0.27 Ω	—	0	5	mV
25	NTSC Operating Input Voltage	V _{NTSC}	6		2.0	—	—	V
26	PAL Operating Input Voltage	V _{PAL}	6		—	—	0.5	V
27	N/P Terminal Input Current	I _{N/P}	6	V _{N/P} = 3 V	—	114	200	μA

Capstan area

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
28	Torque Control Input Current	CEC	9	CEC = CECR = 1.5 V	-2	-1	—	μA
29	Torque Control Reference Voltage	CECR	9		1.3	1.5	1.7	V
30	Torque Control Input Voltage	CEC	10		0.2	—	2.8	V
31	Output Maximum Voltage	CCS _{max}	10	R _{CCS} = 0.34 Ω	0.19	0.23	—	V
32	Torque Control I/O Gain	CG _{io}	10		0.21	0.24	0.27	
33	Output Idle Voltage	CCS _{idle}	10		—	0	4	mV
34	Torque Control Input Offset	CEC _{ofs}	10		-100	41	100	mV
35	Torque Control Dead Zone	CEC _{dz}	10		30	82	130	mV
36	Low Side V _{CE} Voltage (1)	CVLL (1)	11	CCS = 60 mV	0.22	0.29	0.50	V
37	Low Side V _{CE} Voltage (2)	CVLL (2)	11	CEC = 0 V, CTL = 1.0 V	0.40	0.54	0.80	V

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
38	Hall Element Permissible Input Voltage	Hin	12		1.2	—	1.5	V
39	Hall Element Input Conversion Offset	Hofs	13		-8	-4.7	8	mV
40	TL-CS Offset	TLoFs	14	CTL = 20 mV	6	9.5	14	mV
41	Forward Rotation Control Voltage	Vf	15		—	—	0.5	V
42	Stop Control Voltage	Vs	15		1.2	—	2.0	V
43	Reverse Rotation Control Voltage	Vr	15		2.7	—	—	V
44	Ripple Cancel Rates	R	16	CCS = 60 mV	8	11.5	18	%
45	Upper Side Drive MAX Current	CI _U	17		10	16	—	mA
46	Low Side Drive MAX Current	CI _L	17		—	-12	-8	mA
47	SW Power Voltage Input Offset	CSWofs	18		-20	13	20	mV
48	SW Power Voltage Control Output Gain	CG _P CS	19		6	8	10	
49	SW Power Voltage Control Output Voltage (1)	VUD (1)	19	CEC = CECR, CPCS = 1.7 V	0.28	0.34	0.6	V
50	SW Power Voltage Control Output Voltage (2)	VUD (2)	19	CEC = 0 V	—	0	0.1	V
51	SW Power Voltage Output MAX Current	CI _{SWB}	19	CEC = 0 V	10	20	—	mA
52	FG Amplifier Loop Gain	CG _{FG}	20	External 1 k Ω , 220 k Ω Input 3 mV _{p-p} , 1 kHz	43	46	—	dB
53	FG Amplifier Output Voltage High Level	CFG _H	20		2.7	3.0	—	V
54	FG Amplifier Output Voltage Low Level	CFG _L	20		—	0.0	0.5	V
55	V _M Under Limit	CV _{ML}	21		1.13	1.45	1.88	V
56	V _M Short Protection	CV _{MS}	21		0.26	0.49	1.00	V
57	SW Output Enforced ONEC Voltage	SWEC	19		—	—	0.6	V
58	NOREG Terminal Current	I _{REG}	18		—	0	2.0	μ A

TEST CIRCUIT 1. $I_{CC(1)}$, $I_{CC(2)}$, V_{ECR} , Y_{IEC}



No. 1 $I_{CC(1)}$

Set $YSTB = 0V$, $YEC = 0V$, $YECR = 1.5V$, $CEC = 0V$, $CECR = 1.5V$ and $CRSF = 0V$ and then measure the current flowing into the V_{CC} terminal.

No. 2 $I_{CC(2)}$

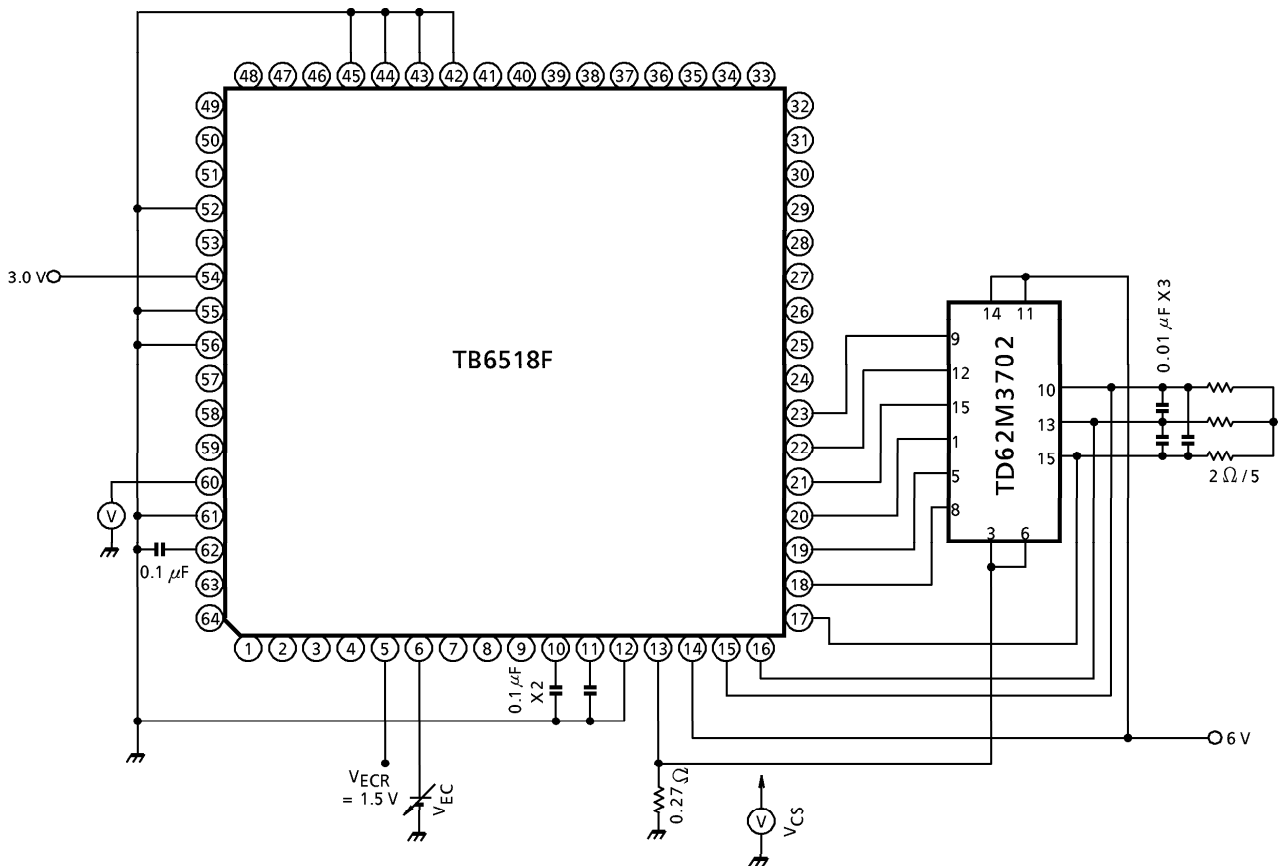
Set $YSTB = 3V$, $YEC = YECR = 1.5V$, $CEC = CECR = 1.5V$ and $CRSF = OPEN$ and then measure the current flowing into the V_{CC} terminal.

No. 3 V_{ECR}

Measure the potential of pin ⑤.

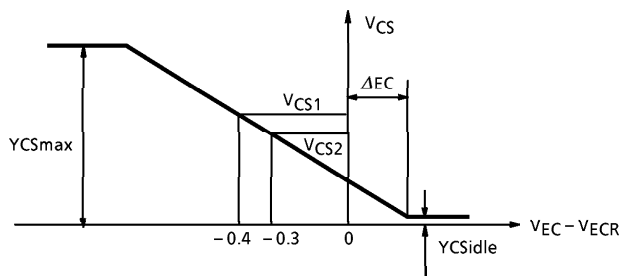
No. 4 Y_{IEC}

TEST CIRCUIT 2. ΔEC , Y_{Gio} , Y_{CSmax} , Y_{CSide} , V_{REF}



No. 5 ΔEC , No. 6 Y_{Gio} , No. 7 Y_{CSmax} , No. 24 Y_{CSide}

Set $Y_{ECR} = 1.5V$, change Y_{EC} from 0V to 3V and then measure the potential of pin ⑬.



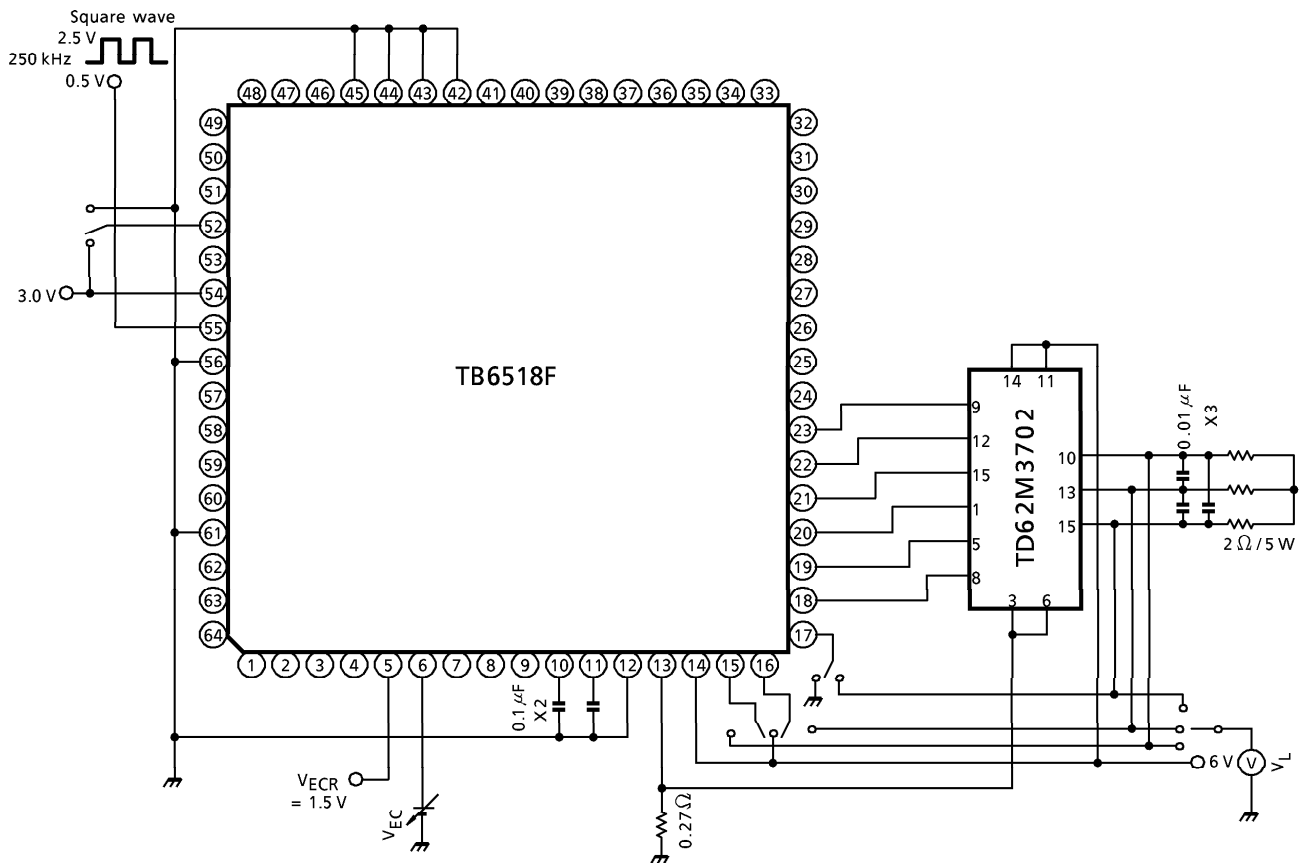
$$\Delta EC = V_{EC} - V_{ECR} \quad (V_{CS} \approx 0V)$$

$$Y_{Gio} = \frac{V_{CS1} - V_{CS2}}{0.1V}$$

No. 22 V_{REF}

Apply 3.0V to the V_{CC} and then measure the voltage of the REFO terminal.

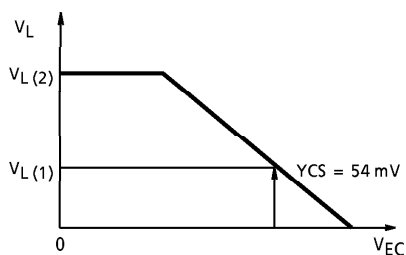
TEST CIRCUIT 3. $V_L(1)$, $V_L(2)$



No. 8 $V_L(1)$, No. 9 $V_L(2)$

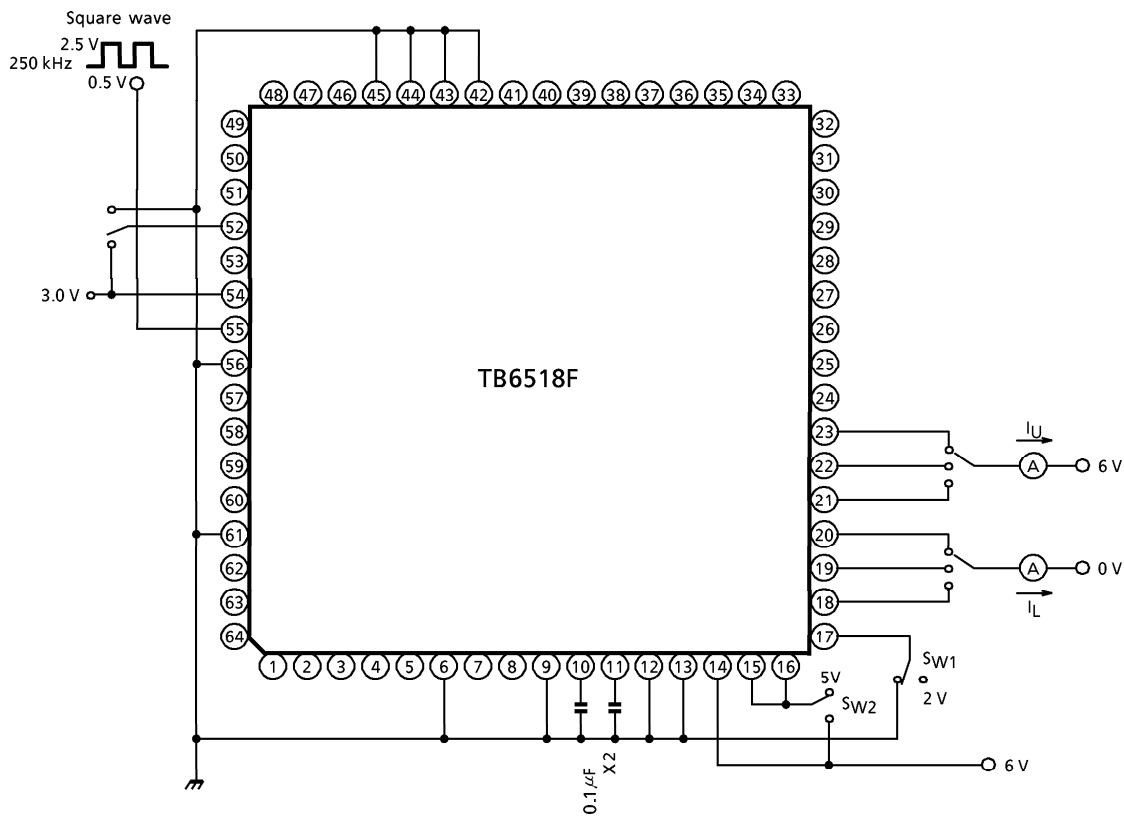
Change the YSTB terminal from H to L with $YMI = 0V$, $YM2 = 6V$ and $YM3 = 6V$ and then enter the following clock counts into the YCLK terminal in order to set the drive angle.

Connect the $YM1$, $YM2$ and $YM3$ terminals to PWTR after setting the drive angle and then carry out the measurement.



CLOCK	80	150	270
Terminal	YM3	YM1	YM2

TEST CIRCUIT 4. I_U, I_L

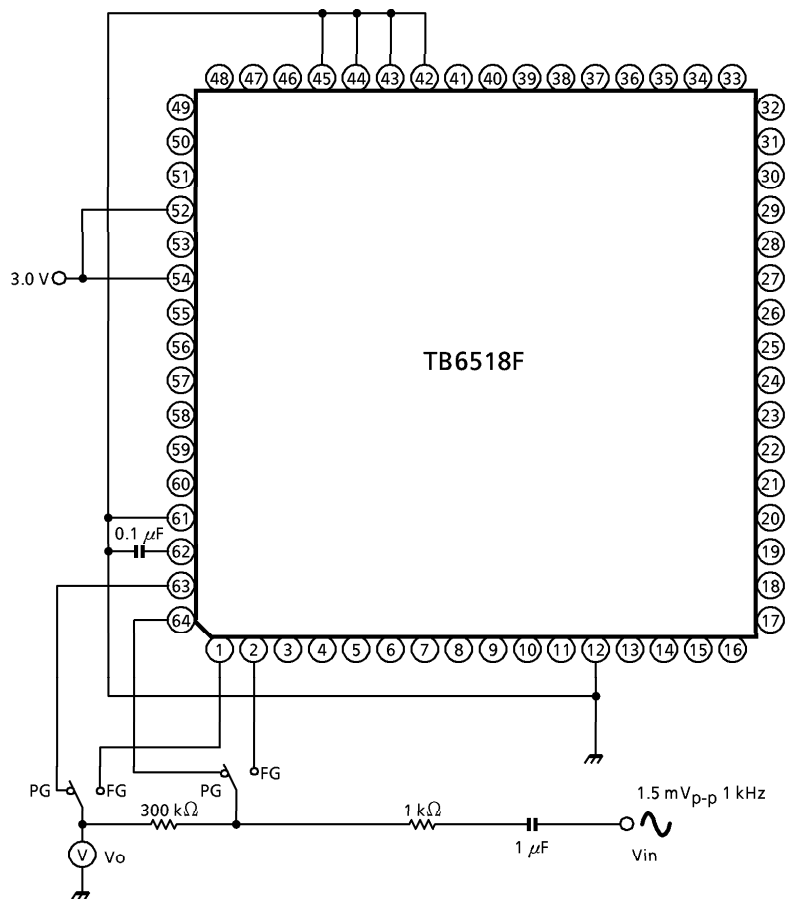


No. 10 I_U , No. 11 I_L

Change the YSTB terminal from H to L and then enter the following clock counts into the YCLK terminal in order to set the drive angle.

CLOCK	50		105		200	
Terminal	YU1	YL3	YU2	YL1	YU3	YL2
SW1	0V	2V	0V	2V	0V	2V
SW2	5V	6V	5V	6V	5V	6V

TEST CIRCUIT 5. G_{FG} , G_{PG}



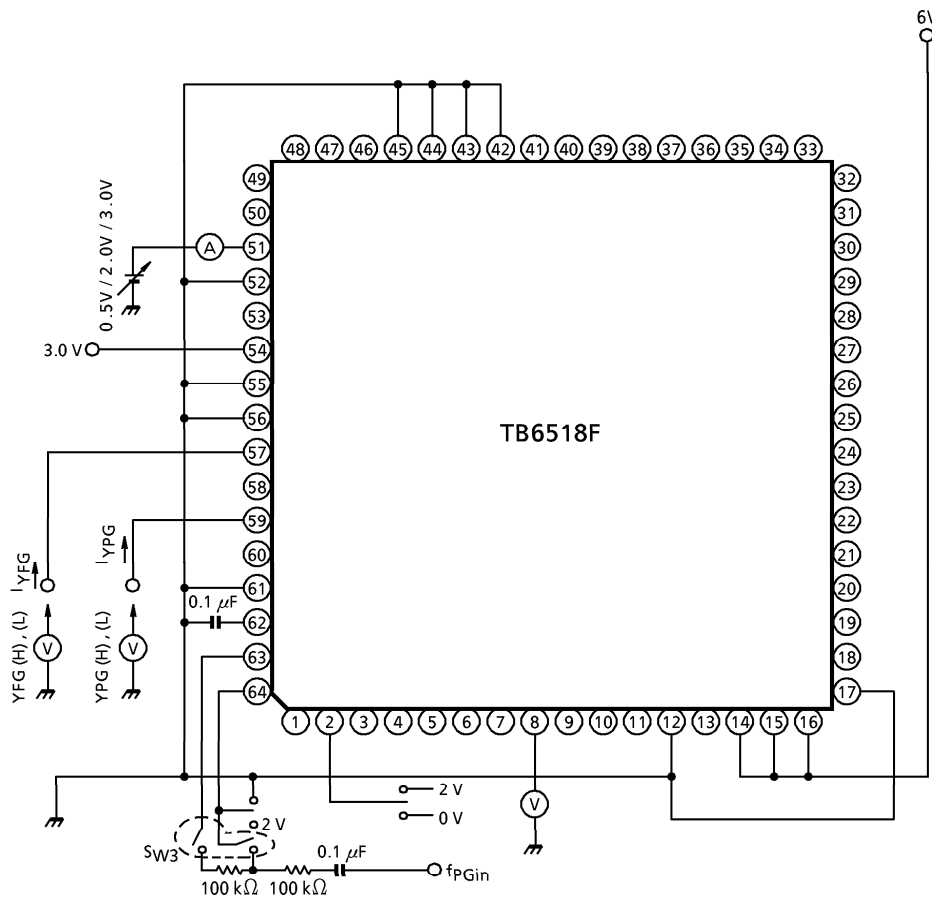
No. 12 G_{FG}

Set the SW to FG, measure V_o when $V_{in} = 1.5 \text{ mV}_{p-p}$ at 1 kHz and acquire $G_{FG} = 20 \log (V_o / V_{in})$.

No. 15 G_{PG}

Set the SW to PG, measure V_o when $V_{in} = 1.5 \text{ mV}_{p-p}$ at 1 kHz and acquire $G_{PG} = 20 \log (V_o / V_{in})$.

TEST CIRCUIT 6. YFG (H), YFG (L), ΔPGin, YPG (H), YPG (L), V_{NTSC}, V_{PAL}, I_{N/P}



No. 13 YFG (H)

Measure the potential of YFG when a current of $I_{YFG} = -100 \mu A$ is flowing after 2 V has been applied to YFGin and YFG has been set at H.

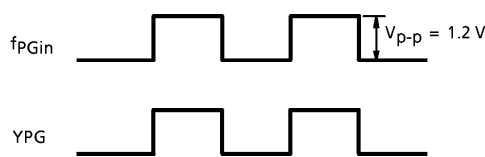
No. 14 YFG (L)

Measure the potential of YFG when a current of $I_{YFG} = -100 \mu A$ is flowing after 0 V has been applied to YFGin and YFG has been set at L.

No. 16 Δ PGin

Set SW3 on, input a 10 kHz square wave from f_{PGin} , set the f_{PGin} V_{p-p} to 1.2 V (Δ PGin = 0.6 V) and confirm that the YPG terminal is operating.

Also, set V_{p-p} to 0.8 V (Δ PGin = 0.4 V) and confirm that the YPG terminal is not operating.



No. 17 YPG (H)

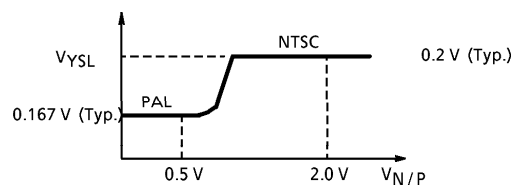
Measure the potential of YPG when a current of $I_{YPG} = -100 \mu A$ is flowing after 2 V has been applied to YPGin and YPG has been set at H.

No. 18 YPG (L)

Measure the potential of YPG when a current of $I_{YPG} = 100 \mu A$ is flowing after 0 V has been applied to YPGin and YPG has been set at L.

No. 25 V_{NTSC} , No.26 V_{PAL}

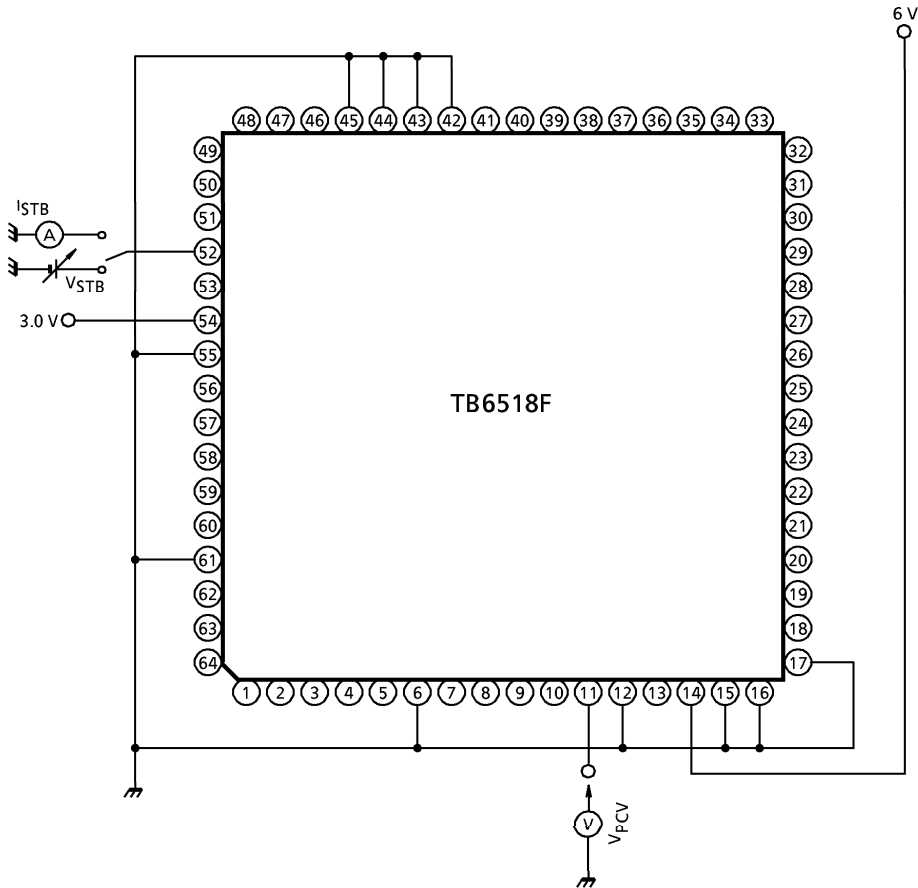
Confirm that 1.21 V is being applied to the YSUL terminal and that the voltage of the YSL terminal changes when the voltage applied to the N/P terminal is changed from 0.5 V to 2.0 V.



No. 27 $I_{N/P}$

Apply 3.0 V to the N/P terminal and measure the current flowing into the terminal.

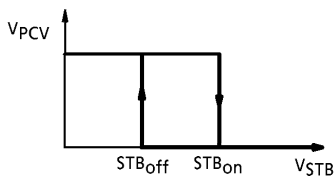
TEST CIRCUIT 7. STB_{on} , STB_{off} , I_{STB}



No. 19 STB_{on} , No. 20 STB_{off}

Change V_{STB} from 0 V to 3 V, and then from 3 V to 0 V, and measure V_{PCV} .

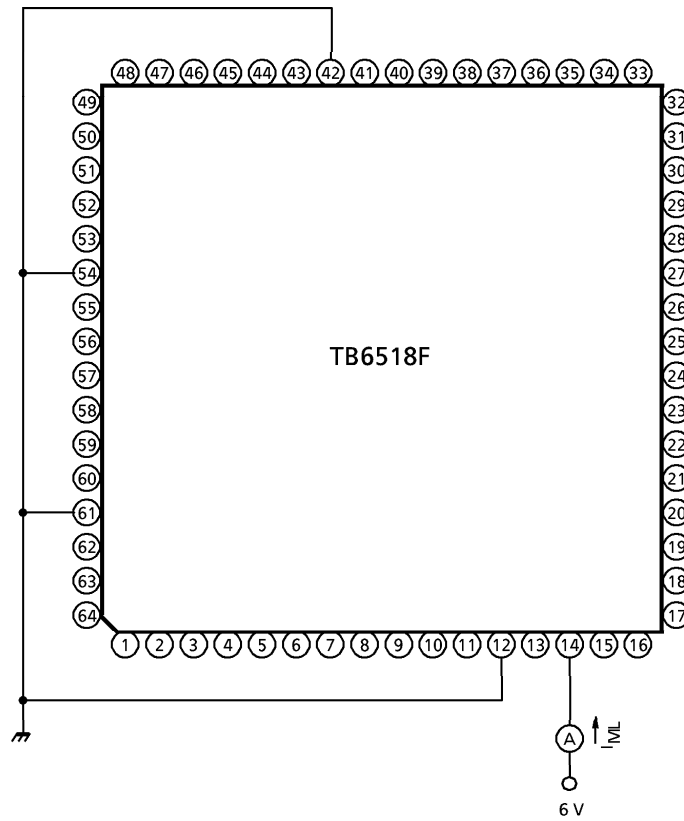
V_{STB} becomes STB_{on} when V_{PCV} changes from H to L, and becomes STB_{off} when V_{PCV} changes from L to H.



No. 21 I_{STB}

Measure I_{STB} when $V_{STB} = 0$ V.

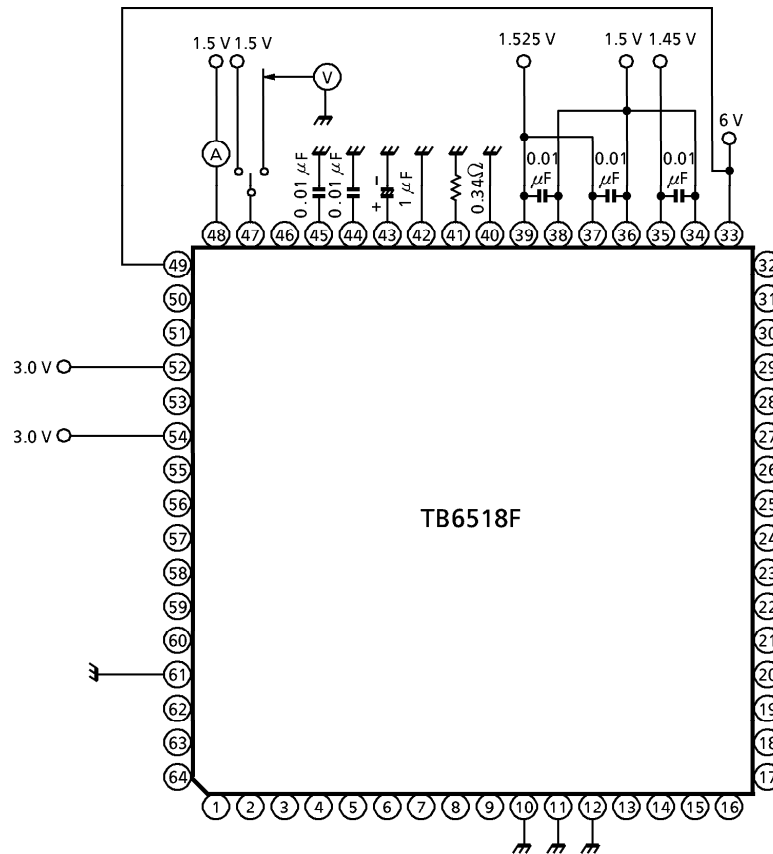
TEST CIRCUIT 8. I_{ML}



No. 23 I_{ML}

Measure the current that flows into pin ⑭ when $YVM = 6V$.

TEST CIRCUIT 9. C_{IEC} , C_{ECR}



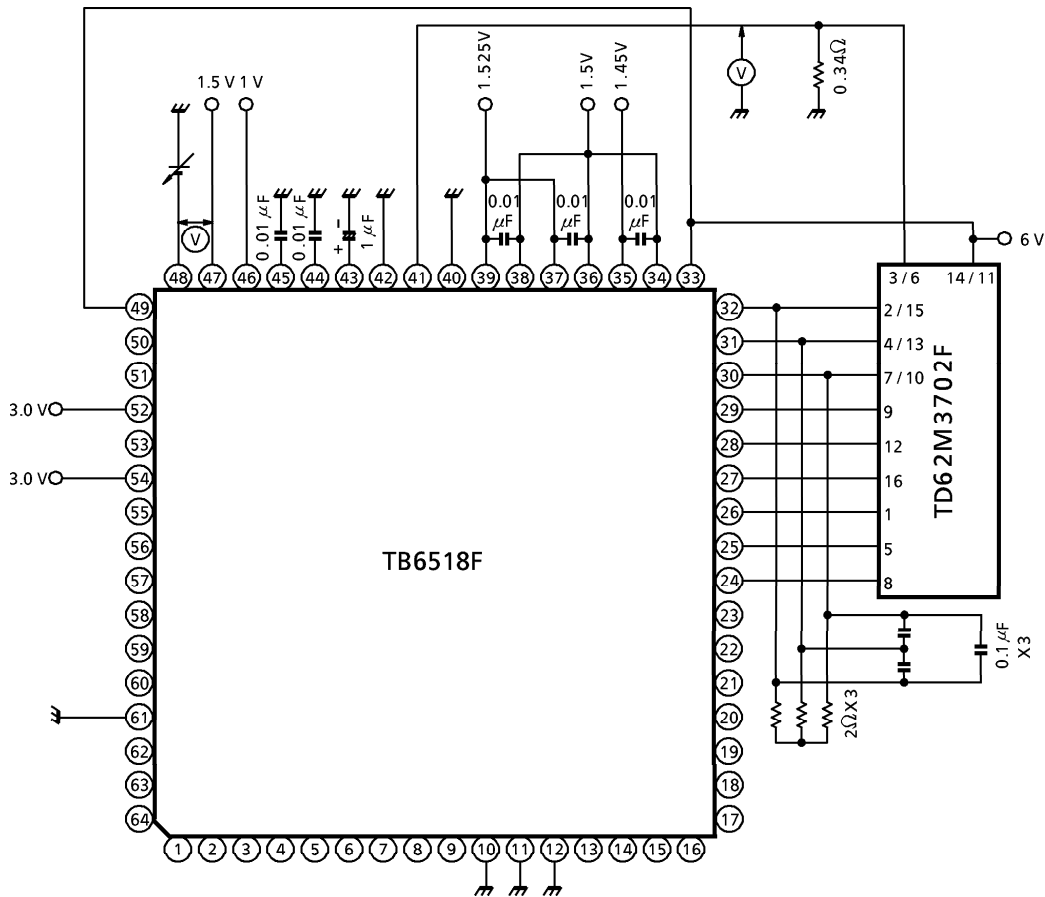
No. 28 C_{IEC}

Measure the current that flows into the CEC terminal with $C_{EC} = 1.5\text{ V}$ and $C_{ECR} = 1.5\text{ V}$.

No. 29 C_{ECR}

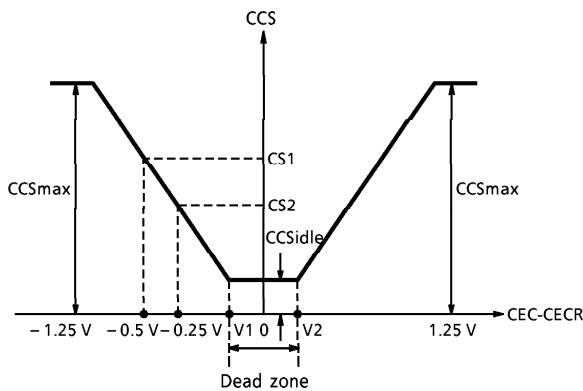
Measure the voltage of the CECR terminal.

TEST CIRCUIT 10. CEC, CCSmax, CGio, CCSidle, CECofs, CECdz



No. 30 No. 31 No. 32 No. 33 No. 34 No. 35

Set CTL = 1.0 V and CECR = 1.5 V, change CEC from 0 V to 3.0 V, measure the potential of the CCS terminal and confirm the V characteristics.



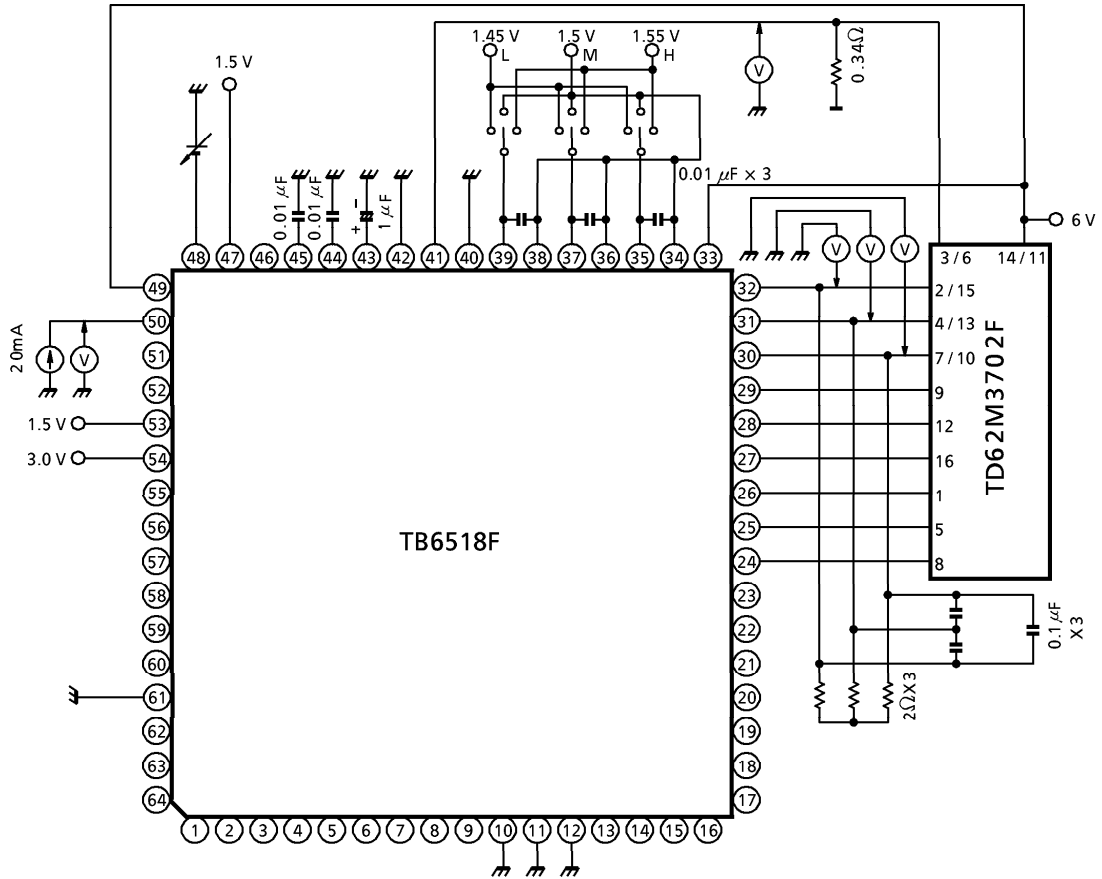
$$CGio = \frac{CS1 - CS2}{0.25 V}$$

CCSide : The CS potential within the dead zone

$$CECofs = \frac{V1 + V2}{2}$$

$$CECdz = V2 - V1$$

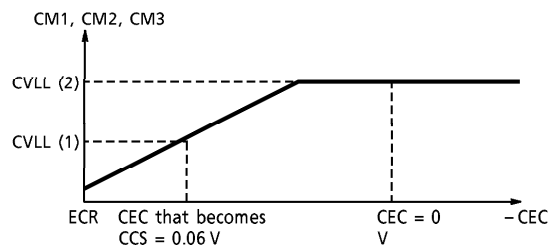
TEST CIRCUIT 11. CVLL (1), CVLL (2)



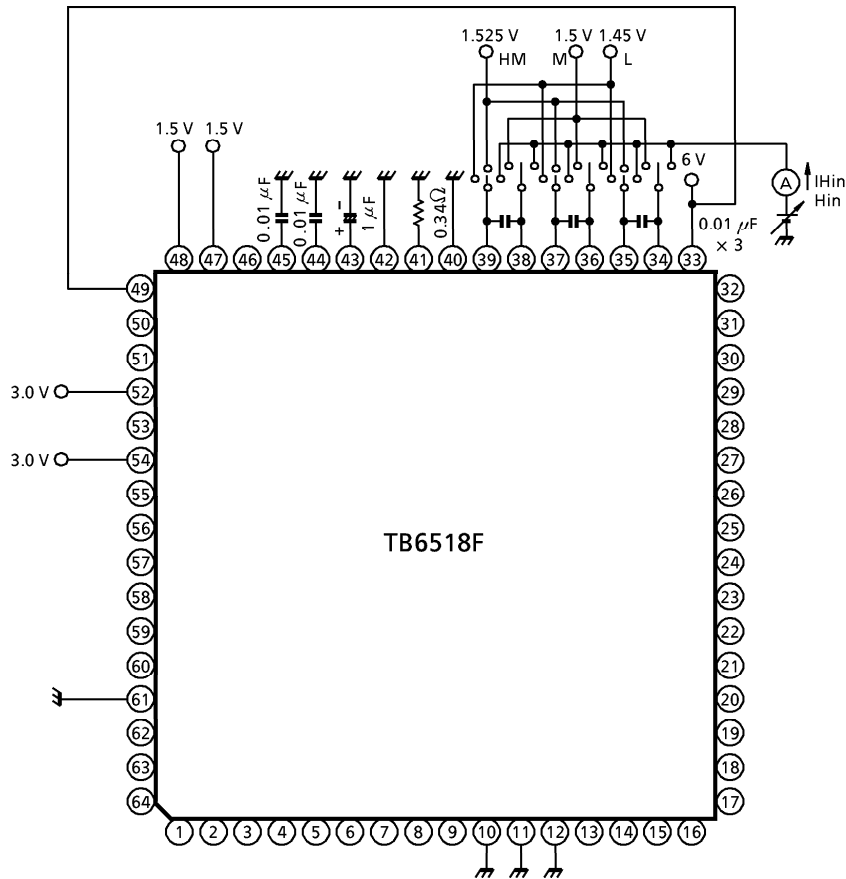
No. 36 CVLL (1), No. 37 CVLL (2)

Perform the settings laid out in the table below and measure the potential of the CM1, CM2 and CM3 terminals when the CEC voltage is adjusted to CCS = 0.06 V and when CEC = 0 V.

	H1 +	H2 +	H3 +	TEST TERMINAL
Setting 1	H	L	M	CM1
Setting 2	M	H	L	CM2
Setting 3	L	M	H	CM3



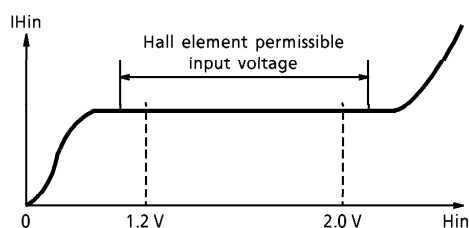
TEST CIRCUIT 12. Hin



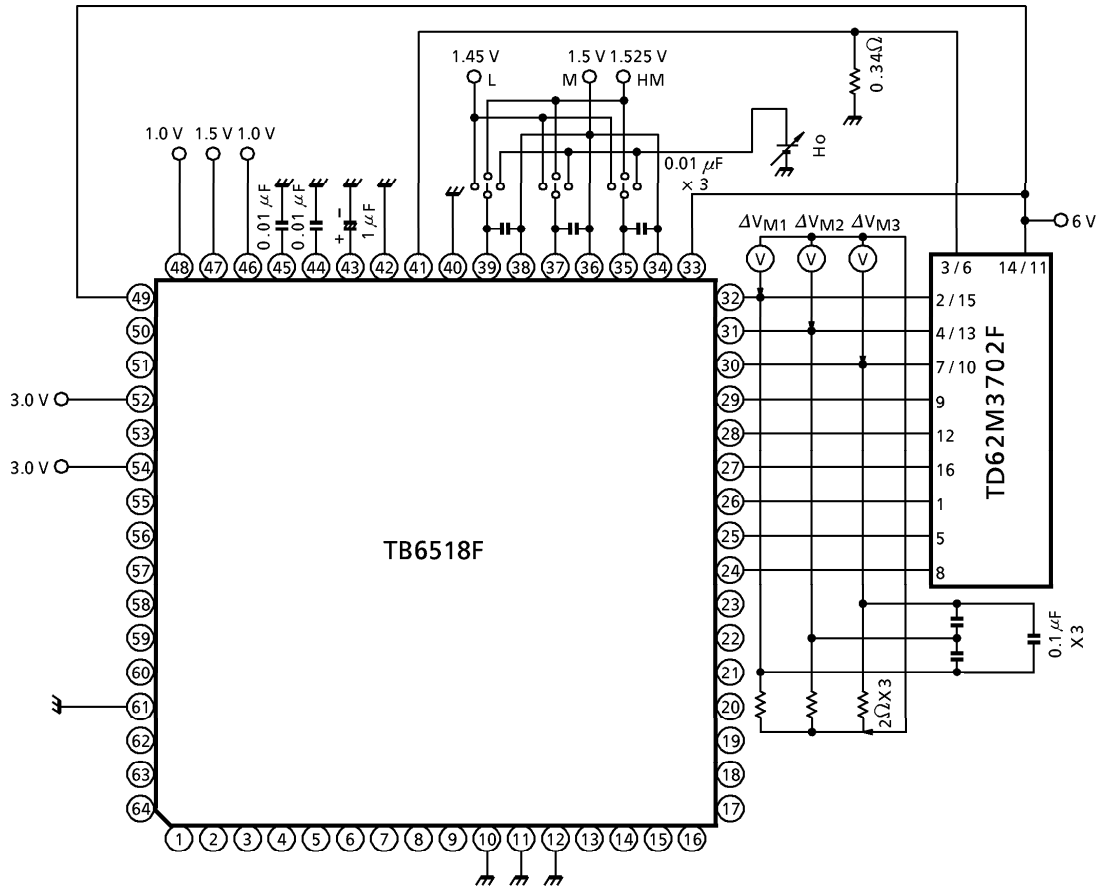
No. 38 Hin

Perform the settings laid out in the table below and then measure the voltage range of the IHin that does change rapidly in accordance with changes in the Hin.

	H1 +	H1 -	H2 +	H2 -	H3 +	H3 -
Setting 1	Hin	Hin	HM	M	L	M
Setting 2	L	M	Hin	Hin	HM	M
Setting 3	HM	M	L	M	Hin	Hin



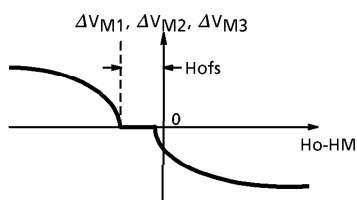
TEST CIRCUIT 13. HofS



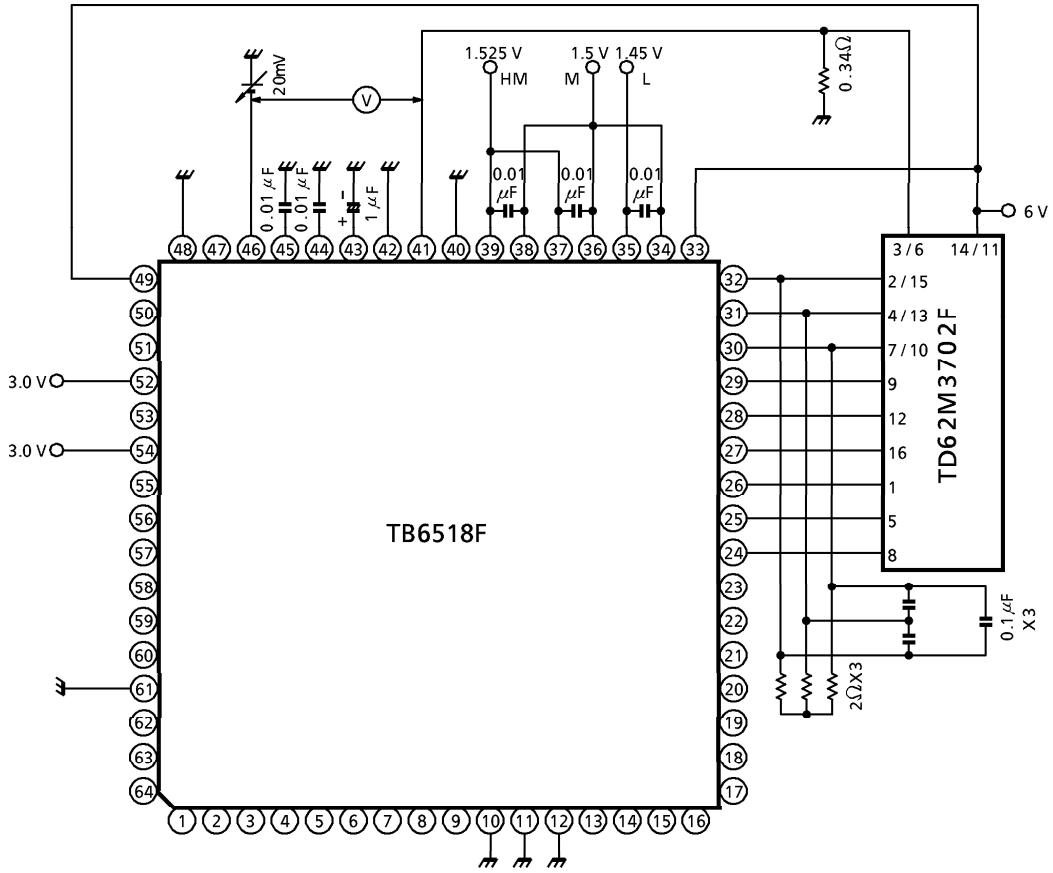
No. 39 HofS

Perform the settings laid out in the table below and then measure the hall element input conversion offset.

	H1 +	H2 +	H3 +	OFFSET MEASUREMENT
Setting 1	Ho	HM	L	$\Delta V_{M1} = 0$ difference between H1 + and H2 +
Setting 2	L	Ho	HM	$\Delta V_{M2} = 0$ difference between H2 + and H3 +
Setting 3	HM	L	Ho	$\Delta V_{M3} = 0$ difference between H3 + and H1 +

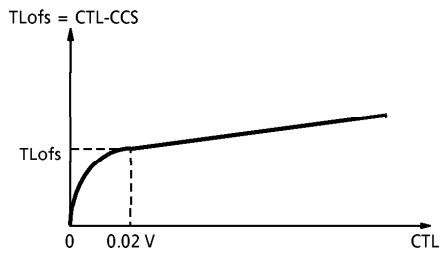


TEST CIRCUIT 14. TLofs

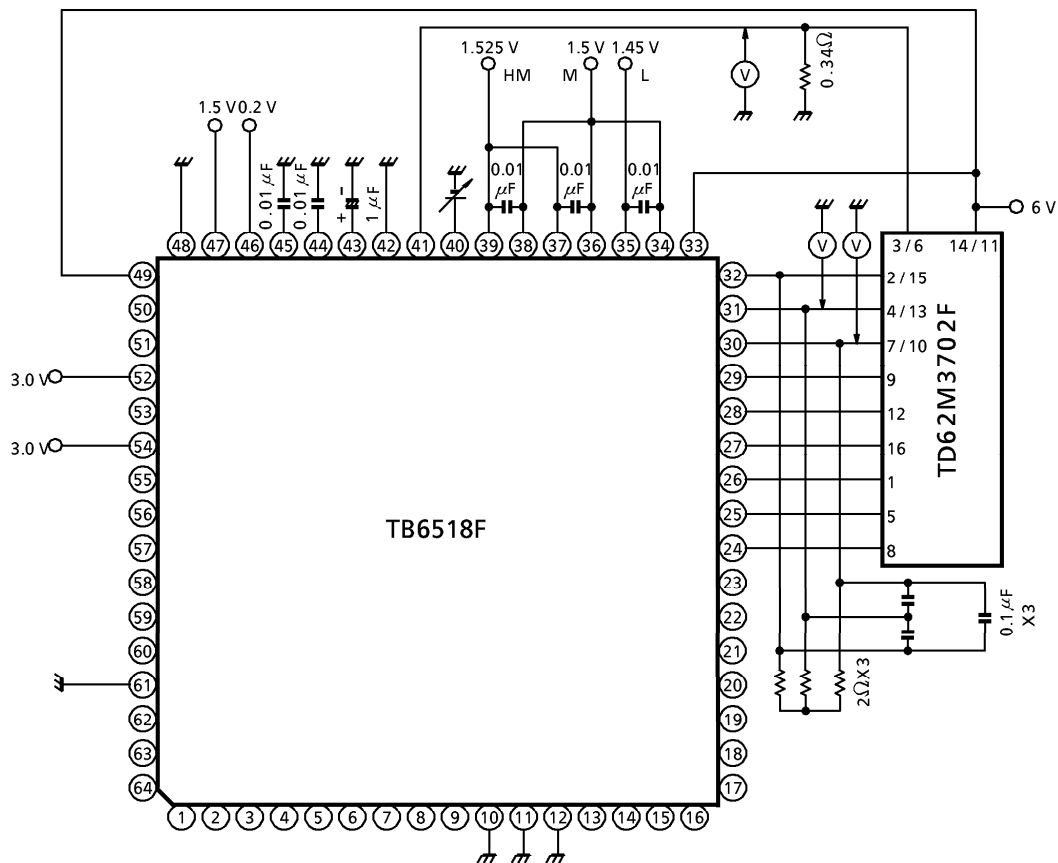


No. 40 TLofs

Measure the potential differential (CTL-CCS) of the CTL and CCS terminals when CTL = 0.02 V.

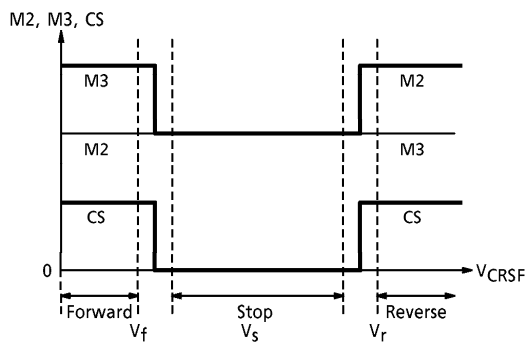


TEST CIRCUIT 15. V_f , V_s , V_r

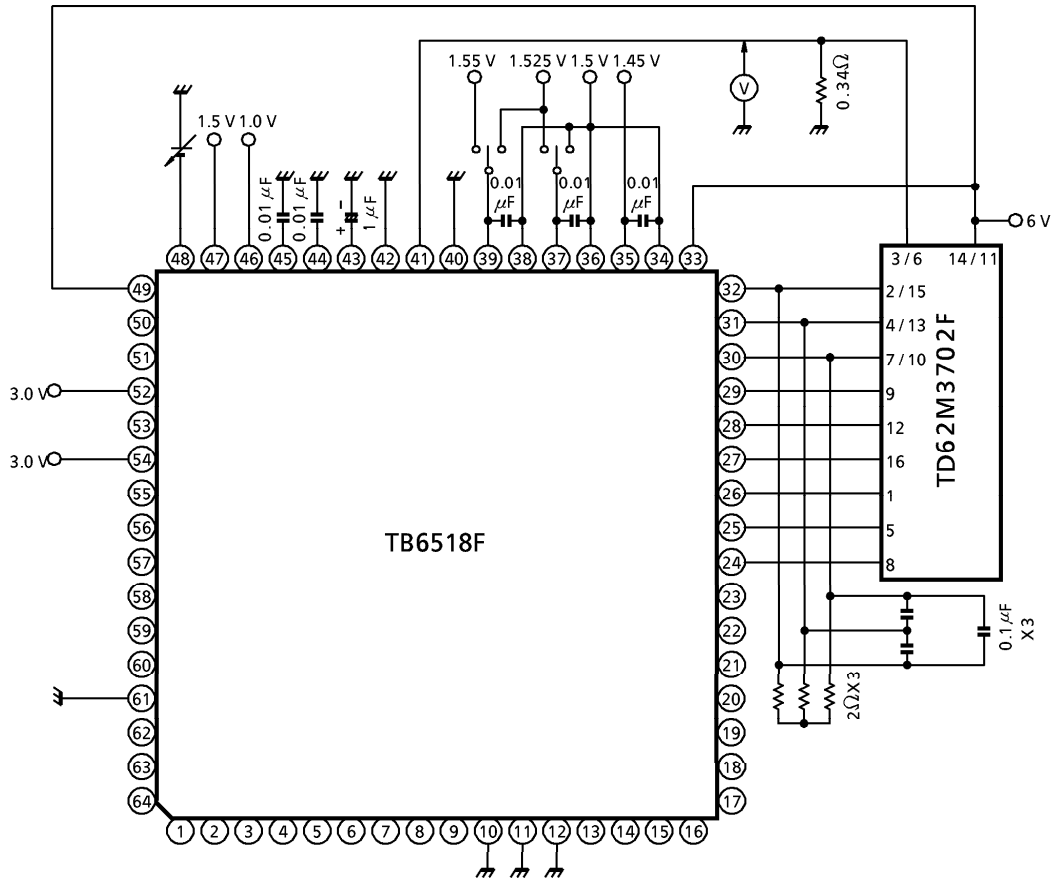


No. 41 V_f , No. 42 V_s , No. 43 V_r

Change CRSF from 0 V to 3.5 V, acquire the characteristics indicated in the following diagram and measure the threshold voltage.



TEST CIRCUIT 16. R

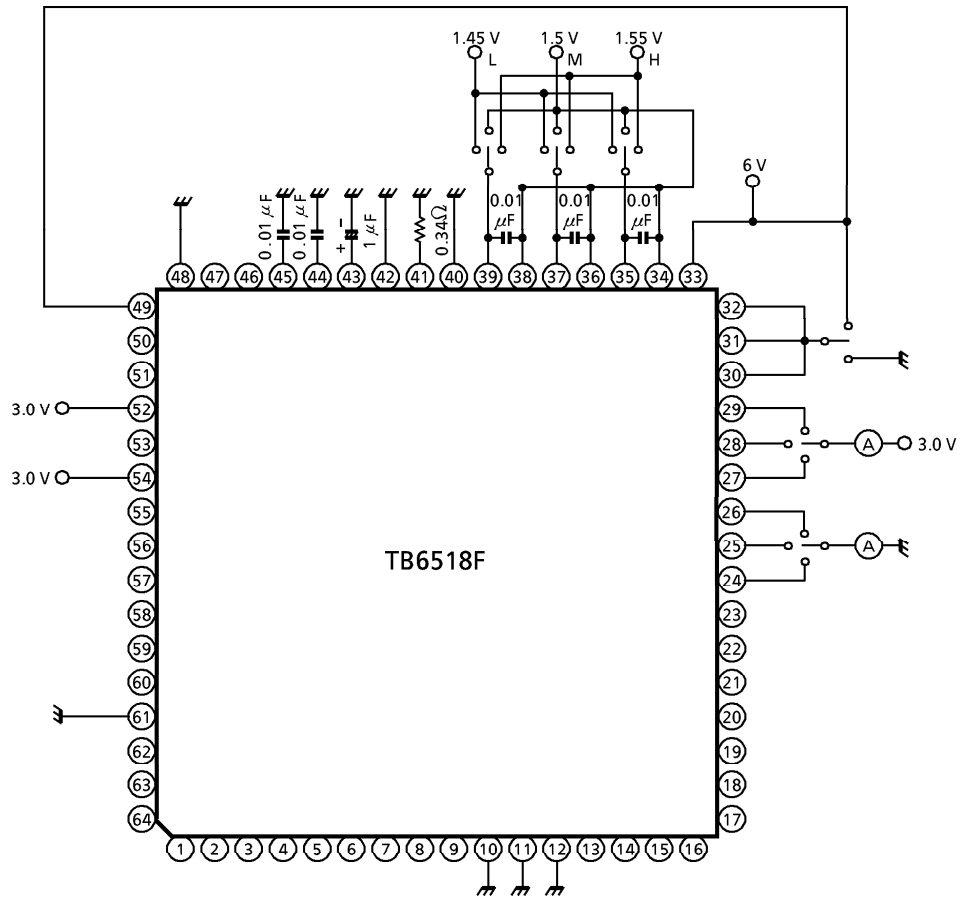


No. 44 R

Adjust the CEC voltage so that CCS becomes 0.06 V with H1+ = 1.525 V and H2+ = 1.525 V, and then measure CCS (CS_L) when H1+ = 1.525 V and H2+ = 1.525 V and CCS (CS_H) when H1+ = 1.55 V and H2+ = 1.5 V.

Then acquire :
$$R = \frac{CS_H - CS_L}{CS_L}$$

TEST CIRCUIT 17. CI_U , CI_L

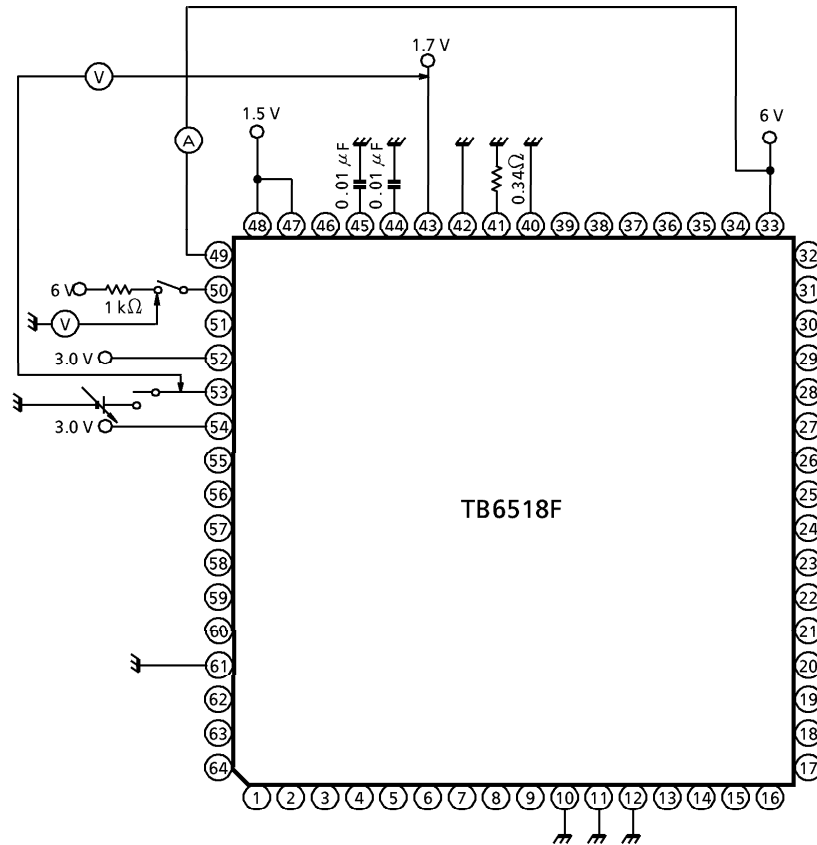


No. 45 CI_U , No. 46 CI_L

Perform the settings laid out in the table below and then measure the current that flows into the CU_1 , CU_2 and CU_3 terminals, and the CL_1 , CL_2 and CL_3 terminals.

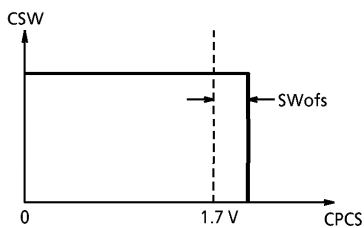
	H1 +	H2 +	H3 +	M1, M2, M3	TEST TERMINAL
Setting 1	L	H	M	GND	CU_1
Setting 2	M	L	H	GND	CU_2
Setting 3	H	M	L	GND	CU_3
Setting 4	H	L	M	V_M	CL_1
Setting 5	M	H	L	V_M	CL_2
Setting 6	L	M	H	V_M	CL_3

TEST CIRCUIT 18. CSWofs, I_{REG}



No. 47 CSWofs

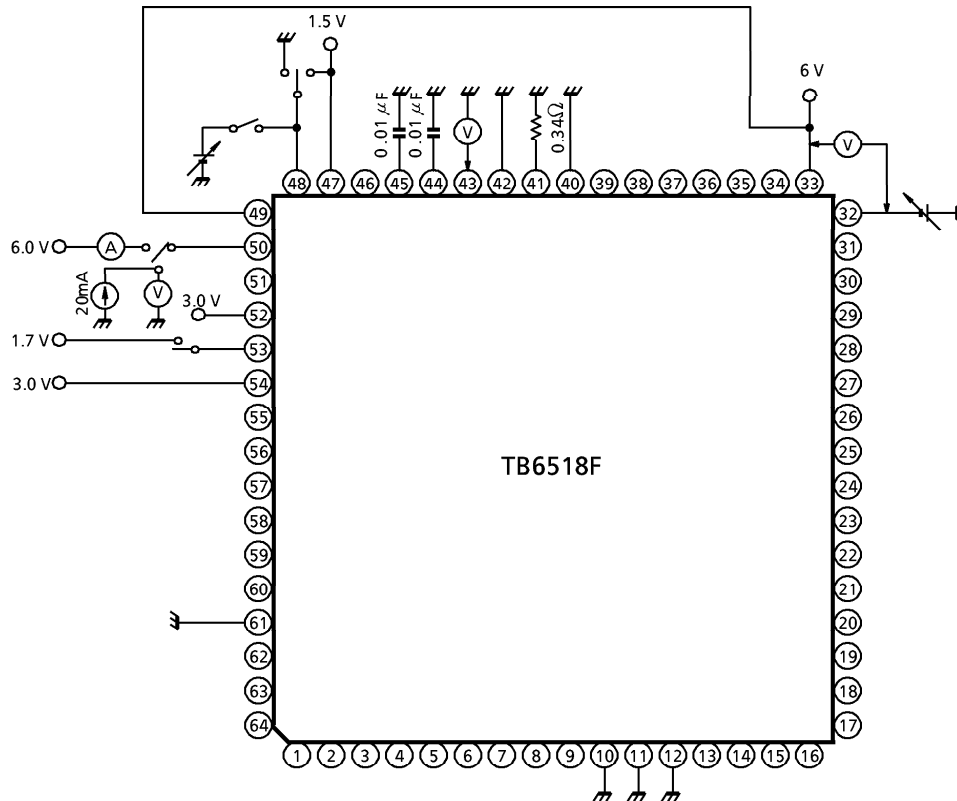
Set SPCS = 1.7V, change FC from 0V to 3.0V and measure the potential difference (FC – CPCS) of the FC terminal and the CPCS terminal when CSW changes from high to low.



No. 58 I_{REG}

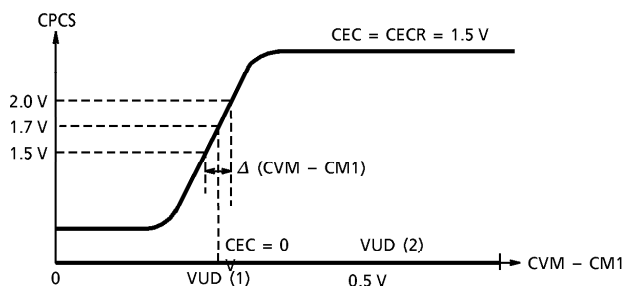
Measure the current of the NOREG terminal when 6V is applied with CVM = 6V and FC = 1.8V, and with the CSW terminal open.

TEST CIRCUIT 19. CG_PCS, VUD (1), VUD (2), Cl_SWB, SWEC



No. 48 CG_PCS, No. 49 VUD (1), No. 50 VUD (2)

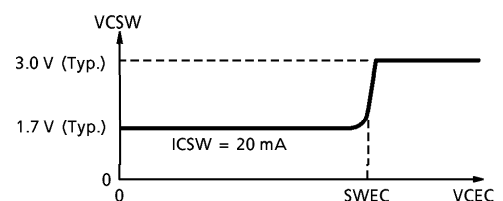
Set CEC = 0 V, change CM1 from 6 V to 5 V and measure the potential difference (CVM – CM1) of the CVM terminal and the CM1 terminal when the potential of the CPCS terminal becomes 1.7 V. Set CEC = CECR = 1.5 V, perform the same measurements as outlined below and acquire the characteristics indicated in the diagram below.



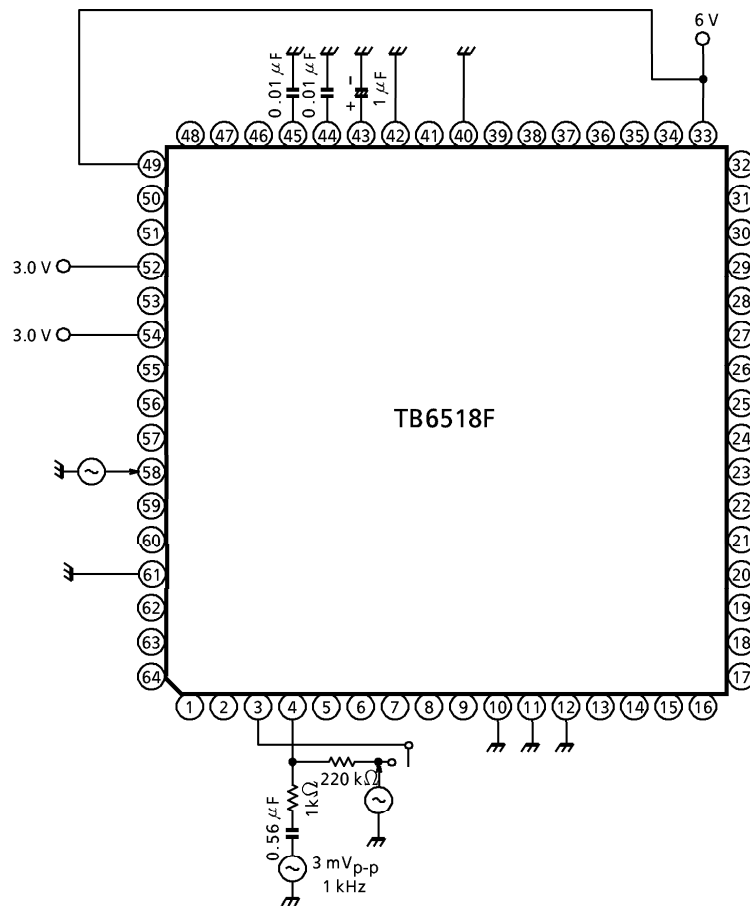
$$CG_{PCS} = \frac{2.0\text{ V} - 1.5\text{ V}}{\Delta (\text{CVM} - \text{CM1})}$$

No. 51 Cl_SWB, No. 57 SWEC

Set FC = 1.7 V, CEC = 0 V and CM1 = 6 V and measure the current that flows into the CSW terminal. Apply 10 mA to the CSW terminal, apply voltage to the CEC terminal and acquire the characteristics indicated in the diagram on the right-hand side.



TEST CIRCUIT 20. CG_{FG}, CFG_H, CFG_L

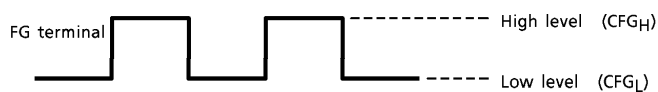


No. 52 CG_{FG} No. 53 CFG_H No. 54 CFG_L

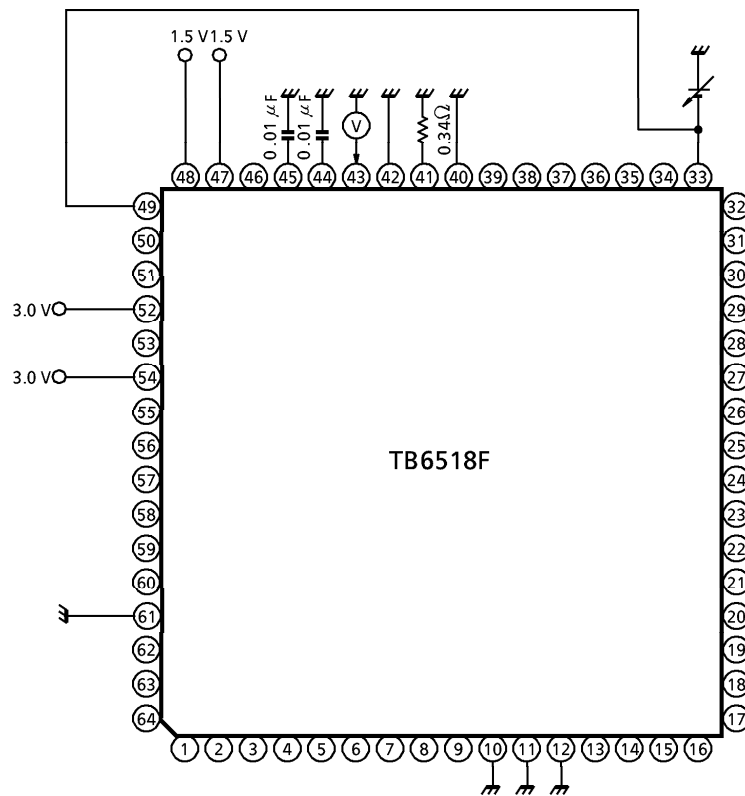
Set CFG_{out} = Vo and measure Vo when Vin = 3 mV_{p-p} at 1 kHz.

Then acquire : $CG_{FG} = 20 \log \frac{V_o}{V_{in}}$

Also, acquire the characteristics indicated in the diagram below and then measure the high level potential and low level potential of the CFG terminal's output wave form.

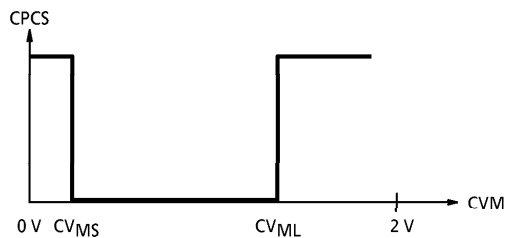


TEST CIRCUIT 21. CV_{ML} , CV_{MS}



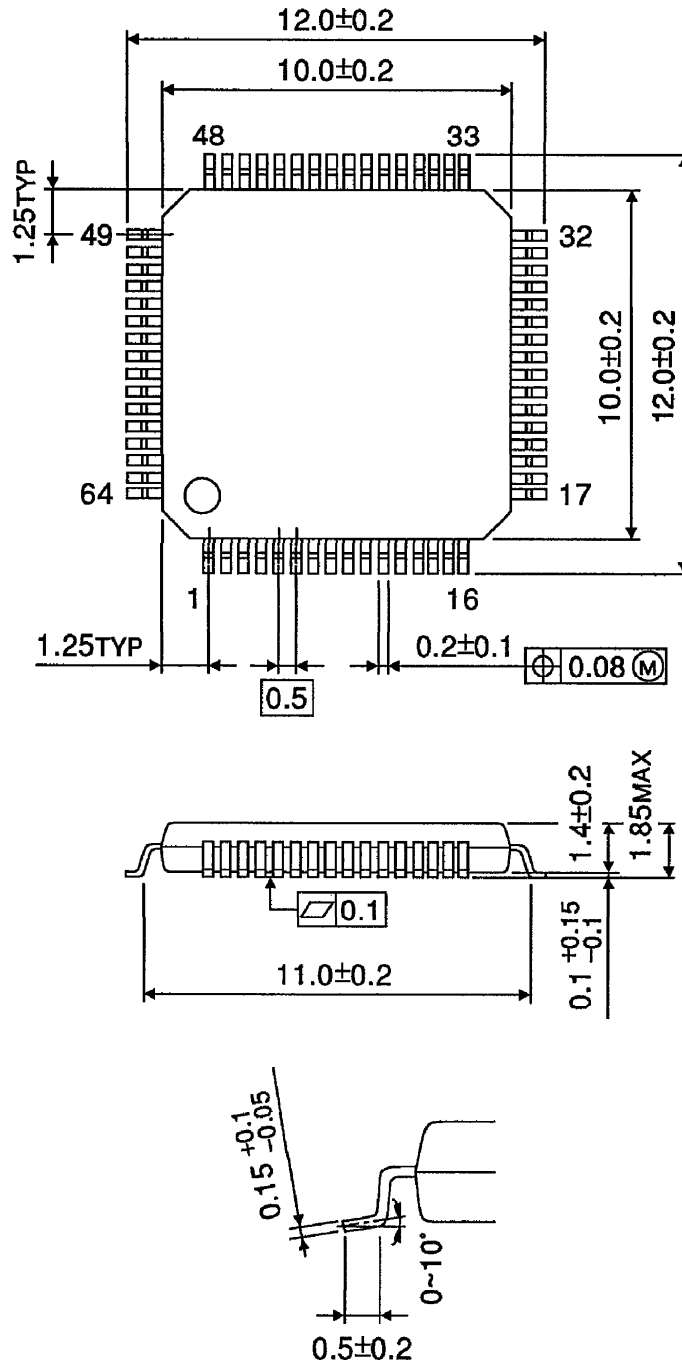
No. 55 CV_{ML} No. 56 CV_{MS}

Change CVM from 2 V to 0 V, acquire the characteristics indicated in the following diagram and measure the threshold voltage.



OUTLINE DRAWING
LQFP64-P-1010-0.50A

Unit : mm



Weight : 0.34 g (Typ.)