CMOS A/D CONVERTER

TOSHIBA (LOGIC/MEMORY)

TC35083P/F
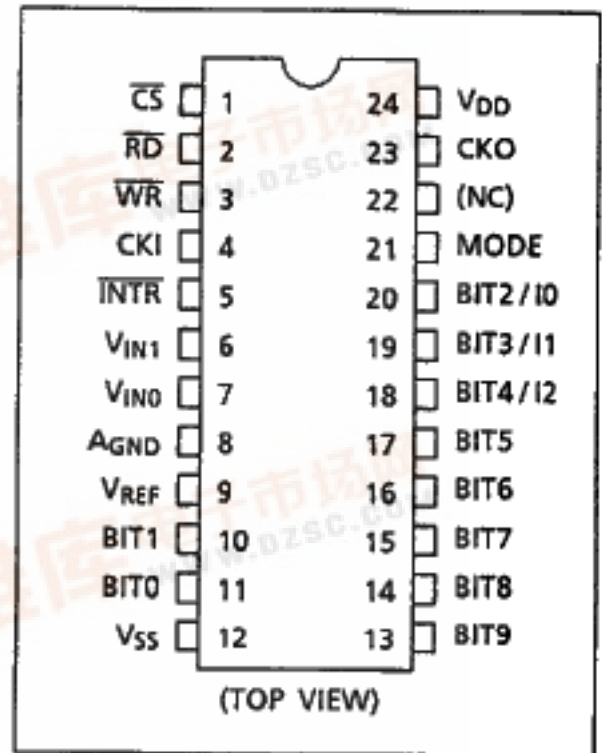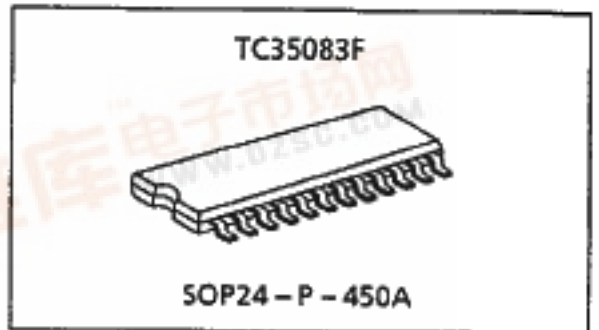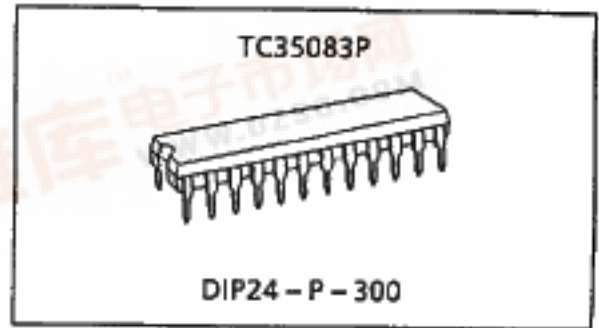
(10-BIT A-D CONVERTER)

1. GENERAL DESCRIPTION

The TC35083P/F is a high precision,and high speed monolithic CMOS 10-bit successive approximation A-D converter with a 10-bit parallel output or an 8-bit time sharing output. It has a 2 channel analog multiplexer input. Conversion data may be output in any of three forms depending on interface requirements. Also, having a built in oscillator circuit, the frequency can be set by means of an external resister (R) and capacitor (C).

2. FEATURES

□ High accuracy : 1.5LSB MAX. @Ta=-40~85°C

□ High speed conversion : $11\mu s$ @ fCKI = 2.0MHz

□ Single power supply : 5.0V±10%

□ Built-in 2-channel Analog multiplexer

□ Latched 3-state output

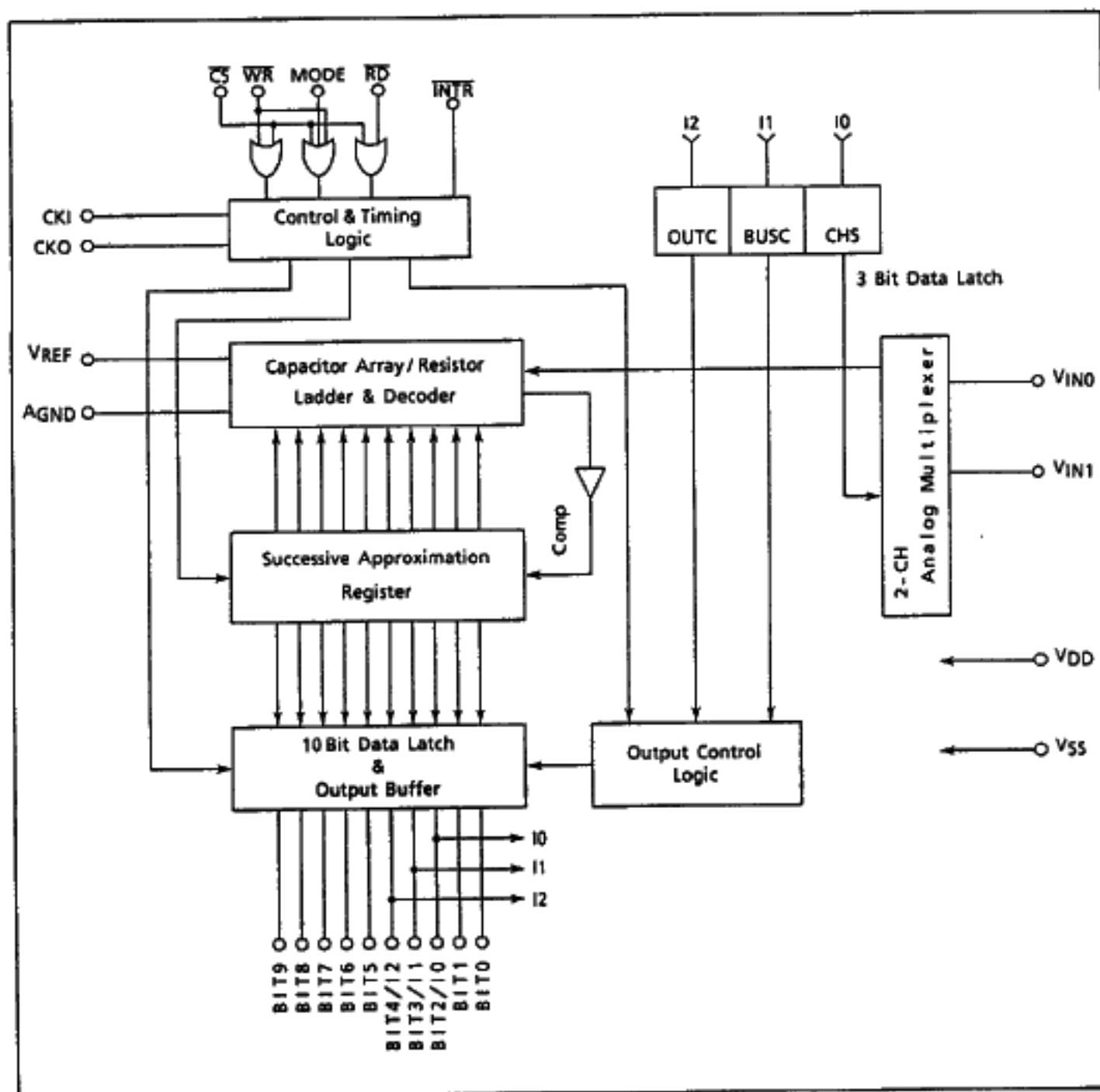□ Built-in clock oscillation circuit

□ Zero or full scale adjustment free

2.1 APPLICATIONS

□ Industrial Control Instruments

□ Electrical Wiring Apparatus

TC35083P

DIP24 – P – 300

TC35083F

SOP24 – P – 450A

$\overline{CS}$	1		24	V_{DD}
$\overline{RD}$	2		23	CKO
$\overline{WR}$	3		22	(NC)
CKI	4		21	MODE
$\overline{INTR}$	5		20	BIT2 / I0
V_{IN1}	6		19	BIT3 / I1
V_{IN0}	7		18	BIT4 / I2
A_{GND}	8		17	BIT5
V_{REF}	9		16	BIT6
BIT1	10		15	BIT7
BIT0	11		14	BIT8
V_{SS}	12		13	BIT9

(TOP VIEW)

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3. SYSTEM DESCRIPTION

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4. PIN DESCRIPTION

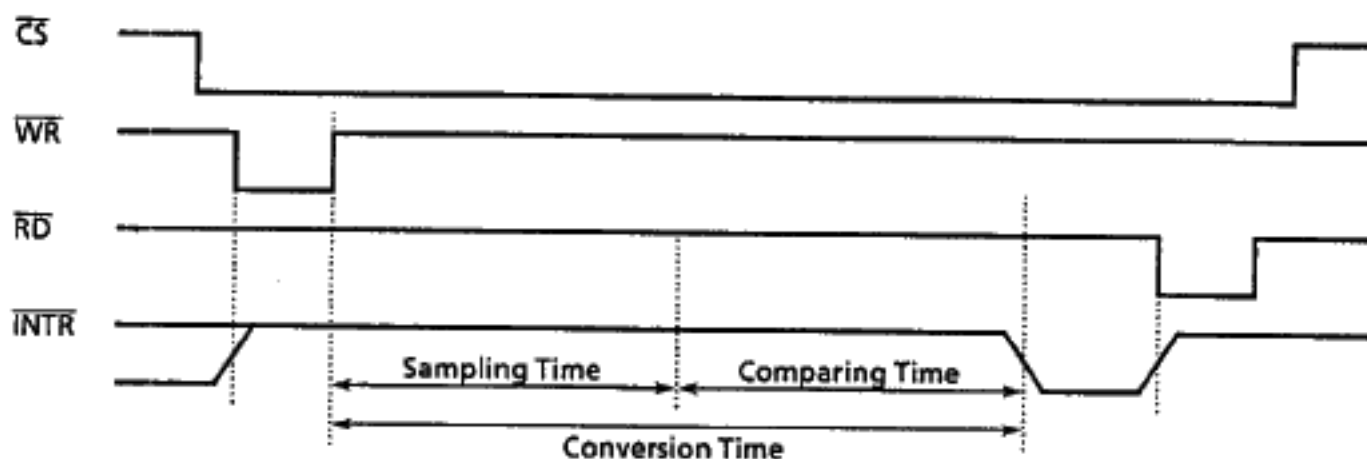| PIN.NO.	SYMBOL	NAME & FUNCTION
1	$\overline{CS}$	[Chip Select] Chip select signal input. When low, permits reading and writing.
2	$\overline{RD}$	[Read] Data read signal input. When low, conversion data is output.
3	$\overline{WR}$	[Write] Conversion start signal input. Conversion starts on the falling edge.
4	CKI	[Clock Input] Basic clock input for conversion operation.
5	$\overline{INTR}$	[Interrupt] End of conversion signal output. When conversion is completed, it goes low and at the first input $\overline{WR}$ or $\overline{RD}$, it goes high.
6	V_{IN1}	[Analog Input] Analog input terminal. Input voltage range is from A_{GND} to V_{REF}.
7	V_{IN0}	
8	A_{GND}	[Analog Ground] A_{GND} defines the zero level of V_{IN}.
9	V_{REF}	[Voltage Reference] V_{REF} defines the zero level of V_{IN}.
10	BIT1	[Data Output] Conversion Data Output Terminal.
11	BIT0	
12	V_{SS}	[Digital Ground] System Ground Terminal. Usually 0.0V.
13	BIT9	[Data Output / Input] Write mode ($\overline{WR}$ = "L") : I0 to I2 Input mode.
14	BIT8	According to MODE, writes the data of
15	BIT7	channel select (CHS) and output control (BUSC, OUTC).
16	BIT6	
17	BIT5	READ MODE ($\overline{RD}$ = 'L") : Outputs the conversion data from BIT0 to BIT9 according to output control status
18	BIT4 / I2	(BUSC, OUTC).
19	BIT3 / I1	BIT0 : LSB
20	BIT2 / I0	BIT9 : MSB
21	MODE	[Mode] Designates the data write mode (I0 to I2). MODE = "L" : I0 input mode MODE = "H" : I0 to I2 Input mode.
22	(NC)	[No connection]
23	CKO	[Clock output] Basic clock output terminal for conversion.
24	V_{DD}	[Power Supply] Supply Terminal 5.0V ± 10%.

Channel select table (for pins 6 and 7):

On channel	CHS
V_{IN0}	"L"
V_{IN1}	"H"

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6	V_{IN1}	[Analog Input] Analog input terminal. Input voltage range is from A_{GND} to V_{REF}.	On channel	CHS
7	V_{IN0}		V_{IN0} — "L" V_{IN1} — "H"	
8	A_{GND}	[Analog Ground] A_{GND} defines the zero level of V_{IN}.		
9	V_{REF}	[Voltage Reference] V_{REF} defines the zero level of V_{IN}.		
10	BIT1	[Data Output] Conversion Data Output Terminal.		
11	BIT0			
12	V_{SS}	[Digital Ground] System Ground Terminal. Usually 0.0V.		
13	BIT9	[Data Output / Input] Write mode ($\overline{WR}$ = "L") : I0 to I2 Input mode. According to MODE, writes the data of channel select (CHS) and output control (BUSC, OUTC). READ MODE ($\overline{RD}$ = 'L') : Outputs the conversion data from BIT0 to BIT9 according to output control status (BUSC, OUTC). BIT0 : LSB BIT9 : MSB		
14	BIT8			
15	BIT7			
16	BIT6			
17	BIT5			
18	BIT4 / I2			
19	BIT3 / I1			
20	BIT2 / I0			
21	MODE	[Mode] Designates the data write mode (I0 to I2). MODE = "L" : I0 input mode MODE = "H" : I0 to I2 input mode.		
22	(NC)	[No connection]		
23	CKO	[Clock output] Basic clock output terminal for conversion.		
24	V_{DD}	[Power Supply] Supply Terminal 5.0V ± 10%.		

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5.2 SYSTEM INITIALIZATION

When $\overline{CS}$ and $\overline{WR}$ are set low at the same time, all circuits except the output latch circuit are reset. If the power is switched "ON" or a wrong operation occurs, reset the system and run at least one conversion cycle as a dummy.

5.3 A to D CONVERSION

$\overline{CS}$ and $\overline{WR}$ set low at the same time and write the channel select (CHS) and output control (BUSC, OUTC) are set according to MODE. The conversion starts at the first edge and after a certain period, $\overline{INTR}$ goes low. When $\overline{CS}$ and $\overline{RD}$ are low, conversion data is output from BIT0 to 9 according to the output control,. After conversion is completed and the first read signal ($\overline{RD}$) or the first write signal ($\overline{WR}$) goes low, $\overline{INTR}$ goes high.

Sampling Time (Tsamp.) $= 8/f_{CKI} + \alpha$

Comparing Time.(Tcomp.) $= 13/f_{CKI}$

Conversion Time.(Tc) $=$ Tsamp. $+$ Tcomp. $\qquad \alpha \leqq 1/f_{CKI}$

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① Data Writing

BIT2/I0, BIT3/I1 and BIT4/I2 go to on input mode according to the MODE, $\overline{CS}$ and $\overline{WR}$ are low. Channel select (CHS) and output control (BUSC, OUTC) can be set. I0, I1 and I2 become the input for the CHS, BUSC and OUTC signals respectively.

● Input mode setting (MODE)

MODE="L" : BIT2/I0 goes to an input mode and sets channel select (CHS). When MODE is "H" level, BIT2/I0, BIT3/I1, BIT4/I2 are set to the input mode and set the channel select (CHS) and output control.

● Channel Select (CHS)

When CHS is "L" level, VIN0 is selected.
When CHS is "H" level, VIN1 is selected.

● Output Control (BUSC, OUTC)

BUSC	OUTC	OUTPUT MODE
L	*1	10BIT Parallel Output
H	L	8BIT Time Sharing Output (At the 2nd Byte : Lower 6Bit = "L")
· H	H	8BIT Time Sharing Output (At the 2nd Byte : Upper 6BIT = "L")

*1 : Don't care.

② Conversion Time (TC)

$\overline{CS}$ and $\overline{WR}$ go low and the sampling of the selected analog input starts at the first raising edge of two signals in about 8/fckI (Sampling Time). Next, the actual conversion period occurs, the analog input level is converted to digital (Conversion period = 13/fckI).
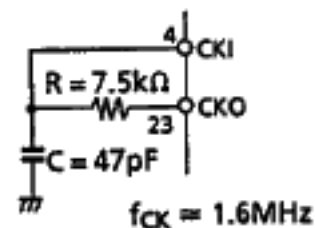
③ Conversion Data output

When $\overline{CS}$ and $\overline{RD}$ are low, conversion data is output from BIT0 to BIT9 according to the setting of the output control.

5.4 CLOCK

The clock input contains an internal oscillation circuit, the frequency of which is controlled by means of an external resistor and capacitor which determine the frequency. An external clock can be input directly to the CKI pin.

$$f_{CK} \simeq \frac{1}{1.8RC}$$

$R = 7.5k\Omega$

$C = 47pF$

$f_{CK} \approx 1.6MHz$

CKI (4)
CKO (23)

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─── **TC35083P/F**

5.5 APPLICATION CIRCUIT of 8-BIT TIME SHARING OUTPUT

① BUSC = "H"
　OUTC = "L"

② BUSC = "H"
　OUTC = "H"

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6. ELECTRICAL CHARACTERISTICS

6.1 MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS} - 0.5$ to $V_{SS} + 7$	V
Input Voltage	V_{IN}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Reference Supply Voltage	V_{REF}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Analog Ground Voltage	A_{GND}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) , 180 (SOP)	mW
Storage Temperature Range	T_{stg}	-65 to 150	°C

6.2 RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0.0V$)

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Input Voltage	V_{IN}		0.0	–	V_{DD}	V
Reference Voltage	V_{REF}	$A_{GND} = 0.0V$	3.0	V_{DD}	V_{DD}	V
Analog Grand Voltage	A_{GND}	$V_{REF} = 5.0V$	0.0	0.0	0.0	V
$V_{REF} - A_{GND}$ Voltage		$V_{DD} = 5.0V \pm 10\%$	3.0	V_{DD}	V_{DD}	V
Clock Frequency	f_{CKI}	$V_{DD} = 5.0V \pm 10\%$	0.4	–	2.0	MHz
Minimum Clock Pulse Width	t_w	$V_{DD} = 5.0V \pm 10\%$	0.2	–	–	μs
Operation Temperature	T_{opr}	$V_{DD} = 5.0V \pm 10\%$	-40	–	85	°C

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6.3. DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ± 10%, V_{SS} = 0.0V)

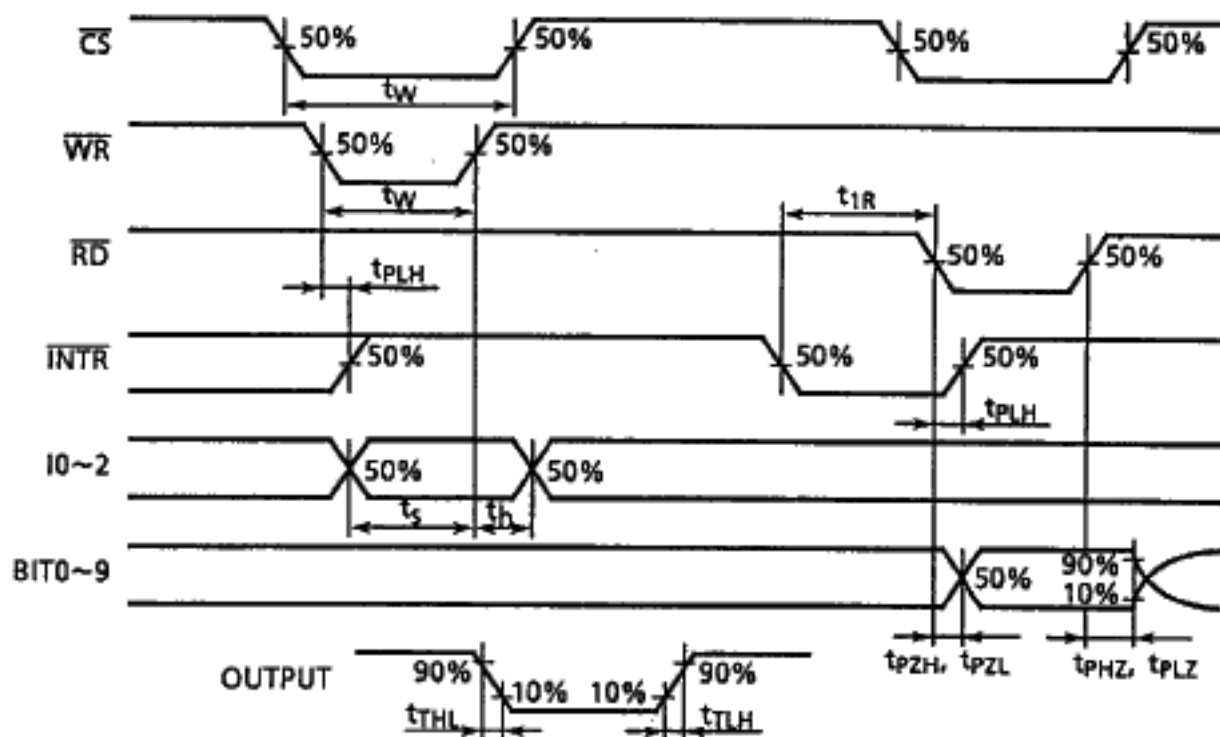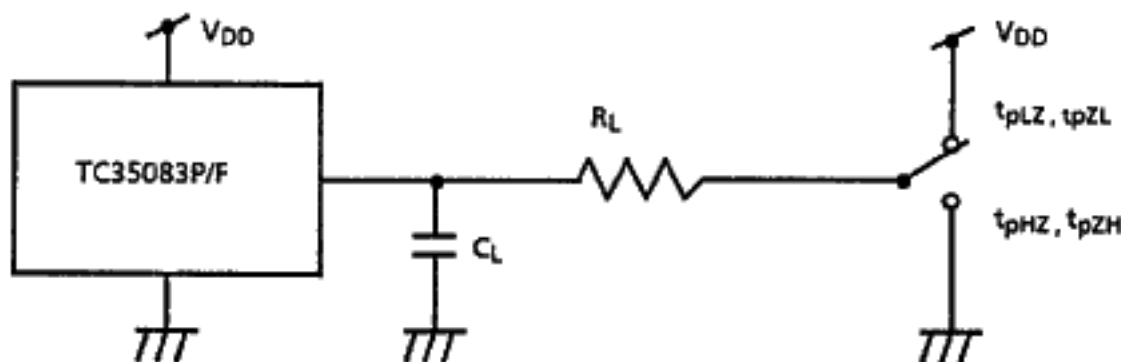| CHARACTERISTIC		SYMBOL	CONDITION	Ta = 25°C			Ta = −40 to 85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Voltage	"H" level	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	$V_{DD} - 0.05$		−	$V_{DD} - 0.05$	−	V
	"L" level	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	−	0.0	0.05	−	0.05	
Output Current	"H" level	I_{OH}	$V_{OH} = V_{DD} - 0.4V$ $V_{IN} = V_{SS}, V_{DD}$	-0.44	−	−	-0.36	−	mA
	"L" level	I_{OL}	$V_{OL} = 0.4V$ $V_{IH} = V_{SS}, V_{DD}$	2.0	−	−	1.6	−	
Input Voltage	"H" level	V_{IH}		2.0	−	−	2.0	−	V
			CIK Terminal, $V_{DD} = 5.0V$	4.5	−	−	4.5	−	
	"L" level	V_{IL}		−	−	0.8	−	0.8	
			CIK Terminal, $V_{DD} = 5.0V$	−	−	0.5	−	0.5	
3-State Disable Current		I_{DH} I_{DL}	$V_{OH} = V_{DD}$, $V_{OL} = V_{SS}$	−	−	± 1.0	−	± 10	
Digital Input Current		I_{IH} I_{IL}	$V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	−	−	± 1.0	−	± 10	μA
On Channel Input Current		I_{ON}	$V_{IN} = V_{SS}, V_{DD}$ Sampling Cycle = 12.5μs	−	−	± 25	−	± 28	
Off Channel Input Current		I_{OFF}	$V_{IN} = V_{SS}, V_{DD}$			± 0.5		± 5	
Operating Consumption Current		I_{DD}	Sampling Cycle = 12.5μs	−	−	6.0	−	7.0	mA
Quiescent Supply Current		I_{DDS}	$CKI = V_{SS}, V_{DD}$ $\overline{CS} = V_{SS}, \overline{WR} = V_{SS}$	−	−	10	−	100	μA
Reference Resistor		R_{Ref}		1.9	3.2	4.3	1.6	4.8	$k\Omega$

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6.4 SWITCHING CHARACTERISTICS (V_{DD} = 5.0V ± 10%, V_{SS} = 0.0V, Ta = -40~85°C)

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Rise/Fall Time	t_{TLH} t_{THL}	C_L = 50pF	–	–	100	ns
Propagation Delay Time	t_{PLH} t_{PHL}	C_L = 50pF	–		450	ns
3-State Output Enable Time	t_{PZH} t_{PZL}	C_L = 50pF R_L = 1KΩ	–		150	ns
3-State Output Disable Time	t_{PHZ} t_{PLZ}	C_L = 50pF R_L = 1KΩ	–		250	ns
Minimum Pulse Width	$t_w(L)$		–		100	ns
Minimum Set-up Time	t_s		–		100	ns
Minimum Hold Time	t_h		–		100	ns
1st Read	t_{1R}		500		–	ns
Input Capacitance	C_{IN1}	Digital Input	–	5	–	pF
	C_{IN2}	Analog Input (ON)	–	70	100	pF
	C_{IN3}	Analog Input (OFF)	–	5	–	pF
Output Capacitance	C_{OUT}	3-State Output	–	10	–	pF

6.4.1 SWITCHING CHARACTERISTIC TEST WAVE FORMS

6.4.2 3-STATE OUTPUT TEST CIRCUIT

6.5 SYSTEM CHARACTERISTICS (Ta = -40 to 85°C)

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Point Error	E_{ZR}	$V_{DD} = 5.0V$	–	± 1/4	± 1	LSB
Full Scale Error	E_{FS}	$V_{REF} = 5.000V$	–	± 1/4	± 1	LSB
Nonlinearity	E_{LI}	$f_{CKI} = 2.0MHz$	–	± 1/2	–	LSB
Total Error	E_T		–	± 3/4	± 1.5	LSB
Conversion Time	T_C	$f_{CKI} = 2.0MHz$	–	11	–	μs