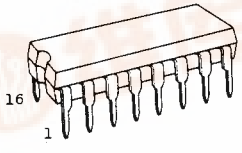
TC40102BP, TC40103BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40102BP 8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTER (2-Decade BCD Type)

TC40103BP 8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTER (8-Bit Bynary Type)

The TC40102BP and TC40103BP are 8-stage presettable synchronous down counters. Output terminal $\overline{CO/ZD}$ is placed in active mode at "L" level when the contents of count become zero.
As the TC40102BP adopts BCD binary coded decimal notation, setting up to 99 counts is possible. The TC40103BP, with 8-bit binary construction, can set up to 255 counts. Each type has $\overline{CI/CE}$ inhibiting clock, $\overline{APE}$ asynchronous preset control input, $\overline{SPE}$ synchronous preset control input and $\overline{RESET}$ control input setting counter to maximum counting mode.
Clock input, with Schmitt function, can accept clock waveform with slow rise and fall edge.

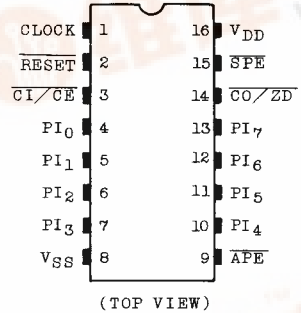


DIP 16(3D16A-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



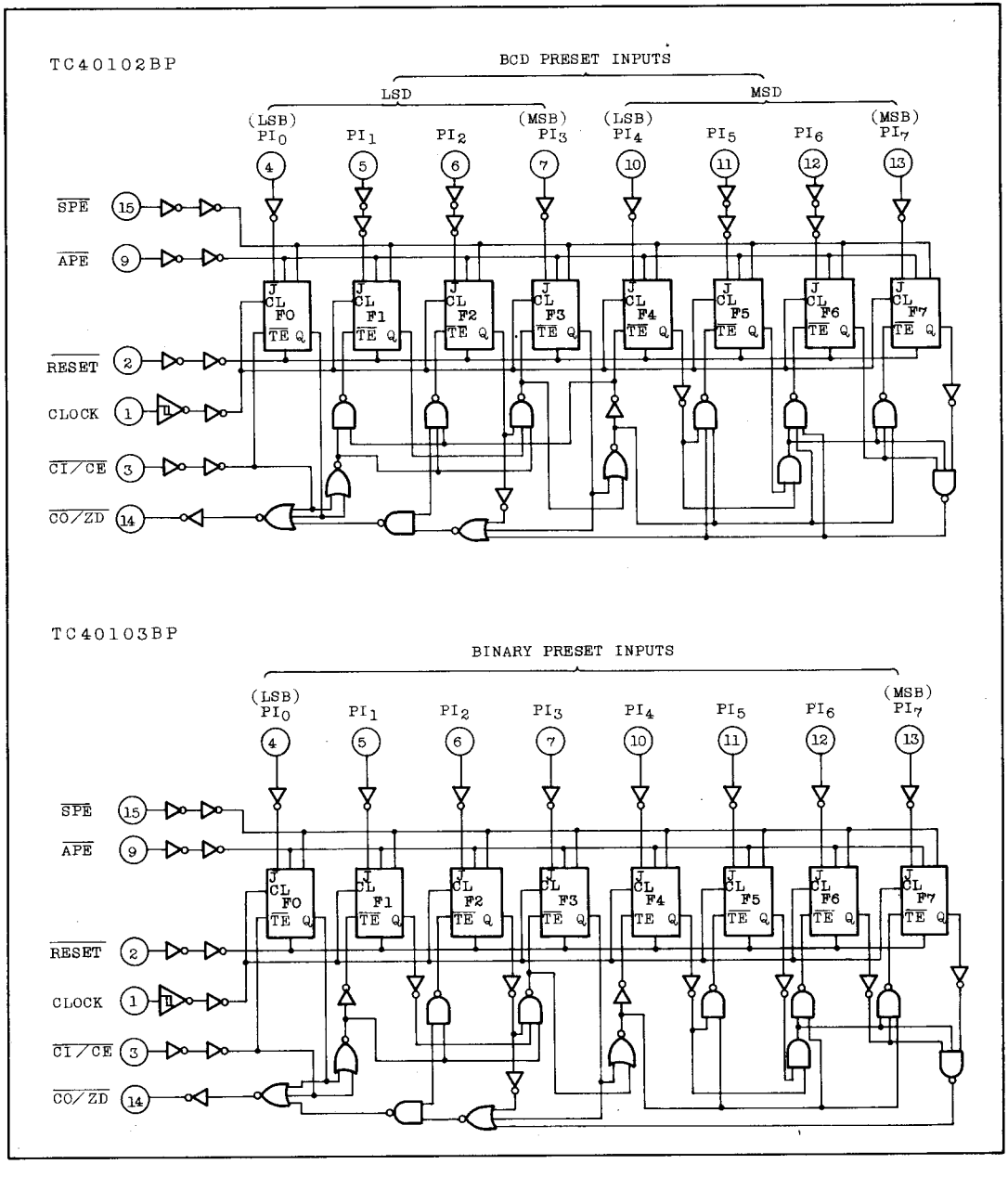
(TOP VIEW)

TRUTH TABLE

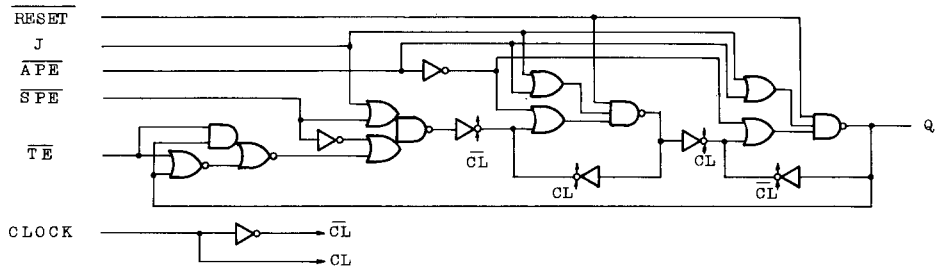
CONTROL INPUT				MODE	FUNCTIONAL DESCRIPTION
$\overline{RESET}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	Count inhibit	Even if clock is given, no count is made.
H	H	H	L	Regular count	Down count at rising edge of clock.
H	H	L	*	Synchronous preset	Data of PI terminal is preset at rising edge of clock.
H	L	*	*	Asynchronous preset	Data of PI terminal is asynchronously preset to clock.
L	*	*	*	Clear	Counter is set to maximum count.

Note 1. * : Don't care
2. Maximum count: "99" for TC40102BP and "255" for TC40103BP.

LOGIC DIAGRAM



INTERNAL FLIP-FLOP (F0 ~ F7) CIRCUIT DIAGRAM AND TRUTH TABLE OF COUNTER



INTERNAL FLIP-FLOP TRUTH TABLE

INPUT						OUTPUT
RESET	APE	SPE	J	TE	CLOCK	Q_n+1
L	※	※	※	※	※	H
H	L	※	L	※	※	H
H	L	※	H	※	※	L
H	H	L	L	※	↓	H
H	H	L	H	※	↓	L
H	H	L	※	※	↑	Q_n
H	H	H	※	L	↓	$\overline{Q_n}$
H	H	H	※	H	※	Q_n

FUNCTIONAL DESCRIPTION

The TC40102BP and TC40103BP are 8-stage presettable synchronous down counters. Carry Out/Zero Deffect ($\overline{CO/ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". The TC40102BP adopts binary coded decimal notation, making setting up to 99 counts possible. While the TC40103BP adopts 8-bit binary counter and can set up to 255 counts.

COUNT OPERATION

At the "H" level of control input of $\overline{RESET}$, $\overline{SPE}$ and $\overline{APE}$, the counter carries out down count operation one by one at the rise of pulse given to CLOCK input. Count operation can be inhibited by setting Carry Input/Clock Enable ($\overline{CI/CE}$) to the "H" level. $\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0", but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.

Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

FUNCTION DESCRIPTION (Cont'd)

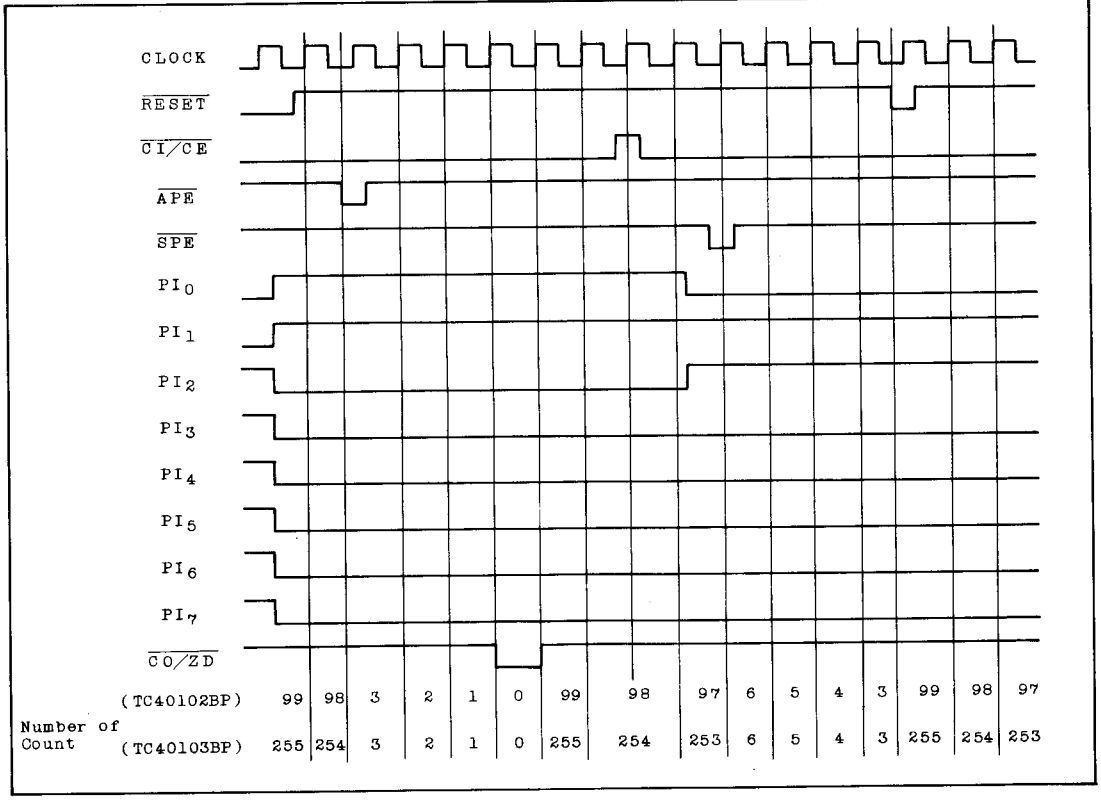
The contents of count jump to maximum count (99 for the TC40102BP and 255 for the TC40103BP) if clock is given when the readout is "0". Therefore, operation of 100-frequency division and that of 256-frequency division are carried out for the TC40102BP and TC40103BP, respectively, when clock input alone is given without various kinds of preset operations. To clock input is attached Schmitt gate.

PRESET OPERATION AND RESET OPERATION

When Reset ($\overline{\text{RESET}}$) input is set to the "L" level, the readout is set to the maximum count independently of other inputs. When Asynchronous Preset Enable ($\overline{\text{APE}}$) input is set to the "L" level, readouts given on P.10 to P.17 can be preset asynchronously to counter independently of inputs other than $\overline{\text{RESET}}$ input. When Synchronous Preset Enable ($\overline{\text{SPE}}$) is set to the "L" level, the readouts given on P.10 to P.17 can be preset to counter synchronously with the rise of clock.

As to these operation modes, refer to the truth table.

TIMING CHART



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
				10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
				10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

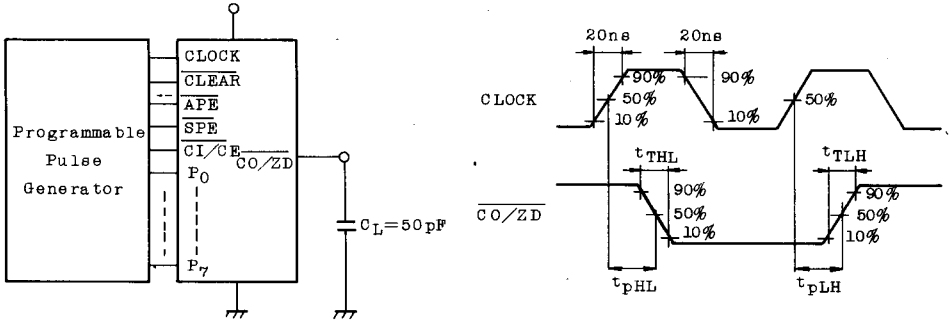
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		5	-	400	600	ns
			10	-	150	260	
			15	-	110	190	
Propagation Delay Time ($\overline{CI/CE}$ - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		5	-	200	400	ns
			10	-	90	180	
			15	-	65	130	
Propagation Delay Time ($\overline{APE}$ - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		5	-	350	1300	ns
			10	-	130	600	
			15	-	100	400	
Propagation Delay Time ($\overline{RESET}$ - $\overline{CO/ZD}$)	t_{pLH}		5	-	300	750	ns
			10	-	120	360	
			15	-	90	200	
Min. Clock Pulse Width	t_w		5	-	100	300	ns
			10	-	40	180	
			15	-	30	80	
Min. Pulse Width ($\overline{RESET}$)	t_{WL}		5	-	140	320	ns
			10	-	60	160	
			15	-	45	100	

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

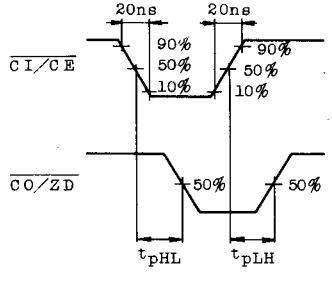
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Min. Pulse Width ($\overline{APE}$)	t_{WL}		5	-	120	360	ns
			10	-	45	160	
			15	-	35	120	
Max. Clock Frequency	f_{CL}		5	0.7	2	-	MHz
			10	1.8	5	-	
			15	2.4	8	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	t_{rCL} t_{fCL}		5	No Limit			μs
			10				
			15				
Min. Set-up Time ($\overline{SPE}$ - CLOCK)	t_{SU}		5	-	120	280	ns
			10	-	75	140	
			15	-	70	100	
Min. Set-up Time (PI - CLOCK)	t_{SU}		5	-	30	100	ns
			10	-	10	50	
			15	-	5	40	
Min. Set-up Time ($\overline{CI/CE}$ - CLOCK)	t_{SU}		5	-	300	500	ns
			10	-	100	250	
			15	-	70	150	
Min. Set-up Time (PI - $\overline{APE}$)	t_{SU}		5	-	150	300	ns
			10	-	60	120	
			15	-	40	80	
Min. Removal Time ($\overline{APE}$-CLOCK)	t_{rem}		5	-	15	220	ns
			10	-	10	100	
			15	-	5	70	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

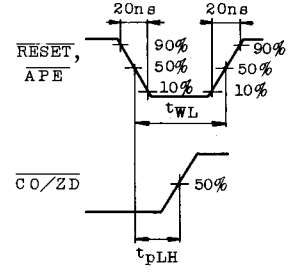
WAVEFORM 1



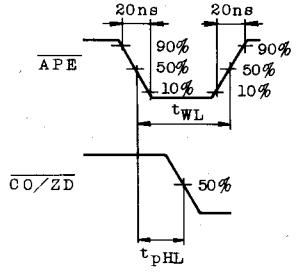
WAVEFORM 2



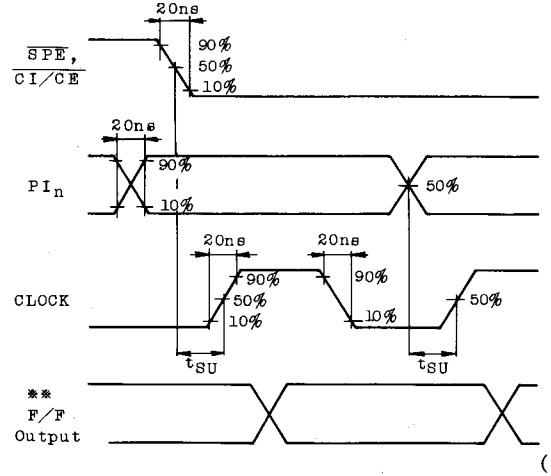
WAVEFORM 3



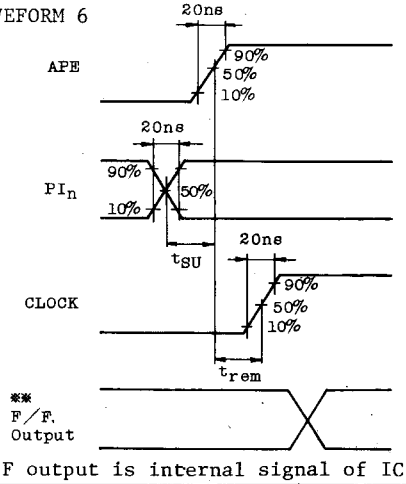
WAVEFORM 4



WAVEFORM 5



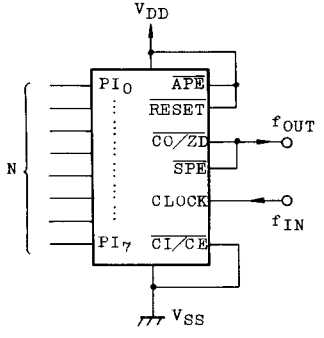
WAVEFORM 6



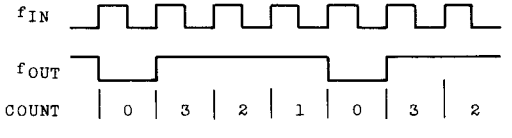
(** F/F output is internal signal of IC.)

APPLICATION CIRCUIT

PROGRAMMABLE DIVIDE-BY-N COUNTER

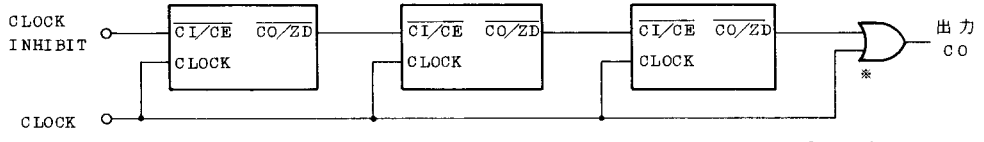


- $f_{OUT} = \frac{f_{IN}}{N+1}$
- Timing chart when N="3" (PIO, PI1=V_{DD}, PI2 ~ PI7=V_{SS})



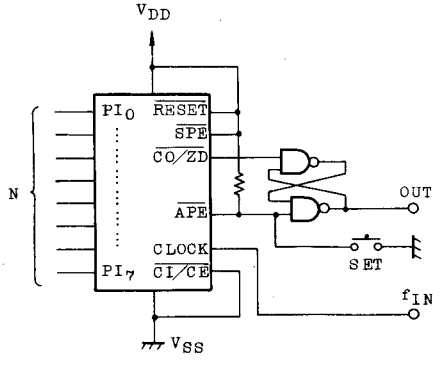
- TC40102BP...1/2 to 1/100 are dividable.
- TC40103BP...1/2 to 1/256 are dividable.

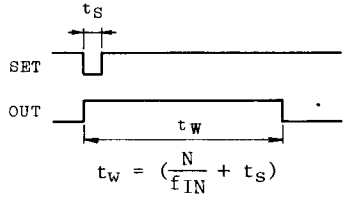
PARALLEL CARRY CASCADING



※ At synchronous cascade connection, buzzard occurs at CO output after its second stage when digit place changes, due to delay arrival. Therefore, take gate from TC4071BP or the like, not from CO output at the rear stage directly.

PROGRAMMABLE TIMER





$$t_W = \left(\frac{N}{f_{IN}} + t_S\right)$$

Note: The above formula does not take into account the phase of clock input. Therefore, the real pulse width is the distance between the above formula-$1/f_{IN}$~ the above formula.