TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

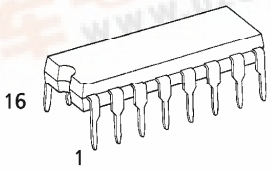
TC4020BP, TC4020BF, TC4020BFN

TC4020B 14 STAGE RIPPLE – CARRY BINARY COUNTER / DIVIDERS

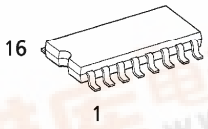
(Note) The JEDEC SOP (FN) is not available in Japan.

TC4020B is 14 stage ripple carry binary counter having asynchronous clear function. The counter advances its counting stage by falling edge of $\overline{CLOCK}$ input. When RESET input is placed "H", all the circuits are reset regardless of $\overline{CLOCK}$ input making all the outputs (Q1, Q4 ~ Q14) to be "L".

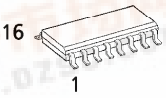
This is most suitable for frequency dividers, control circuits and timing circuits.



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

MAXIMUM RATINGS

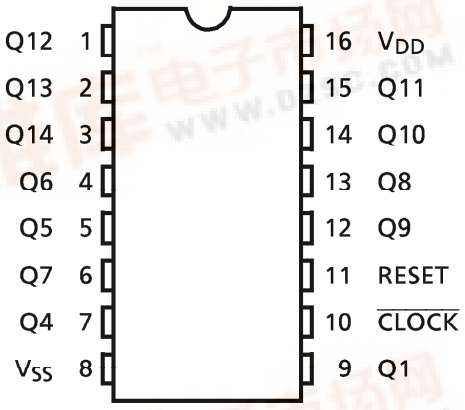
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T_{opr}	– 40~85	°C
Storage Temperature Range	T_{stg}	– 65~150	°C

TRUTH TABLE

$\overline{CLOCK}$△	RESET	OUTPUT STATE
*	H	ALL OUTPUTS = "L"
⌐	L	NO CHANGE
⌐	L	ADVANCE TO NEXT STATE

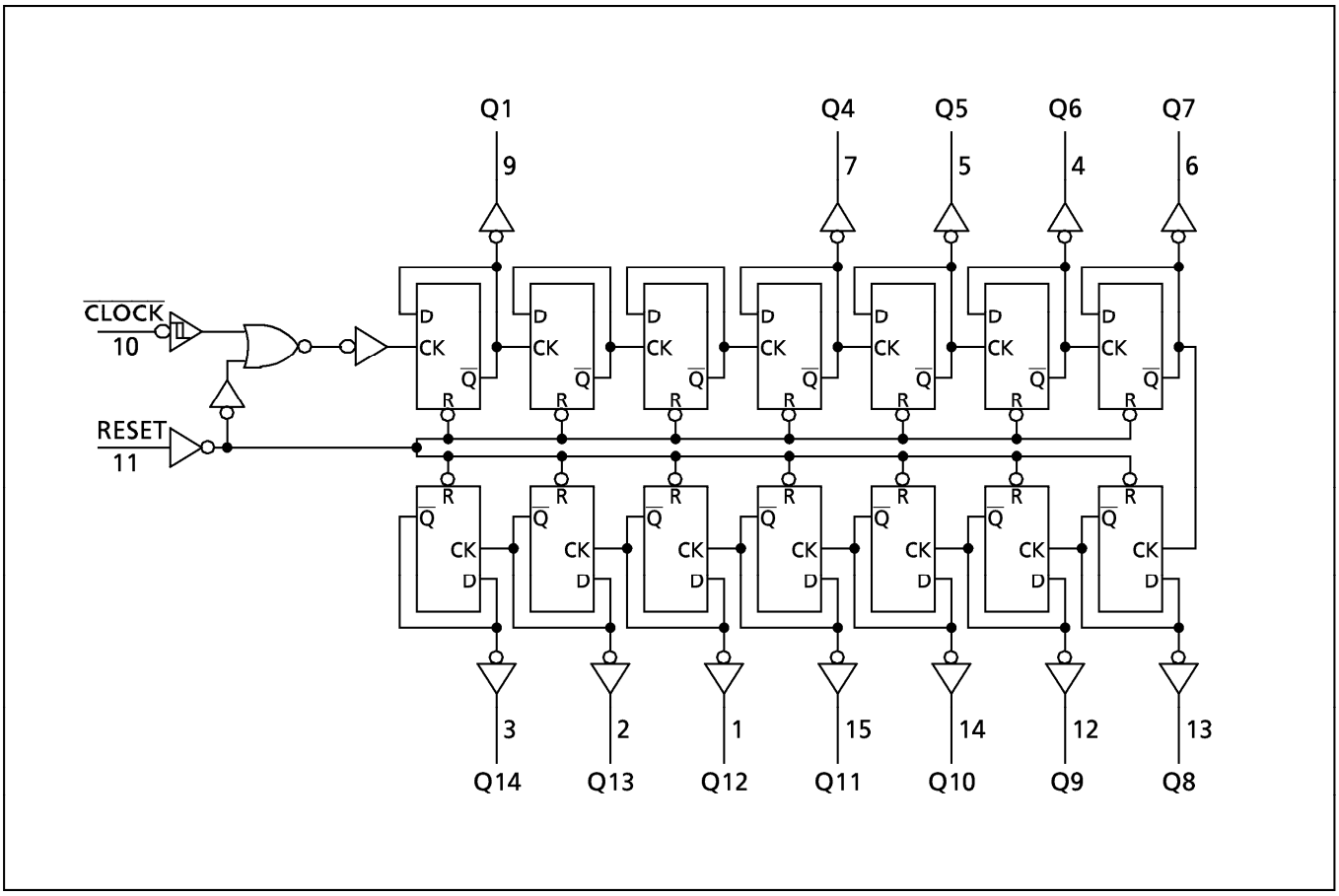
△ : Level Change * : Don't Care

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	—	18	V
Input Voltage	V_{IN}		0	—	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	−40°C MIN.	−40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$	5	4.95	—	4.95	5.00	—	4.95	—	V
		$V_{IN} = V_{SS}, V_{DD}$	10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$	5	—	0.05	—	0.00	0.05	—	0.05	
		$V_{IN} = V_{SS}, V_{DD}$	10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	
Output High Current	I_{OH}	V_{OH} = 4.6V	5	−0.61	—	−0.51	−1.0	—	−0.42	—	mA
		V_{OH} = 2.5V	5	−2.50	—	−2.10	−4.0	—	−1.70	—	
		V_{OH} = 9.5V	10	−1.50	—	−1.30	−2.2	—	−1.10	—	
		V_{OH} = 13.5V	15	−4.00	—	−3.40	−9.0	—	−2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Output Low Current	I_{OL}	V_{OL} = 0.4V	5	0.61	—	0.51	1.2	—	0.42	—	
		V_{OL} = 0.5V	10	1.50	—	1.30	3.2	—	1.10	—	
		V_{OL} = 1.5V	15	4.00	—	3.40	12.0	—	2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT} = 0.5V, 4.5V	5	3.5	—	3.5	2.75	—	3.5	—	V
		V_{OUT} = 1.0V, 9.0V	10	7.0	—	7.0	5.50	—	7.0	—	
		V_{OUT} = 1.5V, 13.5V	15	11.0	—	11.0	8.25	—	11.0	—	
		$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT} = 0.5V, 4.5V	5	—	1.5	—	2.25	1.5	—	1.5	
		V_{OUT} = 1.0V, 9.0V	10	—	3.0	—	4.50	3.0	—	3.0	
		V_{OUT} = 1.5V, 13.5V	15	—	4.0	—	6.75	4.0	—	4.0	
		$\|I_{OUT}\| < 1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH} = 18V	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL} = 0V	18	—	−0.1	—	-10^{-5}	−0.1	—	−1.0	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ *	5	—	5	—	0.005	5	—	150	
			10	—	10	—	0.010	10	—	300	
			15	—	20	—	0.015	20	—	600	

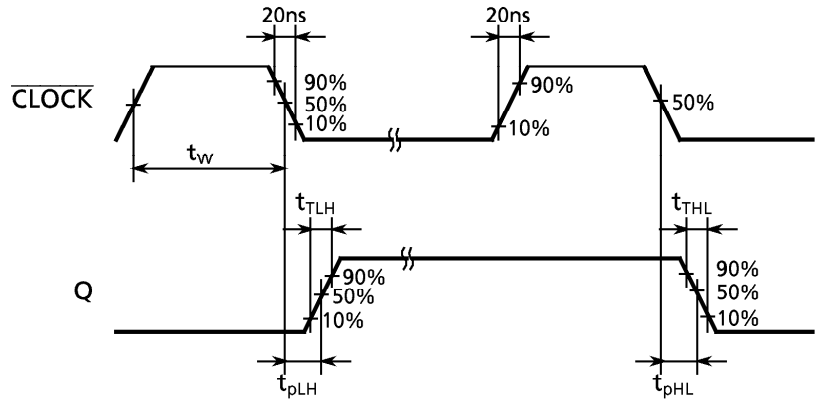
* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, C_L = 50pF)

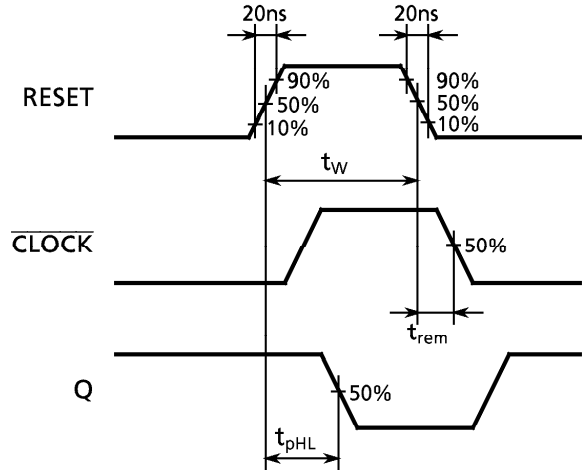
CHARACTERISTIC	SYMBOL	TEST CONDITION V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}	5	—	70	200	ns
		10	—	35	100	
		15	—	30	80	
Output Transition Time (High to Low)	t_{THL}	5	—	70	200	
		10	—	35	100	
		15	—	30	80	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pLH}	5	—	160	360	
		10	—	80	160	
		15	—	65	130	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pHL}	5	—	160	360	
		10	—	80	160	
		15	—	65	130	
Propagation Delay Time ($\overline{CLOCK}$ - Q14)	t_{pLH}	5	—	1000	2000	
		10	—	500	1000	
		15	—	400	800	
Propagation Delay Time ($\overline{CLOCK}$ - Q14)	t_{pHL}	5	—	1000	2000	
		10	—	500	1000	
		15	—	400	800	
Propagation Delay Time (RESET - Q)	t_{pHL}	5	—	150	280	
		10	—	70	120	
		15	—	50	100	
Max. Clock Frequency	f_{CL}	5	3.5	10	—	MHz
		10	8.0	20	—	
		15	12.0	25	—	
Min. Clock Pulse Width (RESET)	t_W	5	—	50	140	ns
		10	—	20	60	
		15	—	15	40	
Min. Pulse Width	t_W	5	—	100	200	
		10	—	40	80	
		15	—	30	60	
Min. Removal Time (RESET - $\overline{CLOCK}$)	t_{rem}	5	—	—	350	
		10	—	—	150	
		15	—	—	100	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t_{rCL} t_{fCL}	5 10 15	No Limit			μs
Input Capacitance	C_{IN}		—	5	7.5	pF

OPERATING SUPPLY CURRENT TEST CIRCUIT

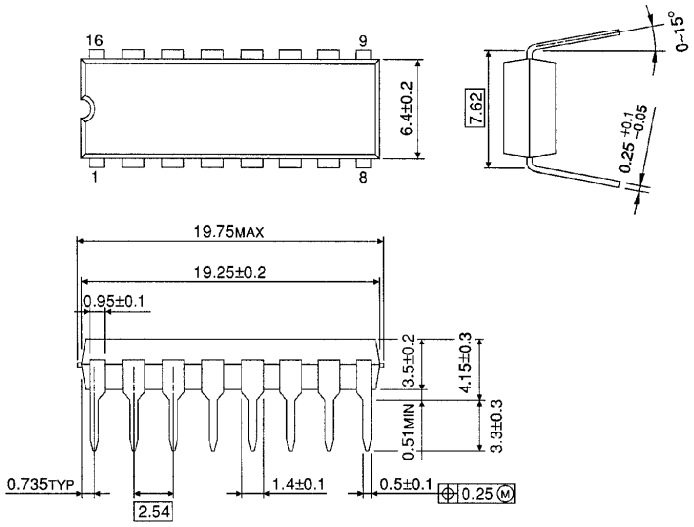
WAVEFORM 1



WAVEFORM 2

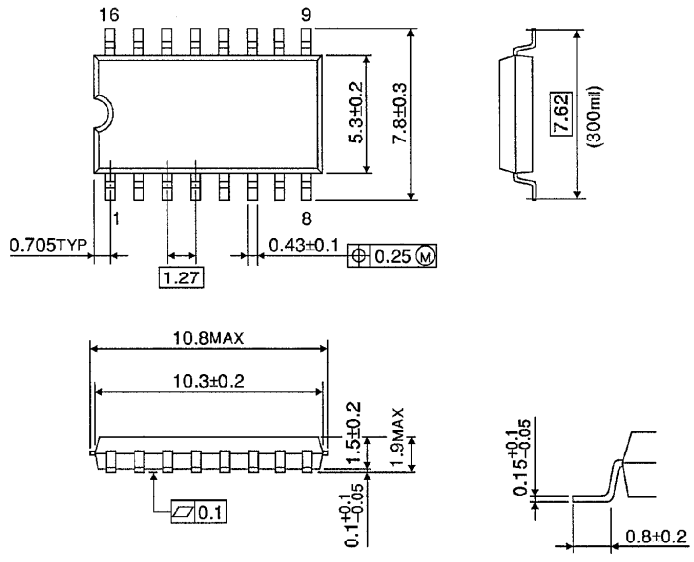


DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

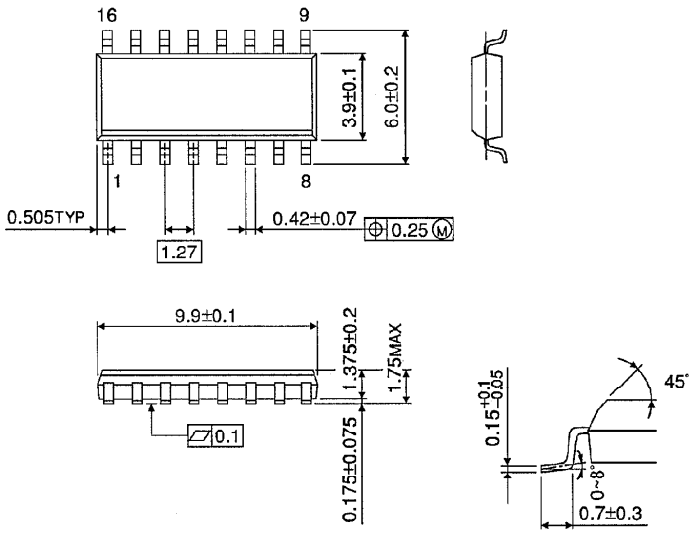
SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)