

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

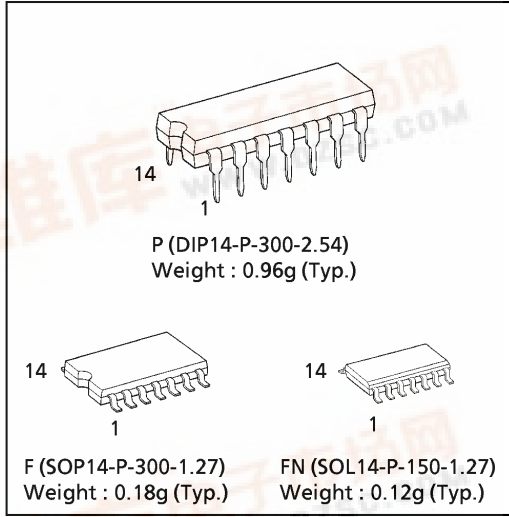
# TC4081BP, TC4081BF, TC4081BFN

(Note) The JEDEC SOP (FN) is not available in Japan.

## TC4081B QUAD 2 INPUT AND GATE

TC4081B is positive logic AND gates with two inputs respectively.

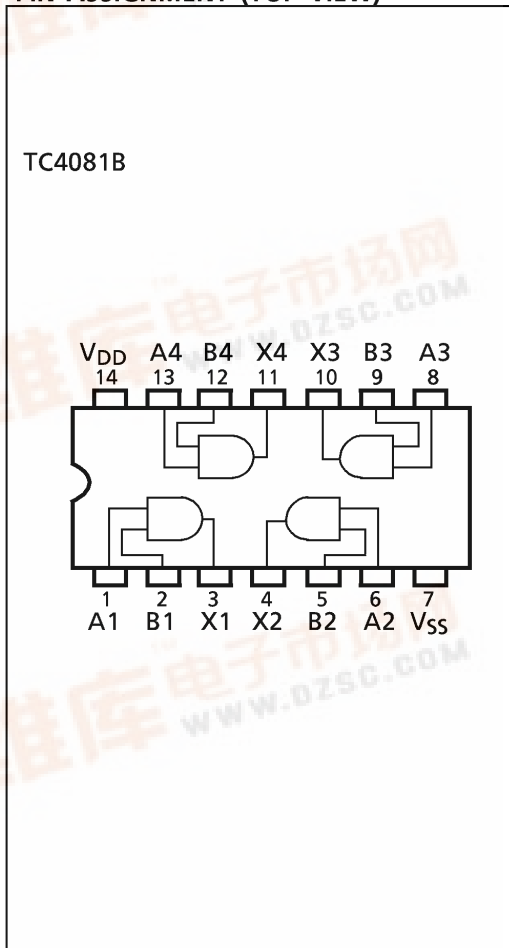
Since all the outputs of these gates are equipped with the buffer circuits of inverters, the input/output propagation characteristic has been improved and variation of propagation time caused by increase of load capacity is kept minimum.



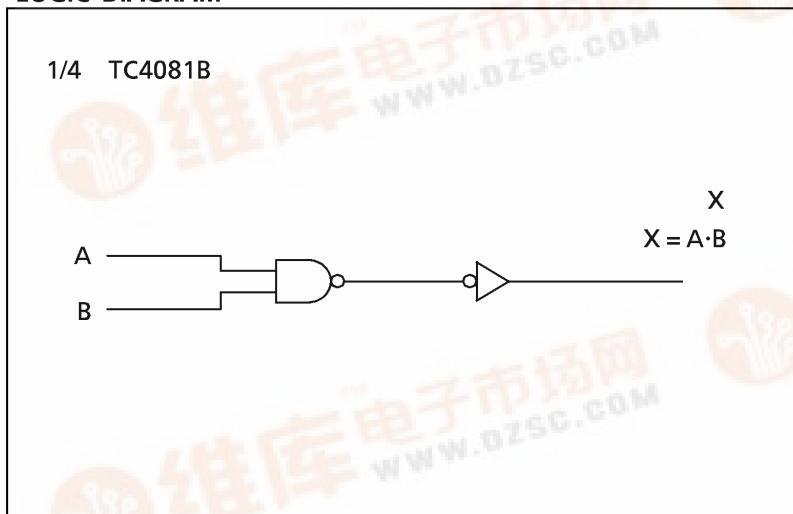
## MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	$V_{DD}$	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	$V_{IN}$	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	$V_{OUT}$	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	$I_{IN}$	$\pm 10$	mA
Power Dissipation	$P_D$	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	$T_{Ope}$	-40~85	°C
Storage Temperature Range	$T_{stg}$	-65~150	°C

## PIN ASSIGNMENT (TOP VIEW)



## LOGIC DIAGRAM



980910EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.



**RECOMMENDED OPERATING CONDITIONS (V<sub>SS</sub> = 0V)**

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V <sub>DD</sub>		3	—	18	V
Input Voltage	V <sub>IN</sub>		0	—	V <sub>DD</sub>	V

**STATIC ELECTRICAL CHARACTERISTICS (V<sub>SS</sub> = 0V)**

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V <sub>DD</sub> (V)	- 40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V <sub>OH</sub>	I <sub>OUT</sub>   < 1μA V <sub>IN</sub> = V <sub>SS</sub> , V <sub>DD</sub>	5	4.95	—	4.95	5.00	—	4.95	—	V
			10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-Level Output Voltage	V <sub>OL</sub>	I <sub>OUT</sub>   < 1μA V <sub>IN</sub> = V <sub>SS</sub> , V <sub>DD</sub>	5	—	0.05	—	0.00	0.05	—	0.05	V
			10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> = 4.6V V <sub>OH</sub> = 2.5V V <sub>OH</sub> = 9.5V V <sub>OH</sub> = 13.5V V <sub>IN</sub> = V <sub>DD</sub>	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA
			5	-2.50	—	-2.10	-4.0	—	-1.70	—	
			10	-1.50	—	-1.30	-2.2	—	-1.10	—	
			15	-4.00	—	-3.40	-9.0	—	-2.80	—	
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> = 0.4V V <sub>OL</sub> = 0.5V V <sub>OL</sub> = 1.5V V <sub>IN</sub> = V <sub>SS</sub> , V <sub>DD</sub>	5	0.61	—	0.51	1.2	—	0.42	—	mA
			10	1.50	—	1.30	3.2	—	1.10	—	
			15	4.00	—	3.40	12.0	—	2.80	—	
			—	—	—	—	—	—	—	—	
Input High Voltage	V <sub>IH</sub>	V <sub>OUT</sub> = 0.5V, 4.5V V <sub>OUT</sub> = 1.0V, 9.0V V <sub>OUT</sub> = 1.5V, 13.5V  I <sub>OUT</sub>   < 1μA	5	3.5	—	3.5	2.75	—	3.5	—	V
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11.0	—	11.0	8.25	—	11.0	—	
			—	—	—	—	—	—	—	—	
Input Low Voltage	V <sub>IL</sub>	V <sub>OUT</sub> = 0.5V, 4.5V V <sub>OUT</sub> = 1.0V, 9.0V V <sub>OUT</sub> = 1.5V, 13.5V  I <sub>OUT</sub>   < 1μA	5	—	1.5	—	2.25	1.5	—	1.5	V
			10	—	3.0	—	4.50	3.0	—	3.0	
			15	—	4.0	—	6.75	4.0	—	4.0	
			—	—	—	—	—	—	—	—	
Input Current	"H" Level	I <sub>IH</sub>	V <sub>IH</sub> = 18V	18	—	0.1	—	10 <sup>-5</sup>	0.1	—	μA
	"L" Level	I <sub>IL</sub>	V <sub>IL</sub> = 0V	18	—	-0.1	—	-10 <sup>-5</sup>	-0.1	—	
Quiescent Supply Current	I <sub>DD</sub>	V <sub>IN</sub> = V <sub>SS</sub> , V <sub>DD</sub> *	5	—	0.25	—	0.001	0.25	—	7.5	μA
			10	—	0.50	—	0.001	0.50	—	15.0	
			15	—	1.00	—	0.002	1.00	—	30.0	

\* All valid input combinations.

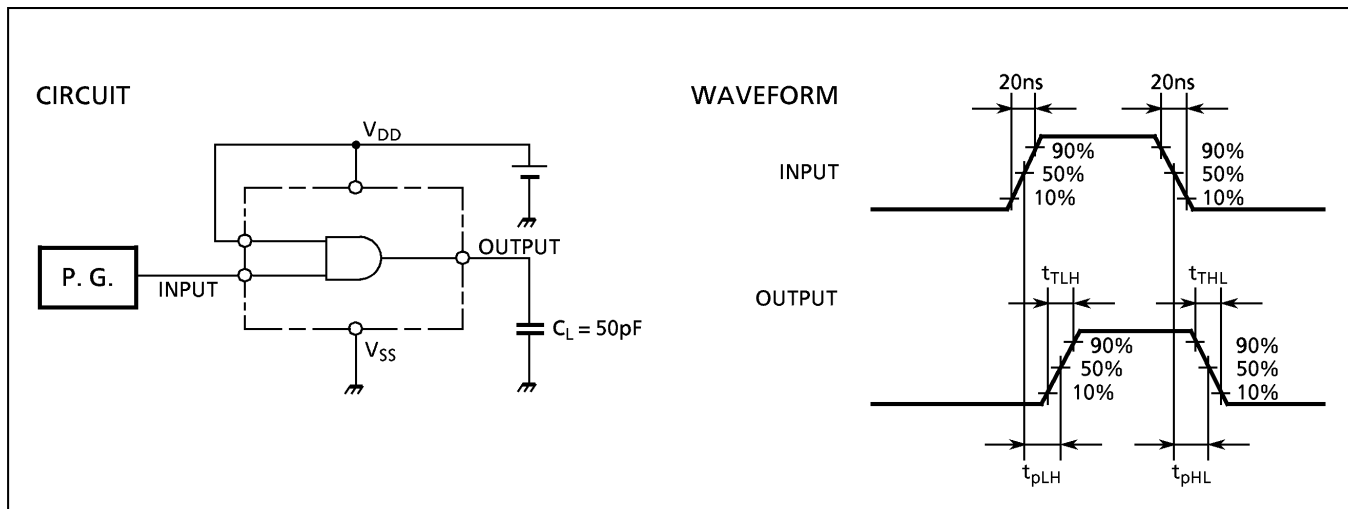
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**DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, CL = 50pF)**

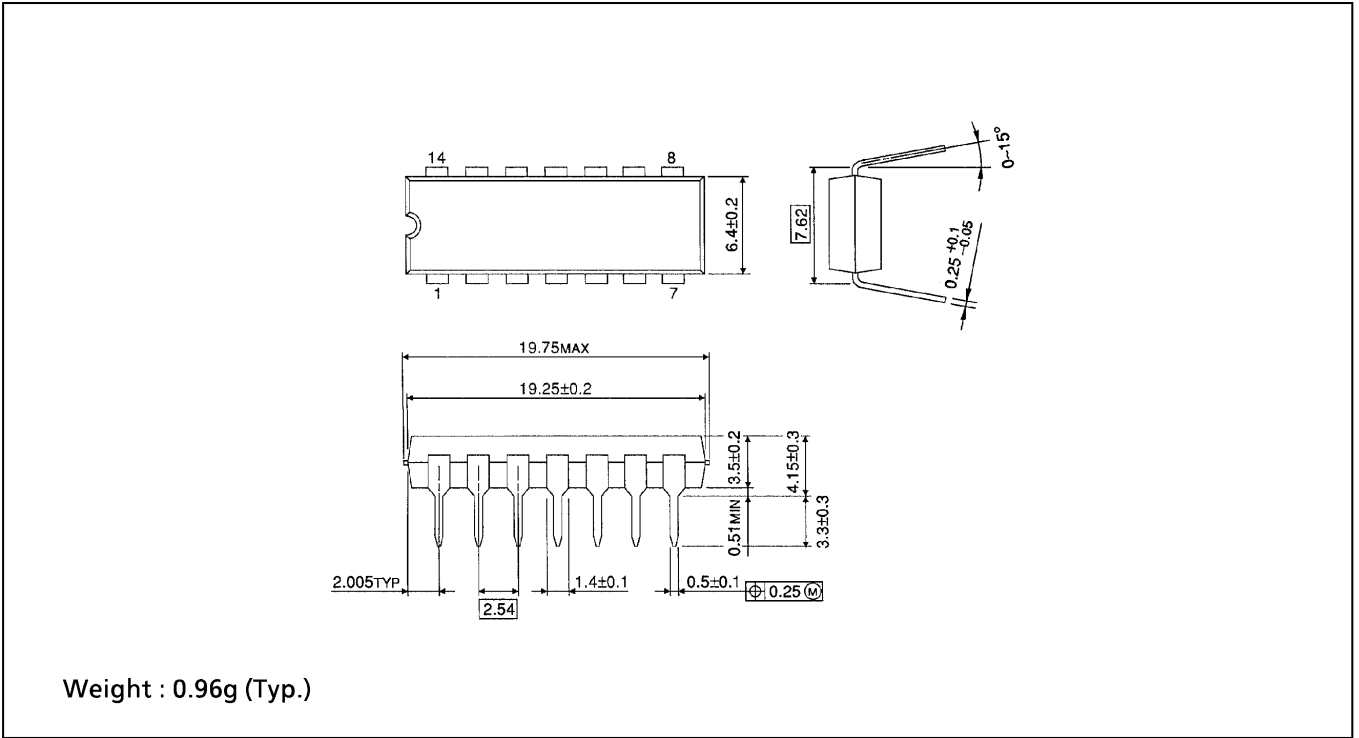
CHARACTERISTIC	SYMBOL	TEST CONDITION	V <sub>DD</sub> (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t <sub>TLH</sub>		5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output Transition Time	t <sub>THL</sub>		5	—	70	200	
			10	—	35	100	
			15	—	30	80	
Propagation Delay Time	t <sub>pLH</sub>		5	—	65	200	
			10	—	30	100	
			15	—	25	80	
Propagation Delay Time	t <sub>pHL</sub>		5	—	65	200	
			10	—	30	100	
			15	—	25	80	
Input Capacitance	C <sub>IN</sub>			—	5	7.5	pF

**CIRCUITS AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS**



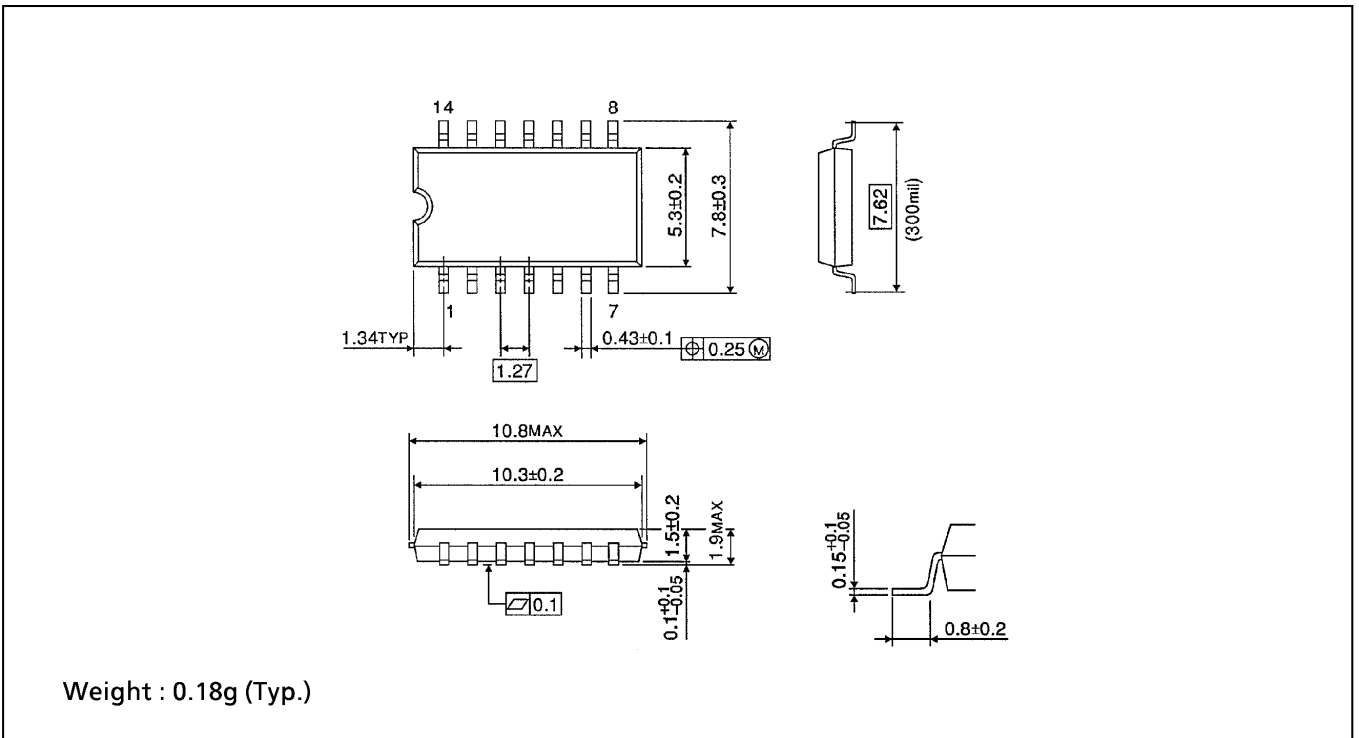
**DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54)**

Unit in mm



**SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)**

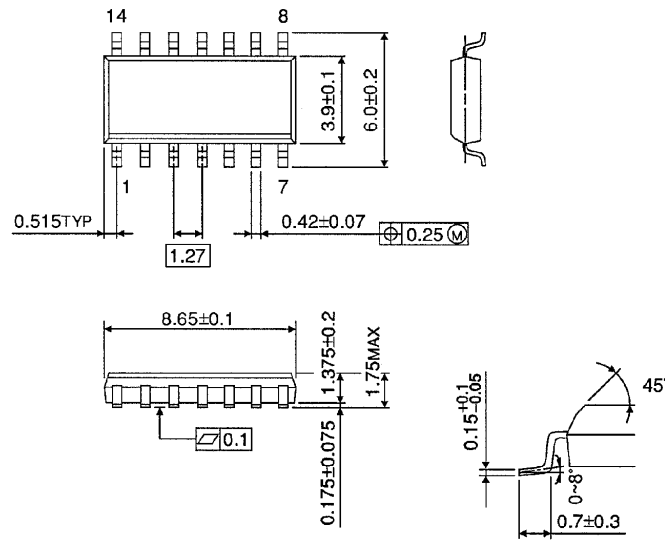
Unit in mm



**SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)