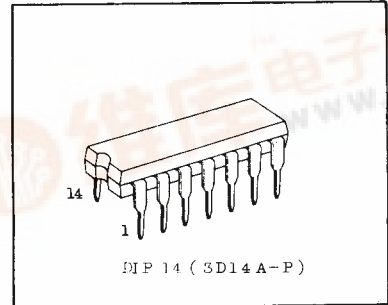


TC5027BP BINARY COUNTER

TC5027BP is four bit binary up counter with the reset function and since the clock for the first stage is independent from the clock for the second through the fourth stages, this can be used as binary, octal or hexadecimal counter/divider.

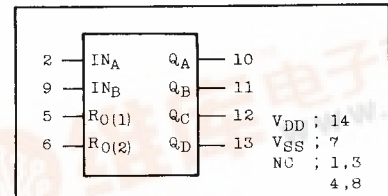
When two inputs of RESET(0) are set to "H", the content of counter is reset to 0 regardless of the clock. The outputs change their states at the falling edge of count inputs (INA, INB).



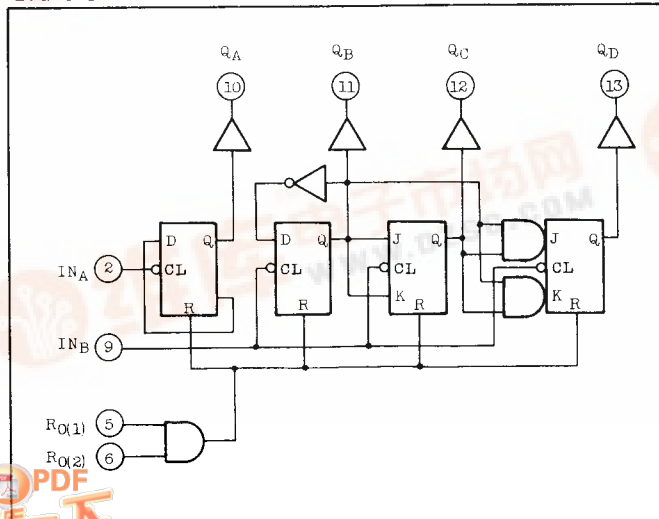
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD}	V _{SS} -0.5 ~ V _{SS} +20	V
Input Voltage	V _{IN}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{SS} -0.5 ~ V _{DD} +0.5	V
DC Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300	mW
Storage Temperature Range	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C · 10sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

RESET / COUNT MODE						
INPUTS				OUTPUT		
IN _A	IN _B	R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B Q _A
*	H	H	H	L	L	L
\overline{L}	L	*	L	COUNT		
\overline{L}	*	L	L	COUNT		
* Don't care						
COUNT MODE A				COUNT MODE B		
COUNT NO.	Q _D	Q _C	Q _B	COUNT NO.	Q _D	Q _C Q _B Q _A
0	L	L	L	0	L	L L L L
1	L	L	H	1	L	L L H H
2	L	H	L	2	L	L H L L
3	L	H	H	3	L	L H H H
4	H	L	L	4	L	H L L L
5	H	L	H	5	L	H L H H
6	H	H	L	6	L	H H L L
7	H	H	H	7	L	H H H H
A : Separate mode.						
B : IN _B should be connected to Q _A .						
				8	H	L L L L
				9	H	L L H H
				10	H	L H L L
				11	H	L H H H
				12	H	H L L L
				13	H	H L H L
				14	H	H H L L
				15	H	H H H H

TC5027BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD}	3	-	18	V
Input Voltage	V _{IN}	0	-	V _{DD}	V
Operating Temp.	Topr	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V _{DD} (V)	-40°C		25°C			85°C		UNIT	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
High Level Output Voltage	V _{OH}	I _{OUT} < 1μA V _{IN} = V _{SS} , V _{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V	
			10	9.95	-	9.95	10.00	-	9.95	-		
			15	14.95	-	14.95	15.00	-	14.95	-		
Low Level Output Voltage	V _{OL}	I _{OUT} < 1μA V _{IN} = V _{SS} , V _{DD}	5	-	0.05	-	0.00	0.05	-	0.05	V	
			10	-	0.05	-	0.00	0.05	-	0.05		
			15	-	0.05	-	0.00	0.05	-	0.05		
High Level Output Current	I _{OH}	V _{OH} = 4.6V V _{OH} = 9.5V V _{OH} = 13.5V V _{IN} = V _{SS} , V _{DD}	5	-0.2	-	-0.16	-	-	-0.12	-	mA	
			10	-0.5	-	-0.4	-	-	-0.3	-		
			15	-1.4	-	-1.2	-	-	-1.0	-		
			5	0.52	-	0.44	-	-	0.36	-		
Low Level Output Current	I _{OL}	V _{OL} = 0.4V V _{OL} = 0.5V V _{OL} = 1.5V V _{IN} = V _{SS} , V _{DD}	5	0.52	-	0.44	-	-	0.36	-	mA	
			10	1.3	-	1.1	-	-	0.9	-		
			15	3.6	-	3.0	-	-	2.4	-		
			5	3.5	-	3.5	2.75	-	3.5	-		
High Level Input Voltage	V _{IH}	V _{OUT} =0.5V, 4.5V V _{OUT} =1.0V, 9.0V V _{OUT} =1.5V, 13.5V I _{OUT} < 1μA	5	3.5	-	3.5	2.75	-	3.5	-	V	
			10	7.0	-	7.0	5.5	-	7.0	-		
			15	11.0	-	11.0	8.25	-	11.0	-		
			5	-	1.5	-	2.25	1.5	-	1.5		
Low Level Input Voltage	V _{IL}	V _{OUT} =0.5V, 4.5V V _{OUT} =1.0V, 9.0V V _{OUT} =1.5V, 13.5V I _{OUT} < 1μA	5	-	1.5	-	2.25	1.5	-	1.5	V	
			10	-	3.0	-	4.5	3.0	-	3.0		
			15	-	4.0	-	6.75	4.0	-	4.0		
			18	-	0.3	-	10 ⁻⁵	0.3	-	1.0		
Input Current	"H" Level	I _{IH}	V _{IH} = 18V	18	-	0.3	-	10 ⁻⁵	0.3	-	1.0	μA
	"L" Level	I _{IL}	V _{IL} = 0V	18	-	-0.3	-	-10 ⁻⁵	-0.3	-	-1.0	
Quiescent Supply Current	I _{DD}	V _{IN} = V _{SS} , V _{DD} *	5	-	20	-	0.005	20	-	150	μA	
			10	-	40	-	0.010	40	-	300		
			15	-	80	-	0.015	80	-	600		

*All valid input combinations

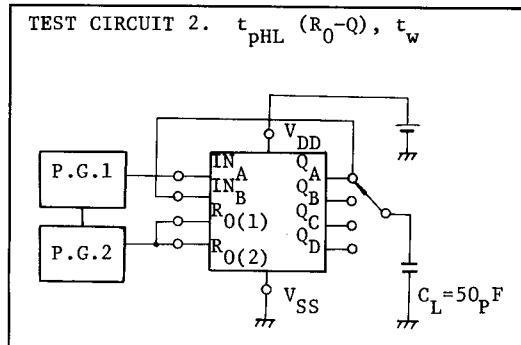
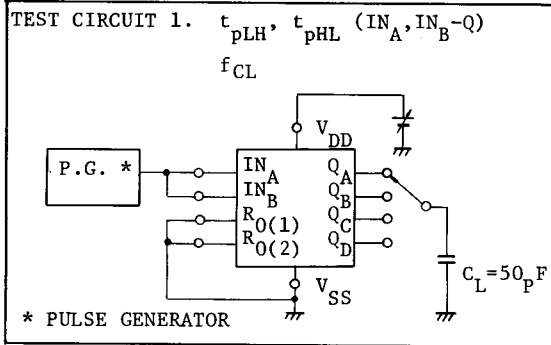
SWITCHING CHARACTERISTICS (T_a=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t _{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Fall Time	t _{THL}		5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	

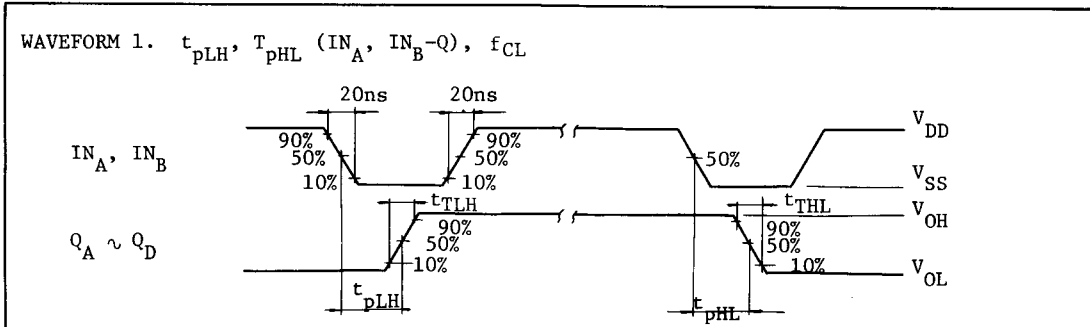
SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50 pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V _{DD}	MIN.	TYP.	MAX.	UNIT
(Low-High) Propagation Delay Time (IN _A , IN _B - Q)	t _{pLH}		5	-	340	750	
			10	-	160	350	
			15	-	130	280	
(High-Low) Propagation Delay Time (IN _A , IN _B - Q)	t _{pHL}		5	-	310	650	ns
			10	-	150	330	
			15	-	120	250	
(High-Low) Propagation Delay Time (R _O - Q)	t _{pHL}		5	-	250	700	ns
			10	-	120	300	
			15	-	100	250	
Max. Clock Rise Time	t _{rCL}		5	20	-	-	μs
Max. Clock Fall Time	t _{fCL}		10	2.5	-	-	
			15	1.0	-	-	
Max. Clock Frequency (IN _A , IN _B)	f _{CL}		5	0.8	1.2	-	MHz
			10	1.5	2.5	-	
			15	2.0	3.2	-	
Min. Reset Pulse Width	t _w (RESET)		5	-	250	500	ns
			10	-	110	200	
			15	-	80	150	
Input Capacitance	C _{IN}		-		5	-	pF

SWITCHING TIME TEST CIRCUITS



SWITCHING TIME TEST WAVEFORMS



TC5027BP

SWITCHING TIME TEST WAVEFORMS

WAVEFORM 2. $t_{pHL} (R_0 - Q)$, t_w ,

