查询TC5043P供应商 捷多邦，专业PCB打样工厂，24小时加急出货

TC5043P PROGRAMMABLE CR TIMER/DIVIDER

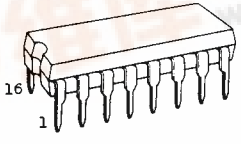
TC5043P is an timer consisting of CR oscillation circuit and frequency division circuit.
The oscillation circuit is made up by externally installing one resistor and one capacitor, being able to be set in a wide range of cycle. The frequency division circuit consists of fixed stage of 1/1000 and variable stage of 1/1 ~ 1/600, being capable of performing frequency division of 6×10^5 max.
Therefore, TC5043P can cover all the regions ranging from conventional CR timers to motor timers.
This device is so designed that the external parts required may be reduced to the minimum by means of the built-in zener diode, auto reset circuit, and pull-up/pull-down resistance.

FEATURES:

- Wide time range of timer (5ms ~ 1500Hr)
- Wide range of fine adjustment of oscillation frequency (±50% or over)
- Low power consumption (2mW ..... Typ.)
- Little supply voltage regulation of oscillation cycle (1%/V)
- Narrow temperature variations of oscillation cycle (0.02%/°C)
- Internal auto reset function
- Precision CR oscillation circuit
- Internal zener diode
- Timer/Divider switchable
- Simple display of time elapsed of oscillation
- Programmable frequency division ratio able to be set in eight ways

APPLICATIONS:

- Industrial timers
- Timers for various commercial equipment
- Low-frequency oscillators



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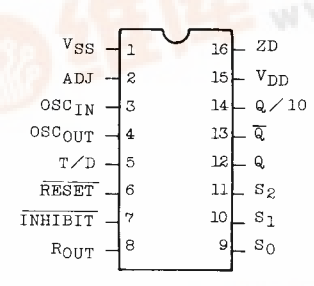
PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	RATING	UNIT
DC Supply Voltage		V_{DD}	V_{SS}-0.5 ~ V_{SS}+12	V
Input Voltage		V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	
Output Voltage	R_{OUT}, Q/10	V_{OUT}	V_{SS}-0.5 ~ V_{SS}+12	
	Q, $\overline{Q}$, OSC_{OUT}		V_{SS}-0.5 ~ V_{DD}+0.5	
DC Input Current		I_{IN}	±10	mA
Zener Current		I_Z	10	
Power Dissipation		P_D	300	mW
Operating Temperature Range		T_{opr}	-40 ~ 85	°C
Storage Temperature Range		T_{stg}	-65 ~ 150	

TRUTH TABLE

$\overline{R}$	T/D	$\overline{INH}$	OPERATION
L	*	*	RESET
H	H	H	TIMER OPERATION
H	L	H	DIVIDER OPERATION
H	*	L	TEMPORARY STOP OF OPERATION

* Don't Care

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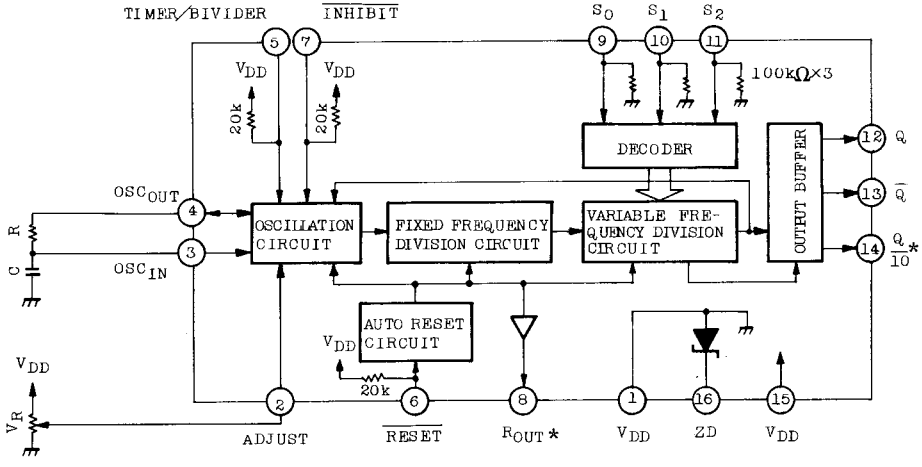
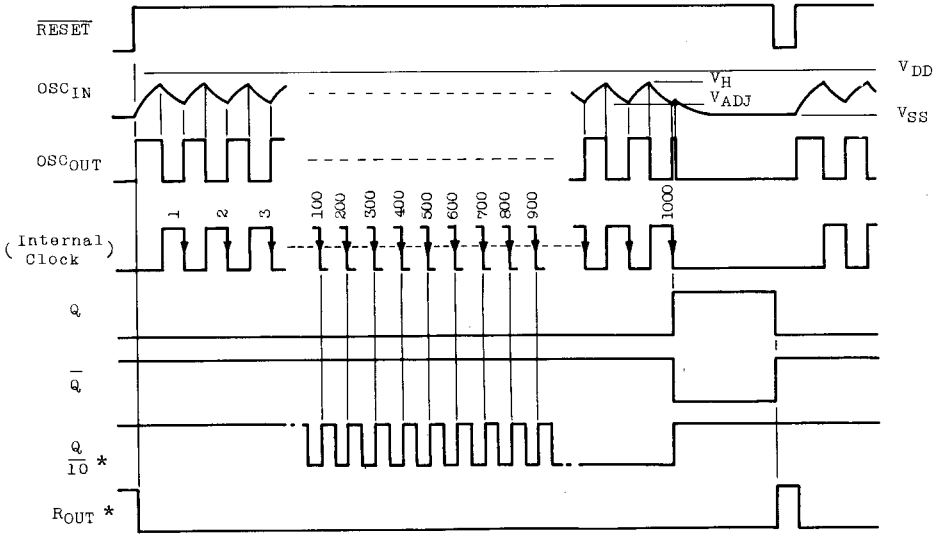
SYSTEM DIAGRAM



· Outputs marked with * are N-channel open drain structure.

TIMING DIAGRAM (1)

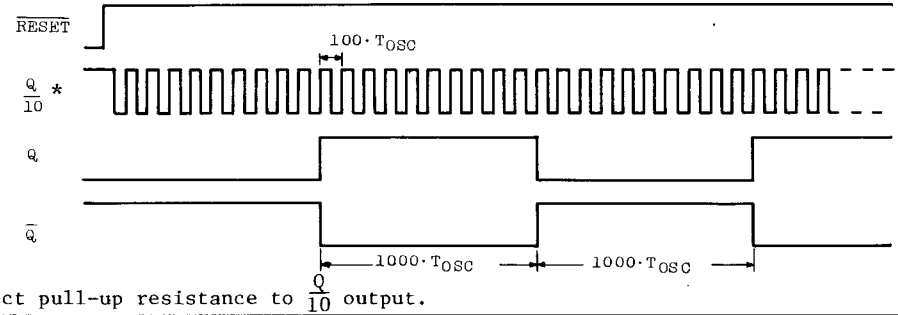
1. Timer operation, Programmable frequency division ratio 1/1
   (T/D="H", $\overline{\text{INHIBIT}}$="H", $S_0=S_1=S_2$="H")



· For outputs marked with *, add pull-up resistance to V_{DD}.

TIMING DIAGRAM

2. Divider operation, Programmable frequency division ratio 1/1
(T/D="L", $\overline{\text{INHIBIT}}$="H", $S_0=S_1=S_2$="L")



* Connect pull-up resistance to $\frac{Q}{10}$ output.

PIN FUNCTION

PIN NO.	SYMBOL	FUNCTION
1	V_{SS}	GND (0V) Pin
2	ADJUST	Pin for fine adjustment for oscillation frequency. Externally apply the voltage ranging from $0.2V_{DD}$ to $0.55V_{DD}$.
3	OSC_{IN}	Oscillation circuit configuration pins : These pins start oscillation when resistor R is connected between OSC_{IN} and OSC_{OUT} and capacitor C between OSC_{IN} and V_{SS}, respectively. In case V_{ADJ} is $0.39V_{DD}$, oscillation cycle becomes almost $T_{OSC}=RC$.
4	OSC_{OUT}	
5	TIMER /DIVIER	Timer/divider switching input. At time of open (or "H" level), this device operates as a timer, and at time of "L" level it operates as a divider.
6	$\overline{\text{RESET}}$	All the counters are reset at "L" level. At the rising edge of this input, the device begins to count.
7	$\overline{\text{INHIBIT}}$	When this pin is set at "L" level, the device keeps stopping oscillation during the period of "L" level state. The pin is used for temporary stop of oscillation.
8	$RESET_{OUT}$	Only at time of timer operation, reset signal is output. (At the time when $\overline{\text{RESET}}$ = "L" and during the period of auto reset at the rising time of power supply, output is off.) For the divider mode, this pin should be open.
9	S_0	$S_0 \sim S_3$ are frequency division ratio switching inputs of the counter. Eight time intervals can be predetermined by combining pins, $S_0 \sim S_2$. ($T = 1000 \times \frac{1}{f_{OSC}}$)

PIN NO.	SYMBOL	FUNCTION
10	S_1	
11	S_2	
12	Q	Q and $\overline{Q}$ are time-up outputs. After the end of time intervals, Q reaches "H" level and $\overline{Q}$ reaches "L" level. While the divider is operating, these outputs oscillate at double the cycle of time range of timer.
13	$\overline{Q}$	
14	$\frac{Q}{10}$	Q/10 is a pin which outputs the elapsed time of timer, and outputs the pulse of 1/10 cycle of timer time. This is N-channel open drain output.
15	V_{DD}	Power supply pin
16	ZD	The cathode terminal of zener diode is put out of this pin. This pin is used as a stabilized power supply by making the connection to V_{DD}.

S_2	L				H			
S_1	L		H		L		H	
S_0	L	H	L	H	L	H	L	H
Time intervals of timer*	T	3T	6T	10T	60T	30T	300T	600T

* In the divider operation mode, the above time intervals of timer become half cycles of Q and $\overline{Q}$.

OPERATIONAL DESCRIPTION

1. Oscillation Circuit

The oscillation circuit can be made up by connecting resistor R between OSC_{IN} and OSC_{OUT} and capacitor C between OSC_{IN} and V_{SS}(GND) as shown in Fig. 1.

This IC has two levels of built-in reference voltage V_H(0.62 V_{DD}) and reference voltage V_L(=V_{ADJ}) externally supplied to ADJ pin, and performs oscillation in such a form as the charge and discharge wave of CR runs between these two levels.

Therefore, oscillation cycle can be adjusted by varying the voltage of ADJ pin.

When $V_{ADJ} \fallingdotseq 0.39\ V_{DD}$, the oscillation cycle is decided from the equation of T_{OSC}=RC (T : [S], R[Ω], C[F]). V_{ADJ} should be used within the range of $0.2V_{DD} \sim 0.55V_{DD}$.

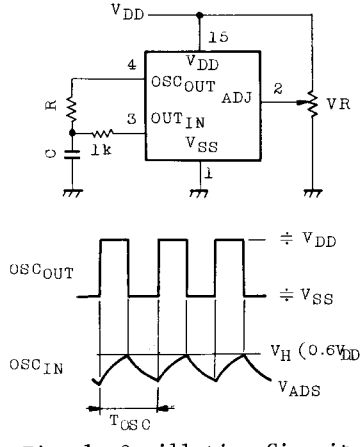


Fig. 1 Oscillation Circuit

2. Counting circuit (Frequency dividing circuit)

This circuit consists of the fixed frequency dividing stage of 1/1000 and the variable frequency dividing stage of 1/1 ∿ 1/600.

Time intervals of timer can be predetermined in eight ways by combining three inputs of S_0 ∿ S_2.

Select Input	S_2	L				H			
	S_1	L		H		L		H	
	S_0	L	H	L	H	L	H	L	H
Time intervals of Timer		T	3T	6T	10T	60T	30T	300T	600T

Note 1. $T = 1000 \cdot T_{OSC}$

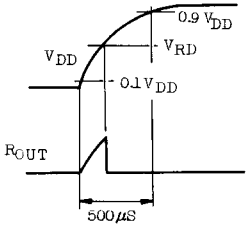
Note 2. "L" level may be open.

3. Reset operation

The internal counter is kept reset by the built-in auto reset circuit until the power supply level reaches reset release voltage (V_{RD}) at time of application of power. However, the power rising time of more than 500μs should be taken for abrupt rising edge of power supply because there may be no possibility of the internal counter being reset. In case of the rising time of 500μs or below, differentiation circuit is made up by adding the capacitor to $\overline{RESET}$ terminal. (Refer to Fig. 2)

It is a matter of course that the internal circuit can be reset even by setting $\overline{RESET}$ input at "L" level. When the reset operation is released, oscillating and counting operations start. The reset signal is being output to this IC.

In case where this pin (R_{OUT}) is internally reset, it is off (at the rising time of power supply and during "L" level of $\overline{RESET}$); therefore, this pin can be used for making the external circuit synchronize by use of pull-up resistance or equivalent. While R_{OUT} is not in use, it should be kept set open (or at "L" level).



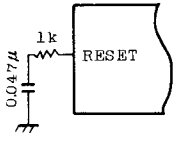


Fig. 2 Auto Reset Circuit

4. Inhibit operation

Oscillation can be stopped by setting $\overline{INHIBIT}$ input at "L" level.
Normal operation can be performed by setting $\overline{INHIBIT}$ input open (or at "H" level).

5. Divider function

When the T/D pin is set open (or at "H" level), this device operates as a timer. When this pin is set at "H" level, this divice can be used as a divider which continues operating oscillation/counting without creating time-up signal.

For the divider mode, however, R_{OUT} cannot be used. (Open or "L").

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		6.2	-	10	V
High Level Input Voltage	V_{IH}		0.8V_{DD}	-	V_{DD}	V
Low Level Input Voltage	V_{IL}		0	-	0.2V_{DD}	V
External Resistor	R		5K	-	2M	Ω
External Capacity	C		1000P	-	5μ	F
Output Voltage	V_{OUT}	* Applcable to R_{OUT}' Q/10	0	-	10	V

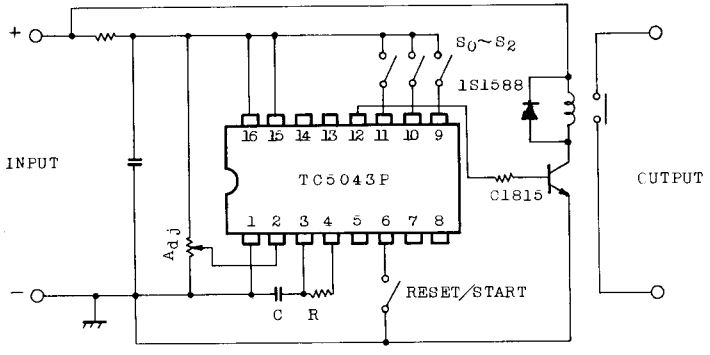
ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Zener Voltage	V_Z	I_Z=1mA	-	6.2	8.1	6.5	7.2	8.2	6.6	8.5	V
		I_Z=10mA		6.2	8.1	6.5	7.3	8.2	6.6	8.5	
High Level Output Current	I_{OH}	V_{OH}=6V	7	-1.2	-	-1.2	-2.5	-	-1.0	-	mA
		V_{OH}=3V		-5.2	-	-5.2	-9.0	-	-4.0	-	
Low Level Output Current	I_{OL}	V_{OL}=0.4V	7	1.0	-	1.0	2.0	-	0.8	-	
High Level Input Current	I_{IH}	V_{IH}=10V, (Exclusive of $S_0 \sim S_2$)	10	-	5	-	10^{-3}	5	-	5	μA
Low Level Input Current	I_{IL}	V_{IL}=0V, (Exclusive of R·$\overline{INH}$·T/D)	10	-	-5	-	-10^{-3}	-5	-	-5	
Pull-up Resistance	R_{PU}	R, $\overline{INH}$, T/D Inputs	-	7	50	10	20	50	10	75	kΩ
Pull-down Resistance	R_{PD}	S_0, S_1, S_2 Inputs	-	45	200	66	100	200	66	300	
Output OFF Current	I_{OFF}	V_{OH}=10V, R_{OUT}, Q/10 Outputs	10	-	1.0	-	10^{-3}	1.0	-	10.0	μA
Auto Reset Release Voltage	V_{RD}		-	-	-	2.6	-	5.2	-	-	V
Supply Current	I_{DD}	C=0.1μF, R=1MΩ*	10	-	-	-	0.3	-	-	-	mA

* All inputs and outputs are open.

EXAMPLES OF APPLIED CIRCUIT

∘ Timer Circuit I (Basic Type)



(Time of timer can be varied to linear by using resistor R deciding time constant with variable resistance.)

∘ Timer Circuit II (Elapsed Time Displaying Type)