SD Memory Card / SDIO Card Controller

TC6387XB

Outline

Rev. 1.0 2002-02-06

TOSHIBA CORPORATION

Revision History

TITLE: TC6387XB Specifications

REV NO.	DATE	CONTENTS	REVISED by	APP'D by
0.90a	2001-08-17	Released 1st edition	S. Ueta	T. Takada
0.90b	2001-11-12	*Modified SD Control Register Map again(page 16). *Regarding [4.7 SDLED signal], added the comments in detail(page 21). *Regarding [4.7 Clock supply to SD Card], added the comments in detail(page 21-22). *Added DC and AC specifications(page 26-40).	S. Ueta	T. Takada
0.90c	2001-11-21	*Regarding [4.1.2 Compact Flash (CF) Interface], defined that #STSCHG of CF interface is not connected to TC6380AF signal(page 13). *Added [Appendix](page42-46).	S. Ueta	T. Takada
0.90d	2001-11-27	Corrected the written(page14, red letters).	S. Ueta	T. Takada
0.90e	2001-12-05	Added each signal states in suspend mode(#SUSPEND=Low)(page24).	S. Ueta	T. Takada
0.90f	2001-12-20	Added an interrupt specification in detail(Page19-37).	S. Ueta	T. Takada
0.90g	2001-12-25	Regarding AC Characteristic, modified written max time to min time. Regarding Attribute Memory Interface AC Characteristic, added a specification of thoh8 (page 57). Regarding SD Card Interface AC Characteristic, modified a specification of Fpp (16MHz→25MHz) (Page 59).	S. Ueta	T. Takada
1.0	2002-02-06	Deleted the function of CompactFlash Interface. Then, defined again HISEL signal as RSV2 signal. Deleted the function of SDICK. Then, defined again SDICK signal as RSV0 signal and CKSEL signal as RSV1 signal. Modified [4.5 Interruption]. Modified the recommended external resistances of #SDCD and SDWP signals. Added [6. Caution in coding device driver]. Added [B Reference diagram].	S. Ueta	T. Takada

Contents

1 Overview

TC6387XB is a controller LSI for SD Memory Card/SDIO Card that comes in with interfaces for Standard Memory with 16 bits bus. Also, TC6387XB meets SD Memory Card Physical Layer Specification and SD I/O Card Specification. TC6387XB automatically detects card types and power supply just by inserting SD Memory Card or SDIO Card.

By using buffer-off function of #SUSPEND signal and gated clock control, power consumption of the system can be kept to a minimum.

1.1 Chip Specifications

- 0.35um CMOS Process
- 0.8mm ball Pitch 64-pin FBGA Package
  (Body Size: 7mm×7mm)
  (Height : Max.1.2mm)

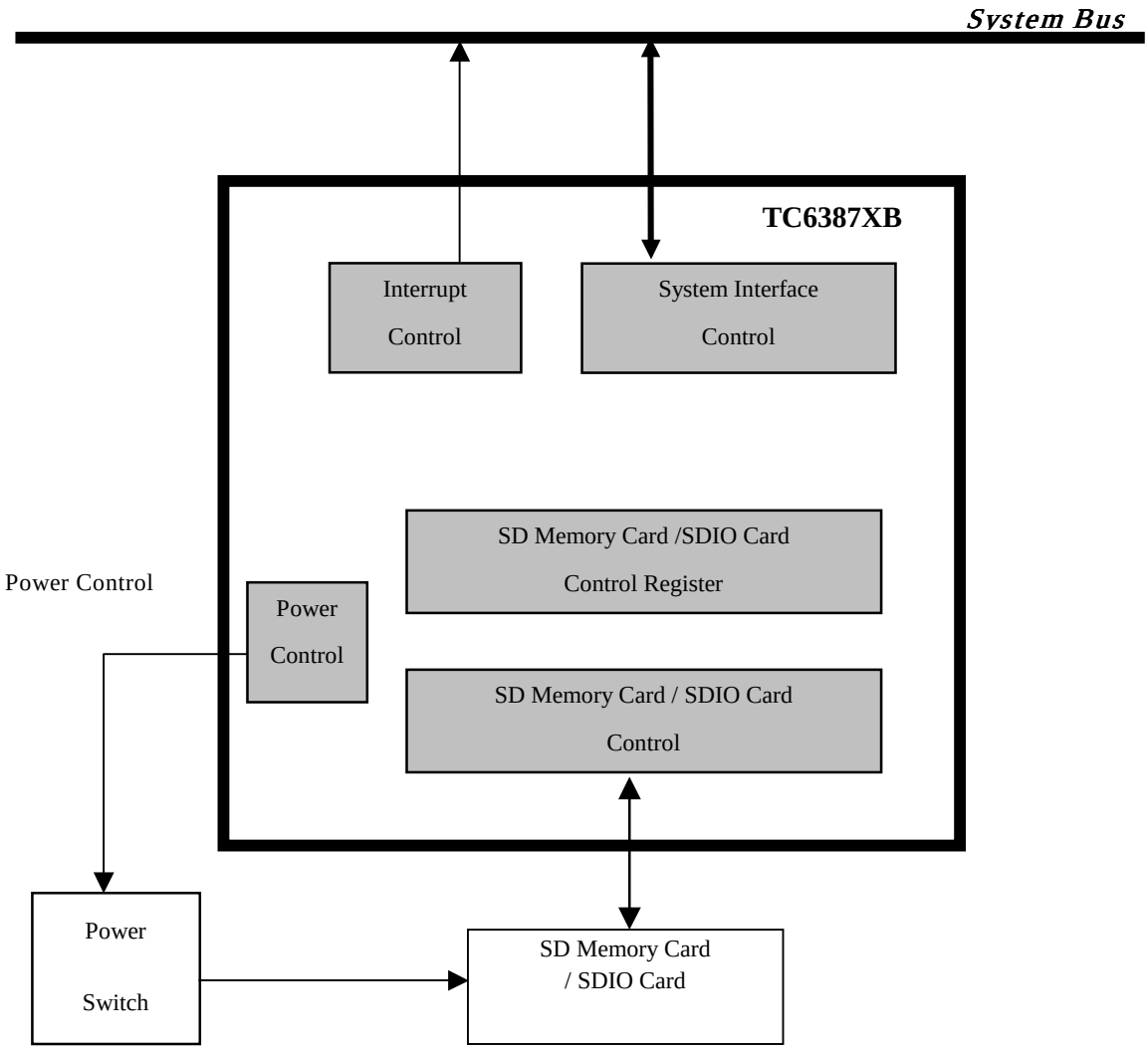
FBGA Package

1.2 Overview Specifications

- Host Bus Interface
  - Standard Memory Interface
  - 16 bit bus Interface
- Interruption Support
- Operating Frequency 33MHz
- Compatible w/ Power Supply Control LSI MIC2563
- Supports SD Card 1 Slot
- Meets SD Memory Card Physical Layer Specification Ver.1.0
  - Operating Frequency (Max. 25MHz)
  - MultiMedia Card Read/Write Capability
  - Compatible w/ 3.3V
  - Compatible w/ Multi Block Write/Read
  - Not compatible w/ SPI Mode
  - Within 512Byte*2 Double Buffers
- Meets SD I/O Card Specification Ver.1.0
  - Operating Frequency (Max. 25MHz)
  - Compatible w/ 3.3V
  - Compatible w/ Multi Block Write/Read

Though Toshiba specified TC6387XB DC supply voltage range(3.0v < Vdd < 3.6v) as recommended commercial operating condition, SDIO card specification has different DC supply voltage range(3.1v < Vdd < 3.5v). Toshiba recommend DC supply voltage range(3.1v < Vdd < 3.5v) in case customer use a SDIO card with TC6387XB as recommended commercial operating condition.

2 Block Diagram



3 Signals

3.1 Pin Assignments

Top View

	1	2	3	4	5	6	7	8
A	CLK32	RSV0	TST1	#SUSPEND	#HCS	HA1	HA5	HA6
B	SDPWR	VDD	TST2	RSV1	HA2	HA3	VDD	HA7
C	VDD	SDCD3	SDCD2	TST0	RSV2	HA4	HA8	HA9
D	SDCLK	SDCMD	SDCD1	VSS	VSS	HA10	HA11	HD1
E	SDCD0	#SDCD	SDWP	VSS	VSS	HD0	HD4	HD2
F	SDLED	HRDY	#PCLR	HD14	HD12	HD6	HD5	HD3
G	#HINT	VDD	#HOE	#HWE	HD13	HD10	VDD	HD7
H	HCLK	VSS	#HBEH	#HBEL	HD15	HD11	HD9	HD8

3.2 Pin Signals

Host Interface (33-pin)

NAME	Pin	IO	VCC (V)	FUNCTION/REMARKS
HD15	H5	IO	3.3	System Data 15-0
HD14	F4			
HD13	G5			
HD12	F5			
HD11	H6			
HD10	G6			
HD9	H7			
HD8	H8			
HD7	G8			
HD6	F6			
HD5	F7			
HD4	E7			
HD3	F8			
HD2	E8			
HD1	D8			
HD0	E6			
HA11	D7	I	3.3	System Address 11-1
HA10	D6	I		
HA9	C8	I		
HA8	C7	I		
HA7	B8	I		
HA6	A8	I		
HA5	A7	I		
HA4	C6	I		
HA3	B6	I		
HA2	B5	I		
HA1	A6	I		
#HCS	A5	I		Chip Selection
#HOE	G3	I		Output Enabled
#HWE	G4	I		Write Enabled
#HBEL	H4	I		Byte Enabled L
#HBEH	H3	I		Byte Enabled H
HRDY	F2	O (OD) *1		Ready

*1 Levels cannot be converted.

Pin Signals (cont'd)

SD Card Interface (9-pin)

NAME	Pin	IO	VCC (V)	FUNCTION/REMARKS
SDCD3	C2	IO	3.3	SD Card /Data Bus
SDCD2	C3			
SDCD1	D3			
SDCD0	E1			
SDCMD	D2			SD Card /Command
SDCLK	D1	O		SD Card /Divided HCLK Clock for SD Card(Max.25MHz)
#SDCD	E2	I		SD Card /Detection
SDWP	E3			SD Card /Write Protection Media is write-protected when this Pin indicates "High".
SDLED	F1	O		SD Card /LED signal

* Buffer with pull-up resistance

SD Card Power Supply Control (1-pin)

NAME	Pin	IO	VCC (V)	FUNCTION/REMARKS
SDPWR	B1	O	3.3	SD Card Power Supply Control. 3.3V Enable Signal

Pin Signals (cont'd)

SYSTEM Interface (5-pin)

NAME	Pin	IO	VCC (V)	FUNCTION/REMARKS
HCLK	H1	I	3.3	System Clock (max.33MHz)
CLK32	A1			Used for card detection and for interruption detection when HCLK is stopped.
#HINT	G1	O (OD) ***1**		Interruption
#PCLR	F3	I		All registers are cleared when this signal is asserted
#SUSPEND	A4			Suspend

***1** Levels cannot be converted.

TEST Pin (3-pin)

NAME	Pin	IO	VCC (V)	FUNCTION/REMARKS
TST2	B3	I	3.3	Test Mode Signal 2,1,0 Utilized for Test Mode Set "000" for TST[2-0] under normal circumstances.
TST1	A3			
TST0	C4			

Other Pin (3-pin)

NAME	Pin	IO	VCC (V)	FUNCTION/REMARKS
RSV0	A2	I	3.3	Link to directly ground.
RSV1	B4			Link to directly ground.
RSV2	C5			Link to directly ground.

3.3 Power Supply/GND (10 pins)

NAME	Pin	FUNCTION/REMARKS
VSS	H2, D4, E4, D5, E5	GND
VDD	C1, B2, G2, B7, G7	3.3V

3.4 Summary: Interface Pins

Interface	# of Pins	Remarks
Host	33	
SD Card	9	
SD Card Power Supply Control	1	
System	11	SYSTEM Interface, TEST Pins, Other Pins
Total	54	
Power Supply	5	
GND	5	
Grand Total	64	

4 Functionality Descriptions

4.1 Host Interface

TC6387XB supports standard memory interfaces and the following suggests examples of circuits for connecting to Standard Memory Interface:

Standard Memory	TC6387XB
A11-1	HA11-1
D15-0	HD15-0
-CS	#HCS
-OE	#HOE
-WE	#HWE
-BEH	#HBEH
-BEL	#HBEL
-RDY	HRDY

4.2 Resource Area

TC6387XB holds the following Resource Area:

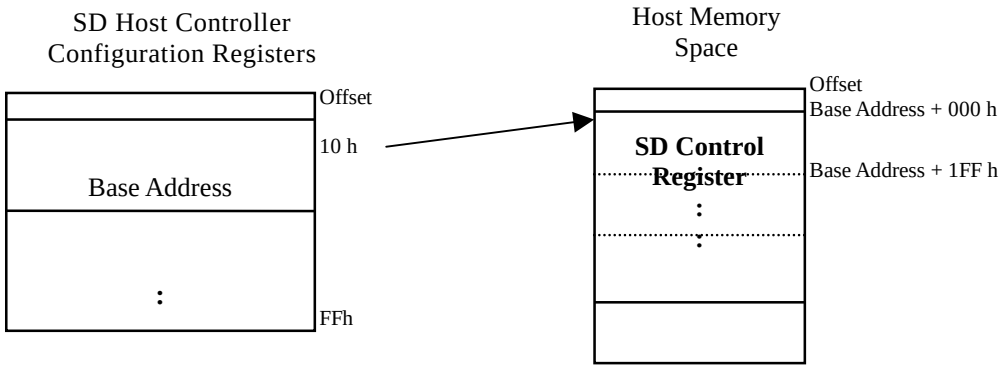
1) SD Host Controller Configuration Area
2) SD Control Register Area

See below for mapping of SD Host Controller Configuration Area and SD Control Register Area. Further, SD Control Register Area are mapped to any memory resources(800-FFFh) by setting BASE Address Register in SD Host Controller Configuration Area.

Offset A11-1	FUNCTION/REMARKS
000 - 0FFh	Reserved for Configuration Area
100 - 1FFh	Reserved for Configuration Area
200 - 2FFh	SD Host Controller Configuration Area
300 - 3FFh	Reserved for Configuration Area
400 - 7FFh	Reserved for Configuration Area
800 - 8FFh 900 - 9FFh A00 – AFFh B00 - BFFh C00 - FFFh	SD Control Register (BASE Address Register of SD Host Controller Configuration Register —configurable in Offset10h--)

- SD Control Register Area

As for accessing Resource in SD Control Register Area, use Configuration Register Base Address Reg.(Config.offset: 10h) in SD Host Controller for mapping the settings to access designated Memory Areas (800-FFFh).



4.3 Register Map

TC6387XB holds internal registers for SD Host Controller.

- SD Host Controller Configuration Register
- SD Control Register

4.3.1 SD Host Controller Configuration Register

31 23	15 07	00	Port
Reserved 2	Reserved 1		00h
Reserved 3	Command		04h
Reserved 5	Reserved 4		08h
Reserved 6			0Ch
SD Control Register Base Address			10h
			14h
			18h
			1Ch
			20h-2Bh
Reserved 8	Reserved 7		2Ch
			30h
	Reserved 9		34h
			38h
	Interrupt Pin	Reserved 10	3Ch
Clock Mode	Gated Clock Control	Stop Clock Control	40h
	Pin Status		44h
Power Control3	Power Control2	Power Control1	48h
	Reserved 11	Card Detect Mode	4Ch
		SD Slot	50h
			54h
	Reserved 12		58h
			5Ch
	Reserved 13		60h
			64h-7Fh
Reserved 16	Reserved 15	Reserved 14	80h
Reserved 19 Reserved 18	Reserved 17		84h
	Reserved 20		88h
			8C-EFh
Reserved 21	Extend Gated Clock Control2	Extend Gated Clock Control1	F0h
Reserved 24	Reserved 23	Reserved 22	F4h
SDLED Enable 1	Extend Gated Clock Control3	Reserved 25	F8h
Reserved 28 SDLED Enable 2	Reserved 27	Reserved 26	FCh

4.3.2 SD Control Register

Base Address: SD Control Register Base Address (Conf.10h)

Offset	15-08 bit	07-00 bit	Offset	15-08 bit	07-00 bit
002h	SD Control Reserved 1		000h	SD Command	
006h	Argument1		004h	Argument0	
00Ah	Transfer Sector Count		008h	Stop internal action	
00Eh	Response1		00Ch	Response0	
012h	Response3		010h	Response2	
016h	Response5		014h	Response4	
01Ah	Response7		018h	Response6	
01Eh	SD Buffer Control & Error Status		01Ch	SD Card Status	
022h	SD Interrupt Mask1		020h	SD Interrupt Mask0	
026h	SD Memory Card Transfer Data Length		024h	SD Card Clock Control	
02Ah	---		028h	SD Memory Card Option Setup	
02Eh	SD Error Detail Status 1		02Ch	SD Error Detail Status 0	
032h	---		030h	SD Data Port	
036h	---		034h	Transaction Control	
03Ah	---		038h	---	
03Eh	---		03Ch	---	
0E2h	SD Control Reserved 2		0E0h	SD Software Reset	
0E6h	SD Control Reserved 3		0E4h	---	
0EAh	---		0E8h	---	
0EEh	---		0ECh	---	
0F2h	---		0F0h	---	
0F6h	SD Control Reserved 4		0F4h	---	
0FAh	SD Control Reserved 6		0F8h	SD Control Reserved 5	
0FEh	SD Control Reserved 8		0FCh	SD Control Reserved 7	
102h	SD Card Port Selection		100h	SD Command	
106h	Argument1		104h	Argument0	
10Ah	Transfer Block Count		108h	---	
10Eh	Response1		10Ch	Response0	
112h	Response3		110h	Response2	
116h	Response5		114h	Response4	
11Ah	Response7		118h	Response6	
11Eh	SD Buffer Control & Error Status		11Ch	SD Card Status	
122h	SD Interrupt Mask1		120h	SD Interrupt Mask0	
126h	SDIO Card Transfer Data Length		124h	---	
12Ah	---		128h	SDIO Card Option Setup	
12Eh	SD Error Detail Status1		12Ch	SD Error Detail Status0	
132h	---		130h	SD Data Port	
136h	Card Interrupt Control		134h	Transaction Control	
13Ah	SDIO Host Information		138h	Clock & Wait Control	
13Eh	SDLED Control		13Ch	Error Control	
1E2h	SD Control Reserved 9		1E0h	SD Software Reset	
1E6h	---		1E4h	---	
1EAh	---		1E8h	---	
1EEh	---		1ECh	---	
1F2h	---		1F0h	SD Control Reserved 10	
1F6h	---		1F4h	---	
1FAh	---		1F8h	---	
1FEh	---		1FCh	---	

4.4 Clock/Reset

4.4.1 Clock

TC6387XB holds the following two Input Clock Pins: HCLK, CLK32

(1) HCLK : System Clock Input (33MHz Max.).
Basic Clock for System Interface and internal operations.

(2) CLK32 : Clock Input for 32KHz. The interrupt signal, implied for a SD card insertion and detachment, shall be generated synchronous to this signal. In addition, this signal is base clock, which input to a register which set timeout error time on SD data from a SDIO card.

4.4.2 Reset-related items

- #PCLR: Reset Signal is asserted when power is supplied.
All registers(built into TC6387XB) are cleared by #PCLR.

Be sure to deactivate assertion of #PCLR when power supply and HCLK oscillation (better than 1ms) are fairly stable.

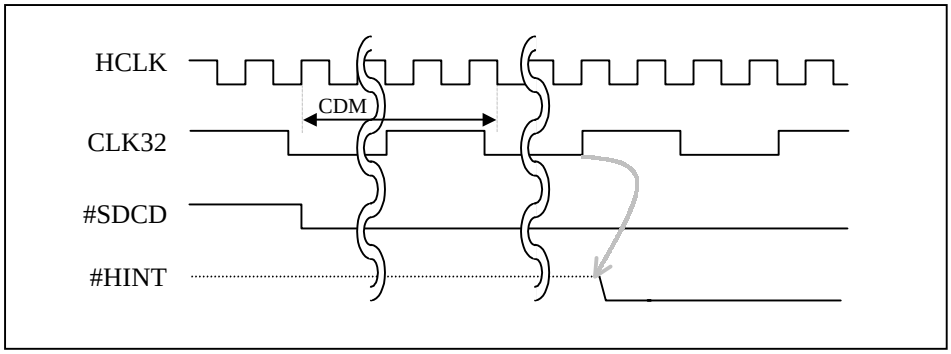
4.5 Interruption

When the TC6387XB detects the each interrupt sources, TC6387XB asserts interrupt signals (#HINT). It is necessary that the interrupt mask bits are released. This mask bits releasing is controlled by setting SD Interrupt Mask Register(Offset:020-023h, 120-123h). Each factor of the interrupt can be evaluated by referring to SD Card Status Register(Offset:01C-01Dh, 11C-11Dh) or SD Buffer Control & Error Status Register(Offset:01E-01Fh, 11E-11Fh). The details of each factor are listed below.

4.5.1 SD card insertion interrupt by #SDCD

+ Interrupt Assert Condition

When an SD card is inserted to a slot, #SDCD is lowered. This condition causes an interrupt to be generated. #SDCD is not recognized as being lowered unless it remains in "0" state for the number of HCLK cycles specified by CDM[1:0] of Card Detect Mode Register(Config Offset:4Ch). The interrupt is asserted in th timing of raising of CLK32 from #SDCD low state.



+ Factor Evaluation Method

The SCIN bit(D4) of SD Card Status Register(Offset:01C-01Dh) is set to "1".

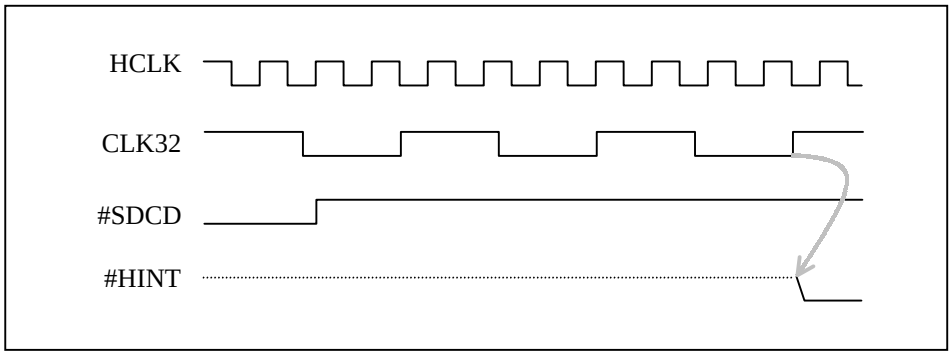
+De-asserting Method

(1) "0" is written into the SCIN bit(D4) of SD Card Status Register(Offset:01C-01Dh).
(2) "1" is written into the MCIN bit(D4) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

4.5.2 SD card removal interrupt by #SDCD

+ Interrupt Assert Condition

When an SD card in a slot is removed, #SDCD is raised. This condition causes an interrupt to be generated. After #SDCD is high, the interrupt is asserted in th timing of raising of CLK32.



+ Factor Evaluation Method

The SCOT bit(D3) of SD Card Status Register(Offset:01C-01Dh) is set to "1".

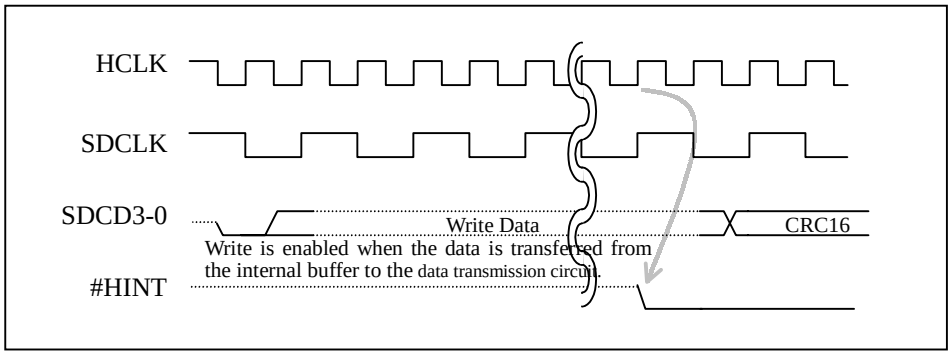
+De-asserting Method

(1) "0" is written into the SCOT bit(D3) of SD Card Status Register(Offset:01C-01Dh).
(2) "1" is written into the MCOT bit(D3) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

4.5.3 Buffer write enable interrupt

+ Interrupt Assert Condition

When data to be transmitted to the card becomes available for the internal buffer, SD Data Port Register(Offset:030-031h, 130-131h), to be written for a write command, an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SBWE bit(D9) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) is set to "1". In the case of SDIO Card, the SBWE bit(D9) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SBWE bit(D9) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MBWE bit(D25) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

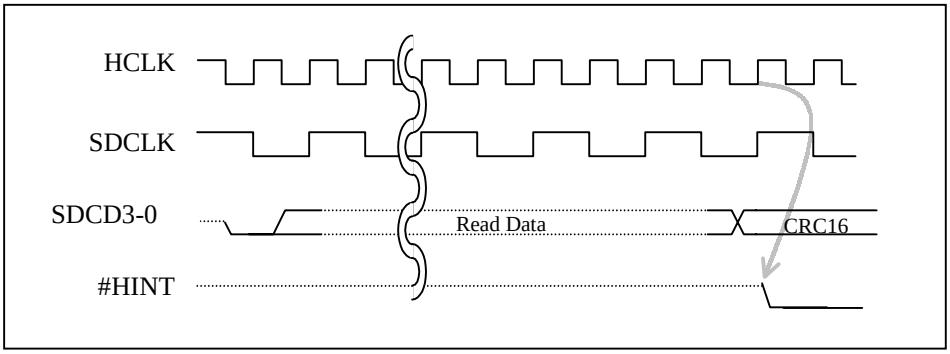
SDIO Card

(1) "0" is written into the SBWE bit(D9) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MBWE bit(D25) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.4 Buffer read enable interrupt

+ Interrupt Assert Condition

When one block of data from the card is stored fully into the internal buffer for a read command, an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SBRE bit(D8) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) is set to "1". In the case of SDIO Card, the SBRE bit(D8) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SBRE bit(D8) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MBRE bit(D24) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

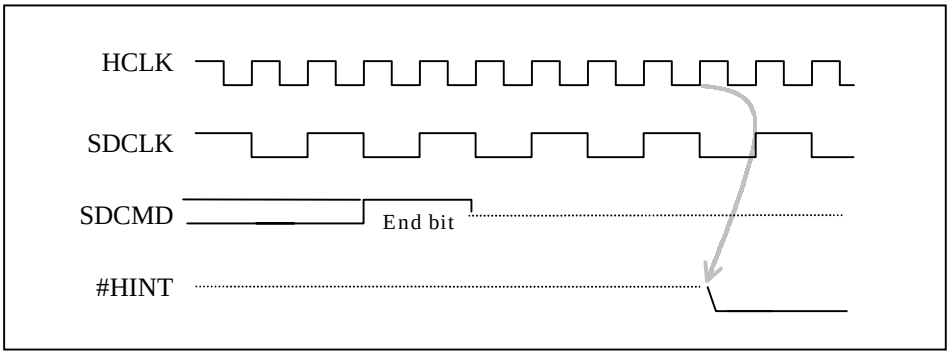
(5) "0" is written into the SBRE bit(D8) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(6) "1" is written into the MBRE bit(D24) of SD Interrupt Mask Register(Offset:120-123h).
(7) Hardware reset by #PCLR = “0”.
(8) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.5 Response end interrupt

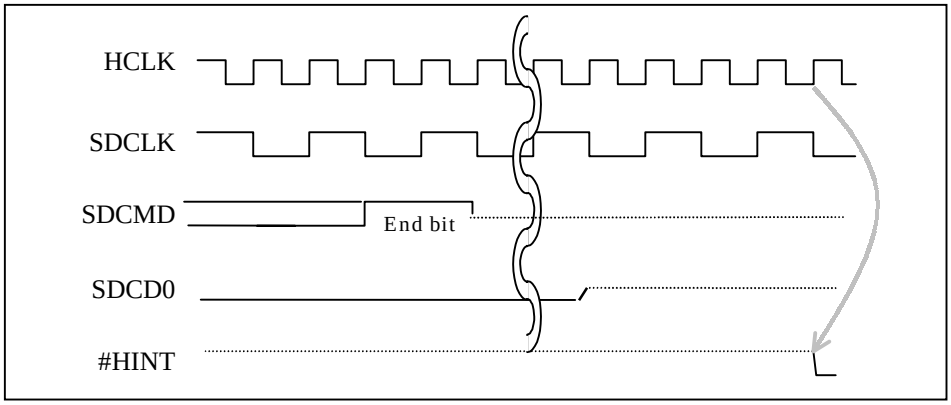
+ Interrupt Assert Condition

After a response received from an SD card, an interrupt is generated. Regarding R1b response type, after busy released from an SD card, an interrupt is generated.

<In the case of normal command>



<In the case of R1b command>



+ Factor Evaluation Method

In the case of SD memory Card, the SREP bit(D0) of SD Card Status Register(Offset:01C-01Dh) is set to "1". In the case of SDIO Card, the SREP bit(D0) of SD Card Status Register(Offset:11C-11Dh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SREP bit(D0) of SD Card Status Register(Offset:01C-01Dh).
(2) "1" is written into the MREP bit(D0) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

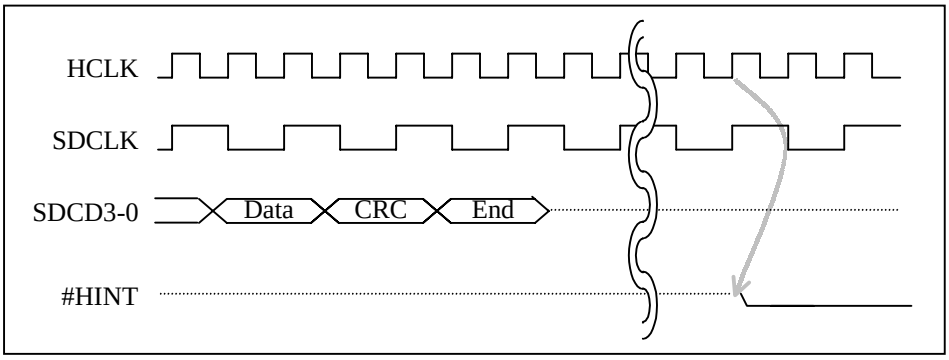
(1) "0" is written into the SREP bit(D0) of SD Card Status Register(Offset:11C-11Dh)
(2) "1" is written into the MREP bit(D0) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.6 R/W end interrupt

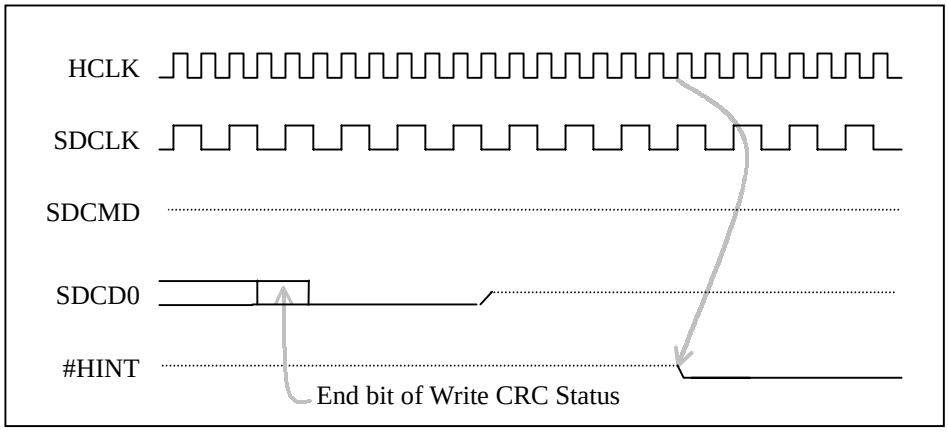
+ Interrupt Assert Condition

When read or write processing for an SD card is completed, an interrupt is generated.

<In the case of read command>



<In the case of write command>



+ Factor Evaluation Method

In the case of SD memory Card, the SRWA bit(D2) of SD Card Status Register(Offset:01C-01Dh) is set to "1". In the case of SDIO Card, the SRWA bit(D2) of SD Card Status Register(Offset:11C-11Dh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SRWA bit(D2) of SD Card Status Register(Offset:01C-01Dh).
(2) "1" is written into the MRWA bit(D2) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

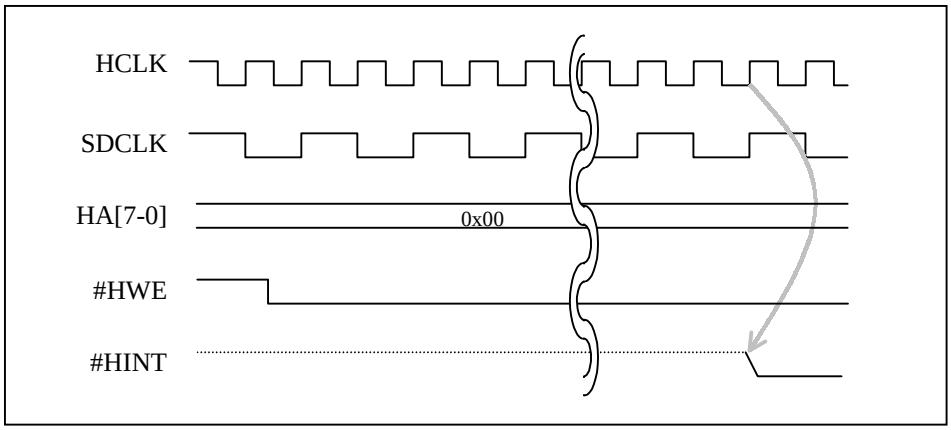
(1) "0" is written into the SRWA bit(D2) of SD Card Status Register(Offset:11C-11Dh)
(2) "1" is written into the MRWA bit(D2) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.7 Illegal access error interrupt

+ Interrupt Assert Condition

When an incorrect command index is written into SD Command Register(Offset:000-001h, 100-101h), an interrupt is generated. Each of the following cases is recognized as an incorrect index. (3) is only applying to SD memory Card.

(1) SD Command Register is written before the previously issued command is not completed.
(2) Though the REP2-0 bits(D10-8) are set to 011b(no response), the NTDT bit(D11) is set to 1b(with data).
(3) Though the CMD1-0 bits(D7-6) are set to 00b and the CIX bits(D5-0) are set to 001100b(CMD12), the NTDT bit(D11) is set to 1b(with data).



+ Factor Evaluation Method

In the case of SD memory Card, the ILA bit(D15) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) is set to "1". In the case of SDIO Card, the ILA bit(D15) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the ILA bit(D15) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the IMSK bit(D31) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

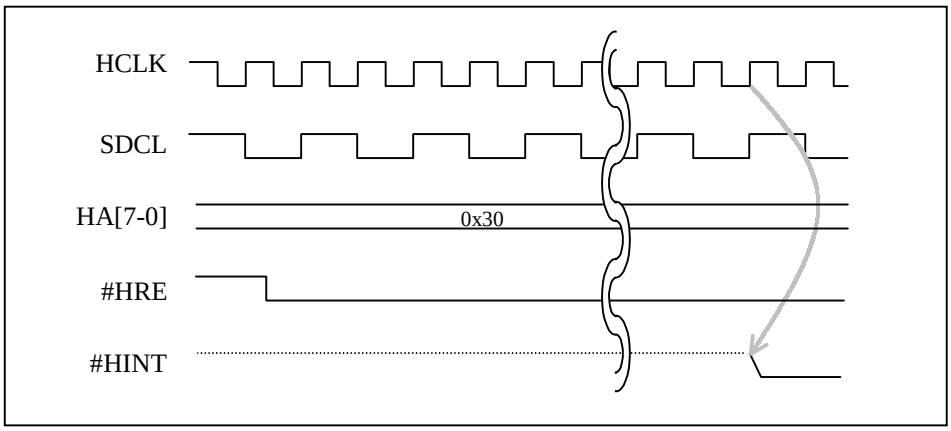
SDIO Card

(1) "0" is written into the ILA bit(D15) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the IMSK bit(D31) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.8 Buffer underflow error interrupt

+ Interrupt Assert Condition

If the host reads SD Data Port Register when the data buffer is empty, an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SFUF bit(D5) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) is set to "1". In the case of SDIO Card, the SFUF bit(D5) of SD Buffer Control & Error Status Register(Offset: 11E-11Fh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SFUF bit(D5) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MFUF bit(D21) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

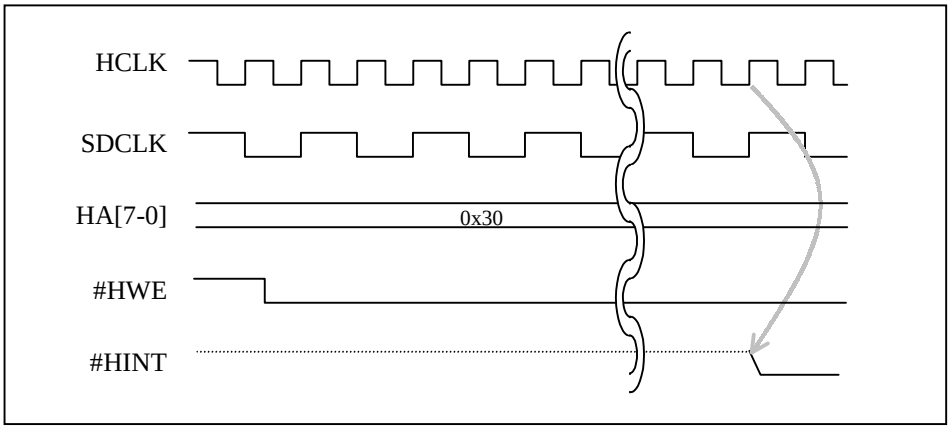
SDIO Card

(1) "0" is written into the SFUF bit(D5) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MFUF bit(D21) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.9 Buffer overflow error interrupt

+ Interrupt Assert Condition

If the host writes SD Data Port Register when the data buffer is full, an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SFOF bit(D4) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) is set to "1". In the case of SDIO Card, the SFOF bit(D4) of SD Buffer Control & Error Status Register(Offset: 11E-11Fh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SFOF bit(D4) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MFOF bit(D20) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

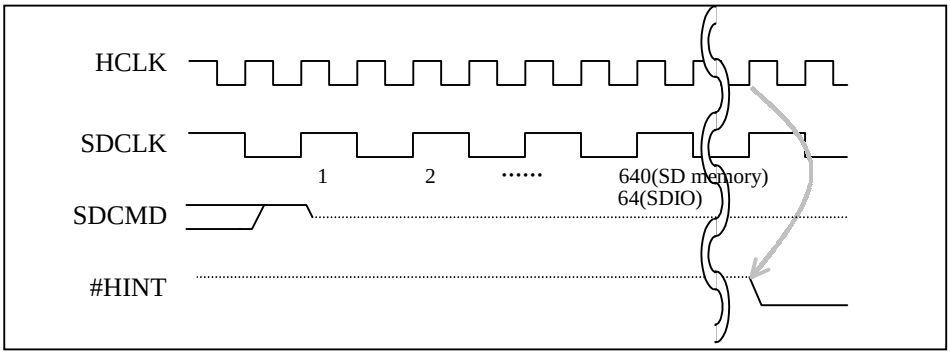
SDIO Card

(1) "0" is written into the SFOF bit(D4) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MFOF bit(D20) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.10 Time out error(command) interrupt

+ Interrupt Assert Condition

If the start bit of a response is not received within SDCLK period X 640(SD memory Card) or X 64(SDIO Card) after the end bit of a command is transmitted to the card, this condition is considered a time out error and an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SCTO bit(D6) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the NCR bit(D16) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1". However, if a response for automatically issued CMD12 is not received, the NRS bit(D17) is set to "1" for differentiation.

In the case of SDIO Card, the SCTO bit(D6) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the NCR bit(D16) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SCTO bit(D6) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MCTO bit(D22) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

(1) "0" is written into the SCTO bit(D6) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MCTO bit(D22) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

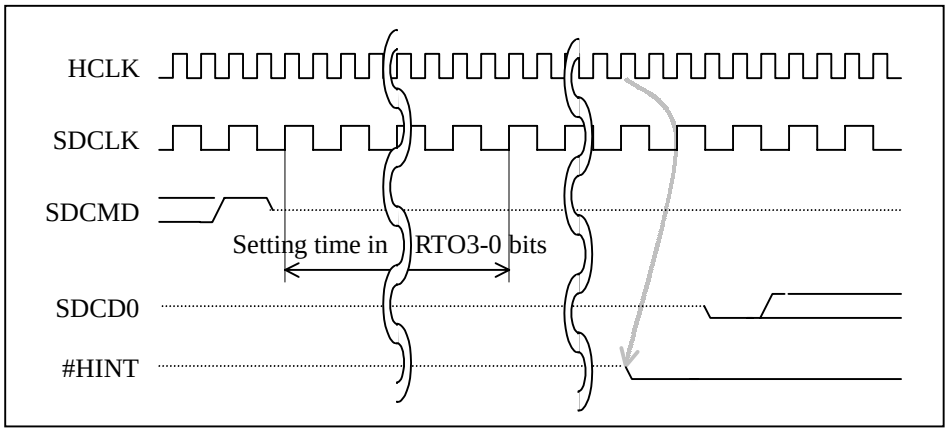
4.5.11 Read data time out error interrupt

+ Interrupt Assert Condition

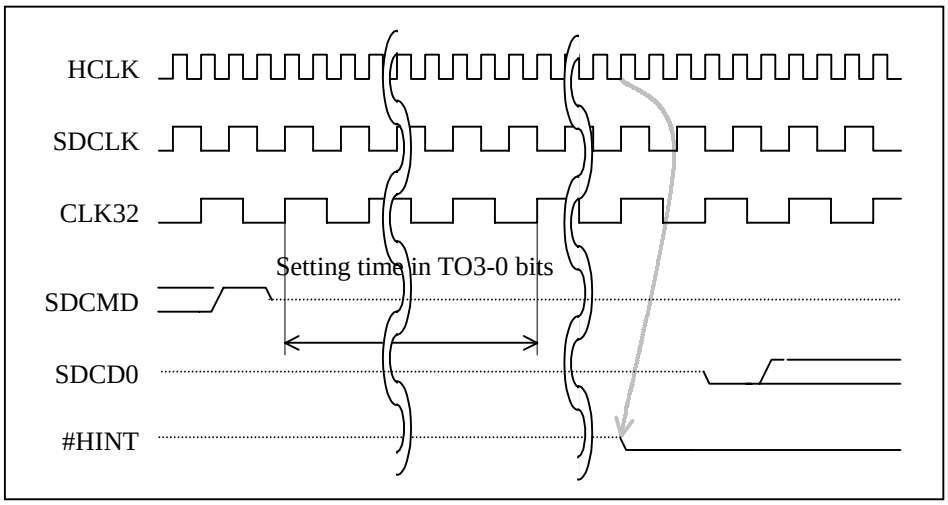
If the start bit of data is not detected within the specified period after the end bit of a response for each read command, an interrupt is generated. In the case of SD memory Card, the specified period is set in RTO[3:0] of SD Memory Card Option Setup Register(Offset:028h) in the form of a multiple number of the SDCLK period. In the case of SDIO Card, the specified period is set in TO[3:0] of SD Memory Card Option Setup Register(Offset:128h) in the form of a multiple number of the CLK32 period. Read data time out error is classified into between a command and a read data, and between a read data and a read data in a multiple block transfer.

*Between a command and a read data, time out

<In the case of SD memory card>

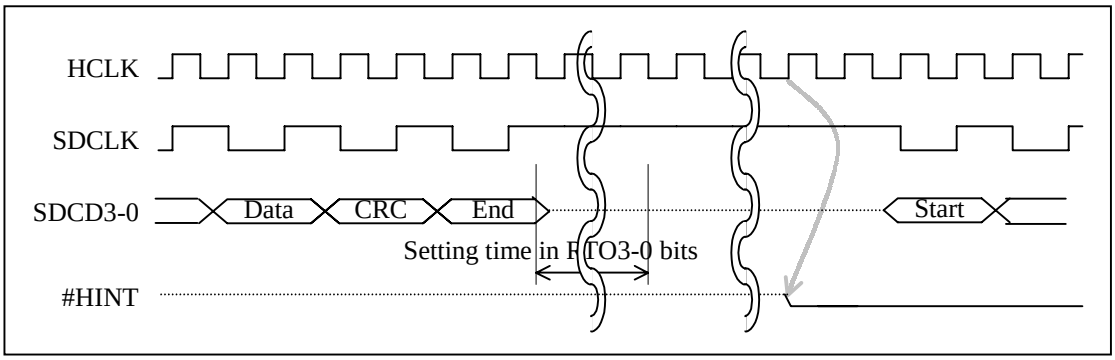


<In the case of SDIO card>

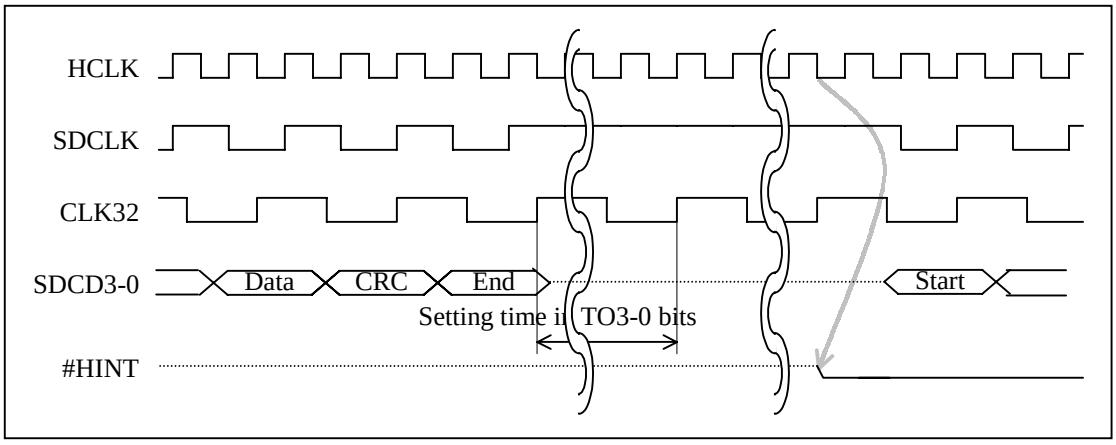


*Between a read data and a read data, time out

<In the case of SD memory card>



<In the case of SDIO card>



+ Factor Evaluation Method

In the case of SD memory Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the NRCS bit(D20) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the NRCS bit(D20) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

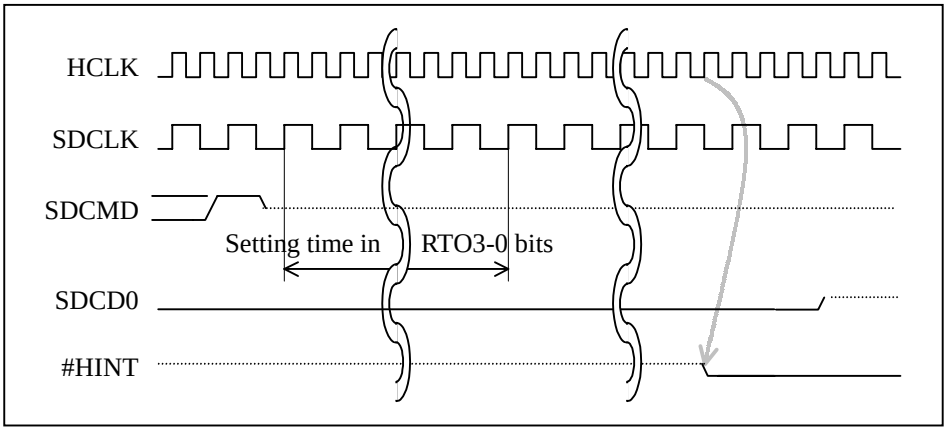
(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.12 Busy time out error interrupt

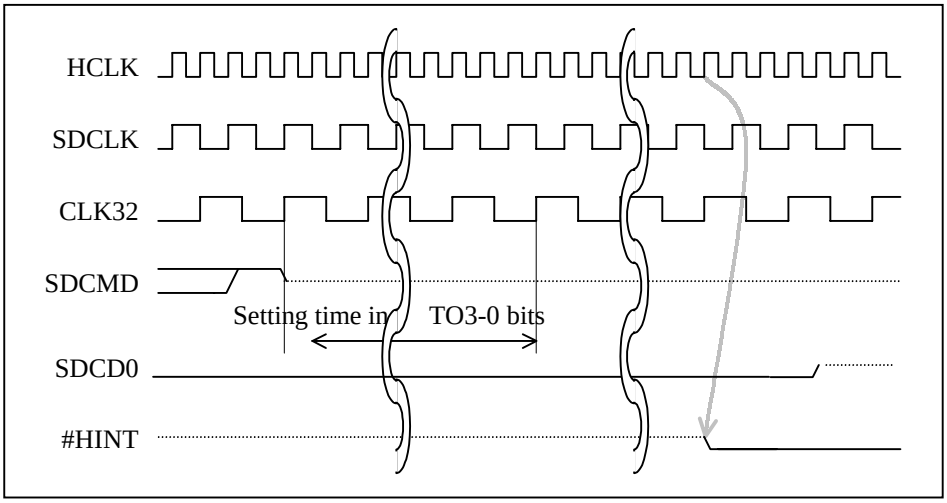
+ Interrupt Assert Condition

If a busy declaration from the card (DAT0 = "0" after response end) remains longer than the specified time, this condition is considered as a time out error and an interrupt is generated. In the case of SD memory Card, the specified period is set in RTO[3:0] of SD Memory Card Option Setup Register(Offset:028h) in the form of a multiple number of the SDCLK period. In the case of SDIO Card, the specified period is set in TO[3:0] of SD Memory Card Option Setup Register(Offset:128h) in the form of a multiple number of the CLK32 period.

<In the case of SD memory card>



<In the case of SDIO card>



+ Factor Evaluation Method

In the case of SD memory Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the NRCS bit(D20) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the NRCS bit(D20) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

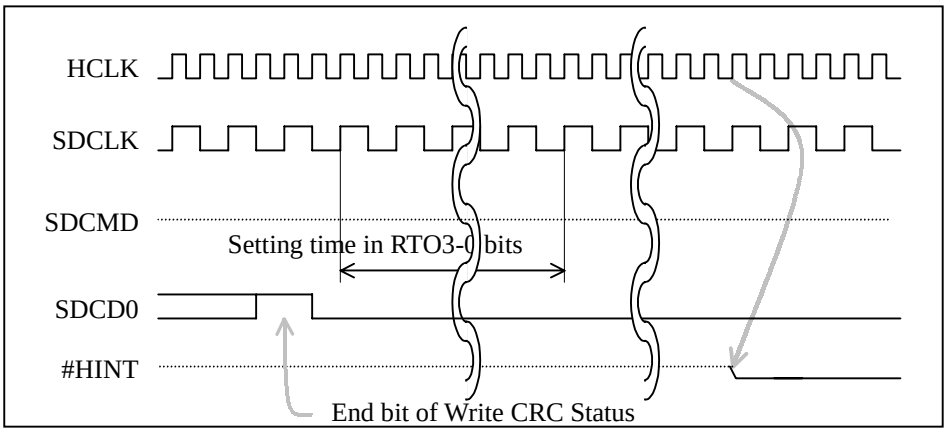
(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.13 CRC status busy time out error interrupt

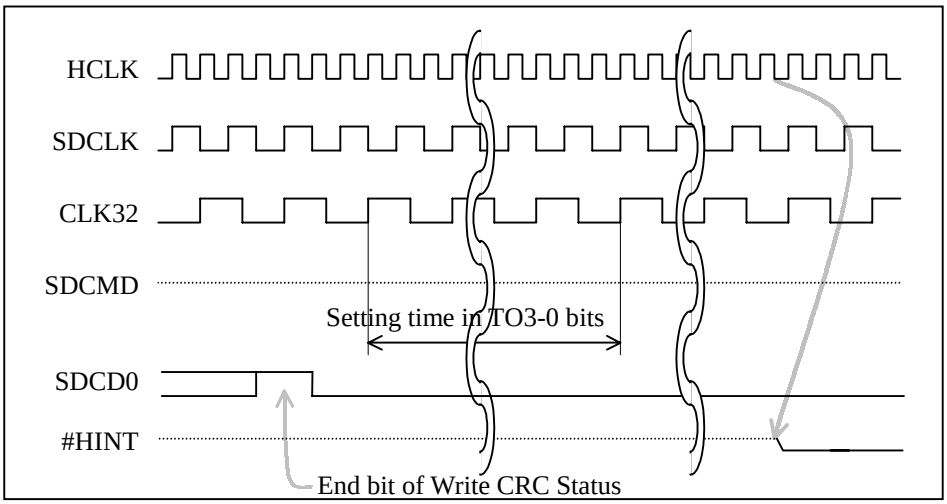
+ Interrupt Assert Condition

If a busy declaration from the card (DAT0 = "0" after Write CRC Status) remains longer than the specified time, this condition is considered as a time out error and an interrupt is generated. In the case of SD memory Card, the specified period is set in RTO[3:0] of SD Memory Card Option Setup Register(Offset:028h) in the form of a multiple number of the SDCLK period. In the case of SDIO Card, the specified period is set in TO[3:0] of SD Memory Card Option Setup Register(Offset:128h) in the form of a multiple number of the CLK32 period.

<In the case of SD memory card>



<In the case of SDIO card>



+ Factor Evaluation Method

In the case of SD memory Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the KBSY bit(D22) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the KBSY bit(D22) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

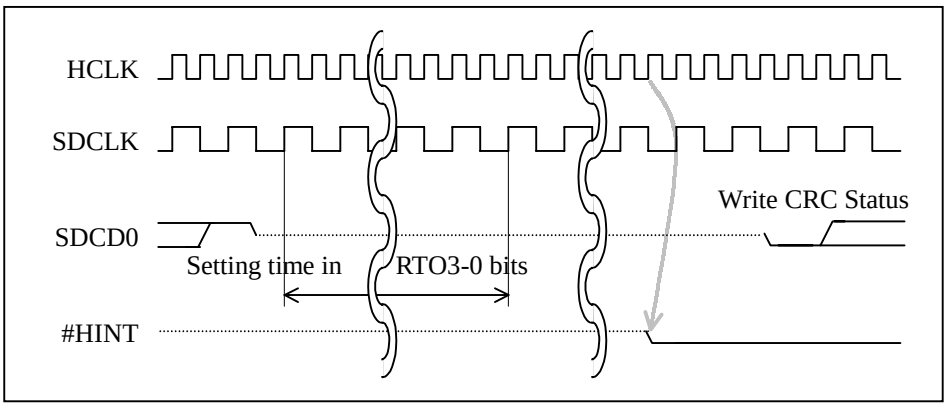
(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.14 CRC status time out error interrupt

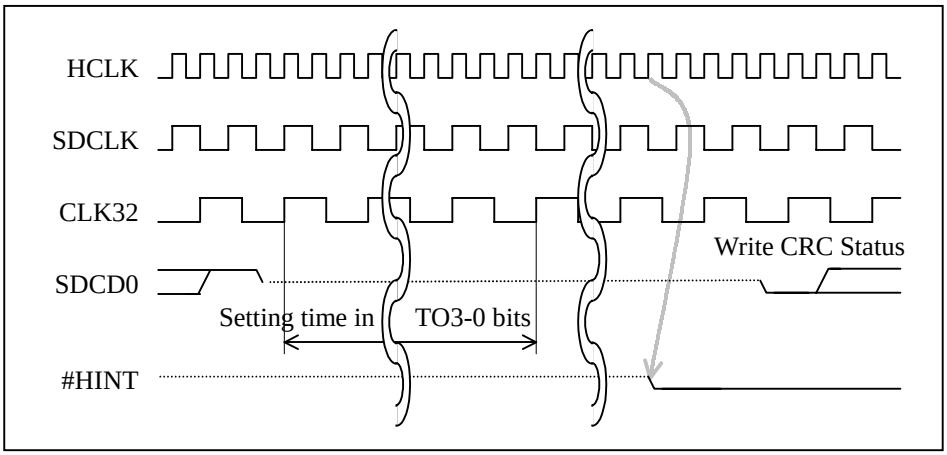
+ Interrupt Assert Condition

If the start bit of CRC status is not detected within the specified period after the end bit of block data for a write command, an interrupt is generated. In the case of SD memory Card, the specified period is set in RTO[3:0] of SD Memory Card Option Setup Register(Offset:028h) in the form of a multiple number of the SDCLK period. In the case of SDIO Card, the specified period is set in TO[3:0] of SD Memory Card Option Setup Register(Offset:128h) in the form of a multiple number of the CLK32 period.

<In the case of SD memory card>



<In the case of SDIO card>



+ Factor Evaluation Method

In the case of SD memory Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the NWCS bit(D21) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the NWCS bit(D21) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

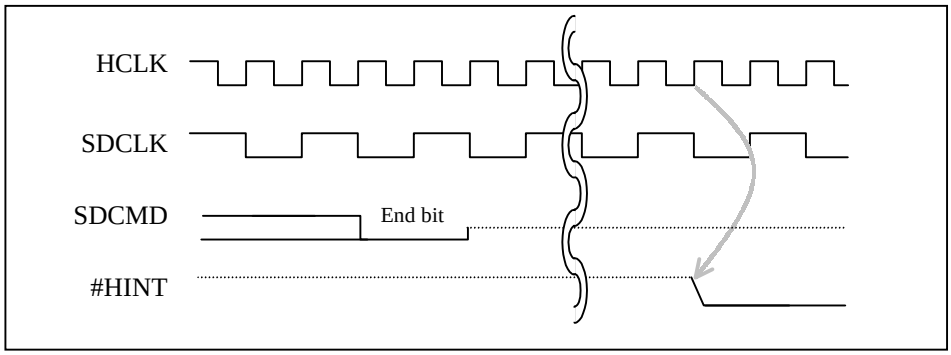
SDIO Card

(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.15 End bit error interrupt

+ Interrupt Assert Condition

If a bit that should be the end bit for the response, read data or CRC status received from the card is "0", an interrupt for detecting an incorrect end bit is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SEND bit(D2) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the WEBER bit, REBER bit, SEBER bit and CEBER bit(D5-2) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SEND bit(D2) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the WEBER bit, REBER bit and CEBER bit(D5-4,2) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

Bit	Name	Error factor	Notes
5	WEBER	End bit error for Write CRC status	
4	REBER	End bit error for read data	
3	SEBER	End bit error of a response for automatically issued CMD12	Only SD memory Card
2	CEBER	End bit error for a response (other than SEBER)	

+De-asserting Method

SD memory Card

(1) "0" is written into the SEND bit(D2) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MEND bit(D18) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

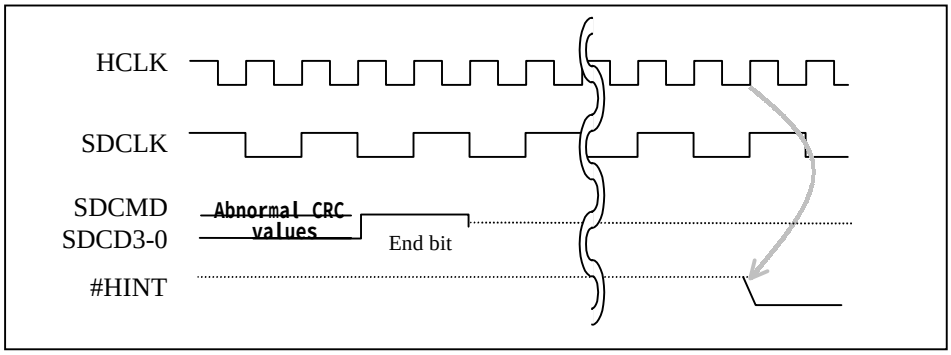
SDIO Card

(1) "0" is written into the SEND bit(D2) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MEND bit(D18) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.16 CRC error interrupt

+ Interrupt Assert Condition

If the CRC value for the response, read data or CRC status received from the card does not agree with the value internally calculated by TC6387XB, an interrupt is generated



+ Factor Evaluation Method

In the case of SD memory Card, the SCRC bit(D1) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the WCRCE bit, RCRCE bit, SCRCE bit and CCRCE bit(D11-8) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SCRC bit(D1) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the WCRCE bit, RCRCE bit and CCRCE bit(D11-10,8) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

Bit	Name	Error factor	Notes
11	WCRCE	Write CRC status error for a write command	
10	RCRCE	CRC error for read data	
9	SCRCE	CRC error of a response for automatically issued CMD12	Only SD memory Card
8	CCRCE	CRC error for a response (other than SCRCE)	

+De-asserting Method

SD memory Card

(1) "0" is written into the SCRC bit(D1) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MCRC bit(D17) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

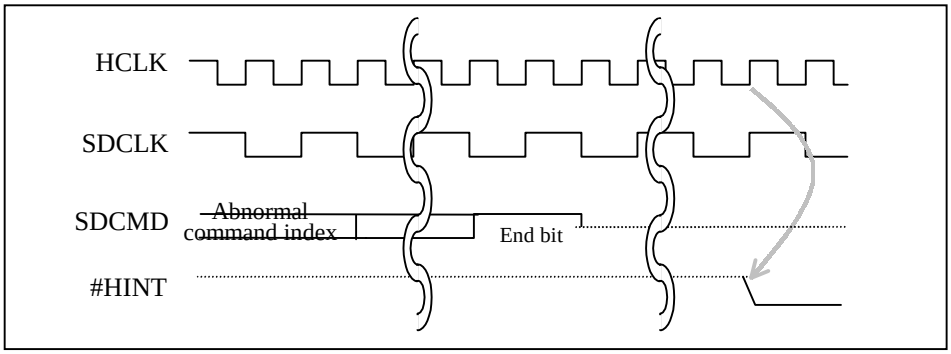
SDIO Card

(1) "0" is written into the SCRC bit(D1) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MCRC bit(D17) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.17 Command Index error interrupt

+ Interrupt Assert Condition

If the command index portion of the response received from the card does not agree with the index issued just before, an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SCIX bit(D0) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the RCMDE bit(D0) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1". If a response for automatically issued CMD12 is not normal, "1" is set to the SCMDE bit(D0).

In the case of SDIO Card, the SCIX bit(D0) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the RCMDE bit(D0) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SCIX bit(D0) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MCIX bit(D16) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

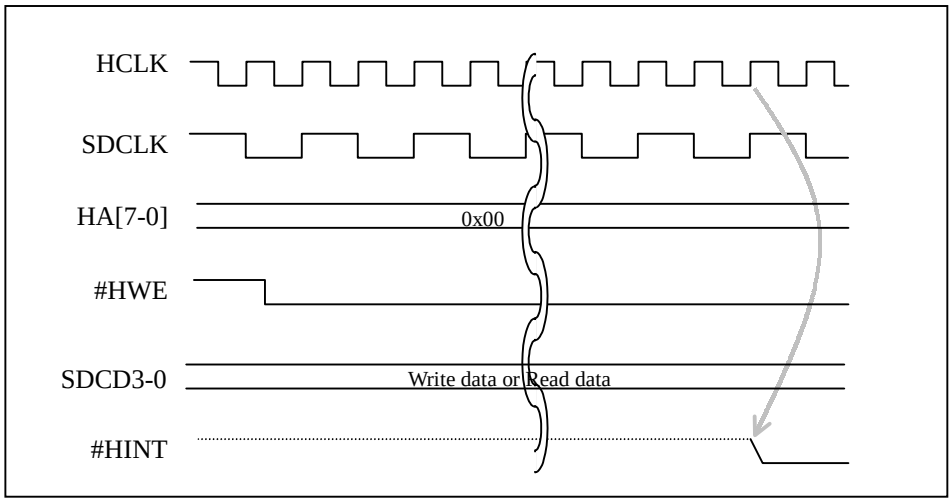
(1) "0" is written into the SCIX bit(D0) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MCIX bit(D16) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.18 Illegal function select interrupt

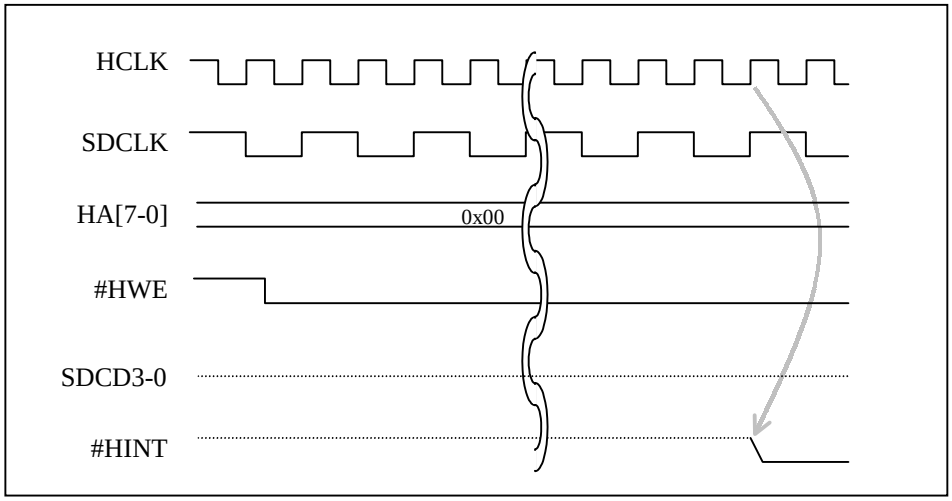
+ Interrupt Assert Condition

Although a transaction is remaining on the SD bus, or a state of SD controller is acceptable, other function in SDIO Card is selected by SD host controller, then an interrupt is generated.

<In the case of remaining transaction on the SD bus>



<In the case of SD controller is an acceptable state>



+ Factor Evaluation Method

The ILFSL bit(D13) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) is set to "1".

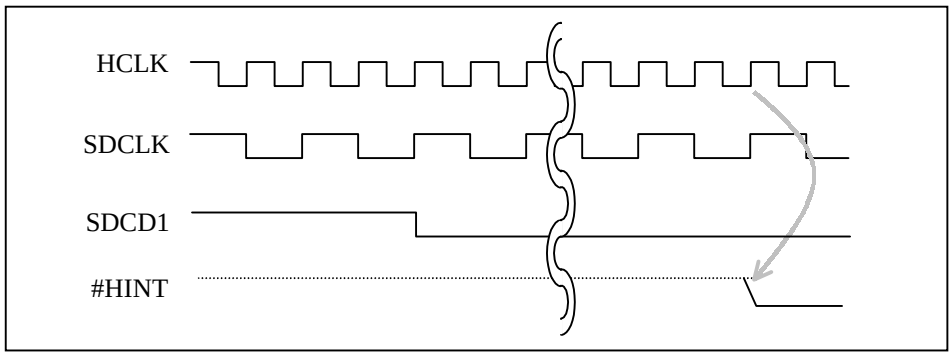
+De-asserting Method

(1) "0" is written into the ILFSL bit(D13) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the IFSMSK bit(D29) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.19 SDIO Card interrupt

+ Interrupt Assert Condition

When an interrupt from SDIO Card by using SDCD1 signal is detected, an interrupt is generated. Please release the interrupt mask by the CIMSK0 bit(D8) of Card Interrupt Control Register(Offset:136h), so the interrupt from #HINT would be generated.



+ Factor Evaluation Method

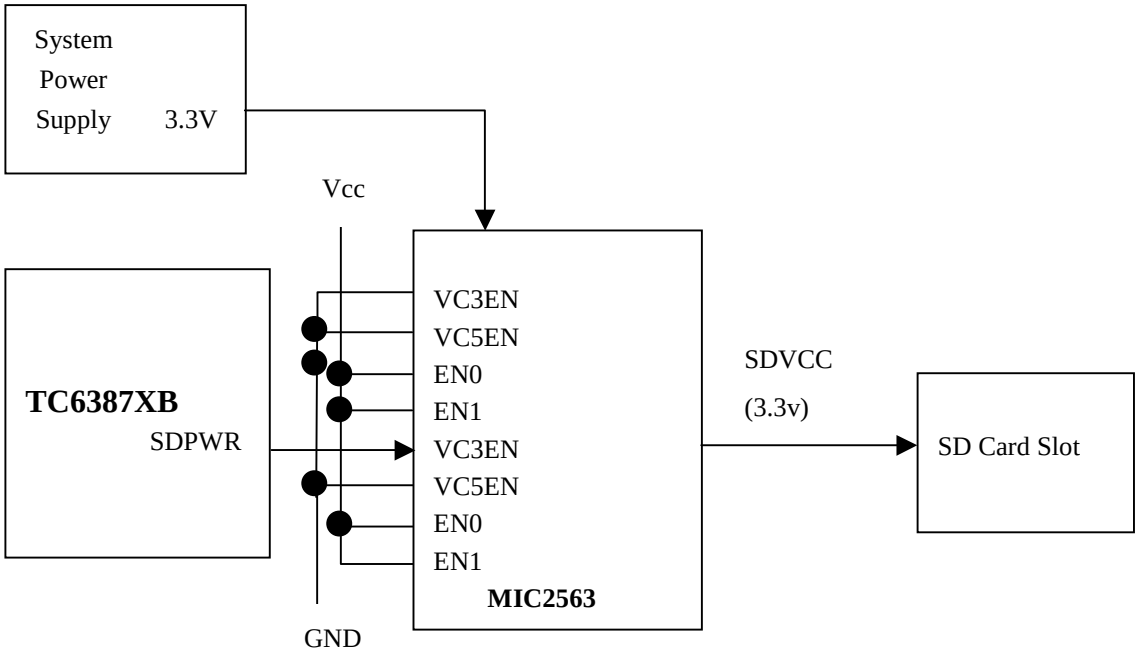
The CINT0 bit(D12) of Card Interrupt Control Register(Offset:136h) is set to "1".

+De-asserting Method

(1) "0" is written into the CINT0 bit(D12) of Card Interrupt Control Register(Offset:136h).
(2) "1" is written into the CIMSK0 bit(D8) of Card Interrupt Control Register(Offset:136h).
(3) Hardware reset by #PCLR = “0”.

4.6 Card Slot Power Supply Control

TC6387XB is designed to provide connection with MIC2563(Power Supply Control LSI).The following suggests applicable circuits:



4.6.1 SD Card Slot Power Supply Controller

Power supply for SD Card is controlled by configuring Power Control Register 2(Config Offset 49h) after detecting SD Card insertion. When #SUSPEND is asserted to low, power supply for SD Card can be automatically shut out by configuring Power Control Register 3(Config Offset 4Ah).

Parallel Power Supply Control Signals

Signal Name	Function/Remarks	Pin
SDPWR	SD Card Slot Power Supply Controller. 3.3V Enable Signal	B1

4.7 SDLED signal

TC6387XB has the SDLED signal for SD interface. This signal is controlled by setting SDLED Control Register(Offset:13Eh). Before accessing SDLED Control Register(Offset:13Eh), please set following registers.

*Set SDLED Enable Register 1(Config Offset:FAh) to 12h.

*Set SDLED Enable Register 2(Config Offset:FEh) to 80h.

4.8 Clock supply to SD Card

The SDCLK signal is used for a provision of SD Memory Card or SDIO Card. Please refer to the following setting for enabling the SDCLK output.

(1) Set Stop Clock Control Register (Config Offset:40h) to 1Fh.
(2) Set D0 of SD Software Reset Register (Offset:0E0h) to 1b.
(3) Set D7-0 of SD Card Clock Control Register (Offset:024h). These bits are used for setting the frequency of SDCLK.
    80h : SDCLK=HCLK/512
    40h : SDCLK=HCLK/256
    20h : SDCLK=HCLK/128
    10h : SDCLK=HCLK/64
    08h : SDCLK=HCLK/32
    04h : SDCLK=HCLK/16
    02h : SDCLK=HCLK/8
    01h : SDCLK=HCLK/4
    00h : SDCLK=HCLK/2

In addition, TC6387XB holds a function that SDCLK can have same frequency as HCLK. In this case, D7-0 settings of SD Card Clock Control Register (Offset:024h)becomes invalid setting.

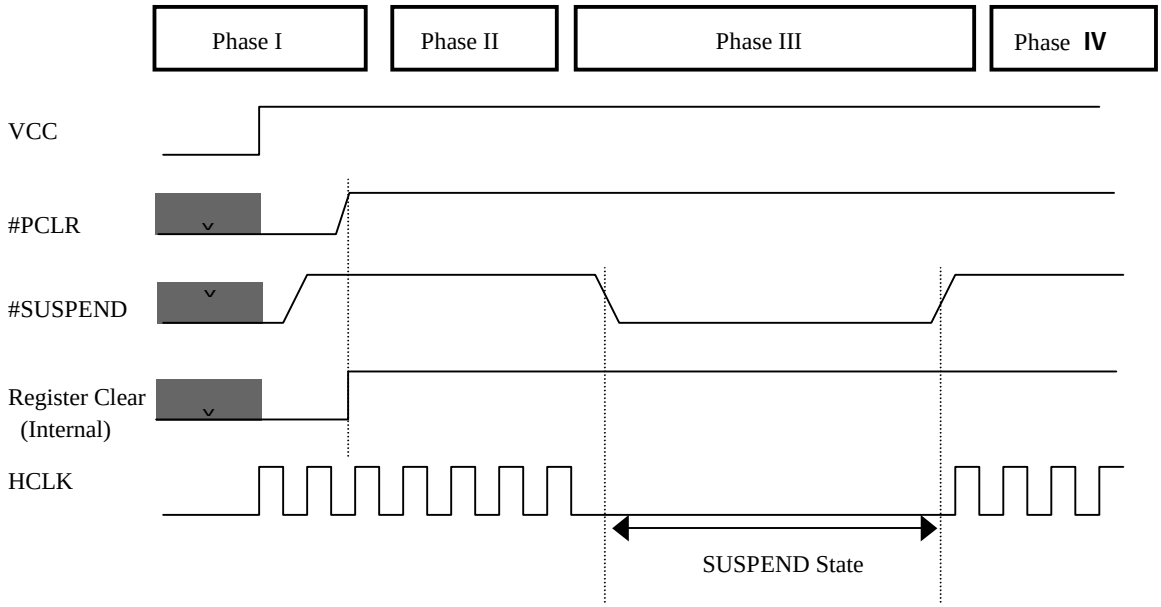
* Set D0 of Clock Mode Register (Config Offset:42h) to 1b.
* Set D15 of SD Card Clock Control Register (Offset:024h) to 1b.

Please attend that the specification of SDCLK is max.25MHz at the case of SD Card and is max.20MHz at the case of MultiMedia Card.

(4) D8 of SD Card Clock Control Register (Offset:024h) to 1b.
(5) D8 of Clock & Wait Control Register (Offset:138h) to 1b.

4.9 Suspension

TC6387XB executes buffer-off for Input Signals from Host interface and SD Card by asserting #SUSPEND.



* Phase I: Immediately after the power is turned ON, #PCLR indicates "L" whereas #SUSPEND indicates "H". All the circuits are cleared in this state.
* Phase II: Assertion of #PCLR deactivated (H). Normal state.
* Phase III: Assert #SUSPEND to activate SUSPEND state. TC6387XB executes Anti-Penetration Process for Input Signals in this state. Also, TC6387XB does not accept Host Interface transactions in this state. Moreover, stopping HCLK can reduce the power consumption.
* Phase IV: TC6387XB is brought back to normal state by deactivating assertion of #SUSPEND.

It shows what state each signals are in suspend mode (#SUSPEND=Low).

NAME	Pin	IO	State	NAME	Pin	IO	State
HD15	H5	IO	Hi-Z	#HCS	A5	I	Hi-Z
HD14	F4	IO	Hi-Z	#HOE	G3	I	Hi-Z
HD13	G5	IO	Hi-Z	#HWE	G4	I	Hi-Z
HD12	F5	IO	Hi-Z	#HBEL	H4	I	Hi-Z
HD11	H6	IO	Hi-Z	#HBEH	H3	I	Hi-Z
HD10	G6	IO	Hi-Z	HRDY	F2	O (OD)	Hi-Z
HD9	H7	IO	Hi-Z	SDCD3	C2	IO	Hi-Z
HD8	H8	IO	Hi-Z	SDCD2	C3	IO	Hi-Z
HD7	G8	IO	Hi-Z	SDCD1	D3	IO	Hi-Z
HD6	F6	IO	Hi-Z	SDCD0	E1	IO	Hi-Z
HD5	F7	IO	Hi-Z	SDCMD	D2	IO	Hi-Z
HD4	E7	IO	Hi-Z	SDCLK	D1	O	L
HD3	F8	IO	Hi-Z	#SDCD	E2	I	-
HD2	E8	IO	Hi-Z	SDWP	E3	I	-
HD1	D8	IO	Hi-Z	SDLED	F1	O	Hi-Z
HD0	E6	IO	Hi-Z	SDPWR	B1	O	*
HA11	D7	I	Hi-Z	HCLK	H1	I	-
HA10	D6	I	Hi-Z	CLK32	A1	I	-
HA9	C8	I	Hi-Z	#HINT	G1	O (OD)	Hi-Z
HA8	C7	I	Hi-Z	#PCLR	F3	I	-
HA7	B8	I	Hi-Z	#SUSPEND	A4	I	-
HA6	A8	I	Hi-Z	TST2	B3	I	-
HA5	A7	I	Hi-Z	TST1	A3	I	-
HA4	C6	I	Hi-Z	TST0	C4	I	-
HA3	B6	I	Hi-Z	RSV0	A2	I	-
HA2	B5	I	Hi-Z	RSV1	B4	I	-
HA1	A6	I	Hi-Z	RSV2	C5	I	-

***** This signal is not controlled by #SUSPEND signal. The state before suspend mode (#SUSPEND=high) is held.

4.10 Pull-up/down Resistance

PULL- UP/DOWN Resistance is to be installed for each interface in TC6387XB. Be aware that Resistance Values (described "Res. Val." in the following tables) indicated in the following tables are provided only for references.

4.10.1 Host Interface

NAME	Pin	IO	Pull-up/ Pull-down	Pull-up Power	Res. Val.	FUNCTION/REMARKS
HRDY	F2	O (OD)	Pull-up	VCC	10KΩ	Ready

4.10.2 SD Card Interface

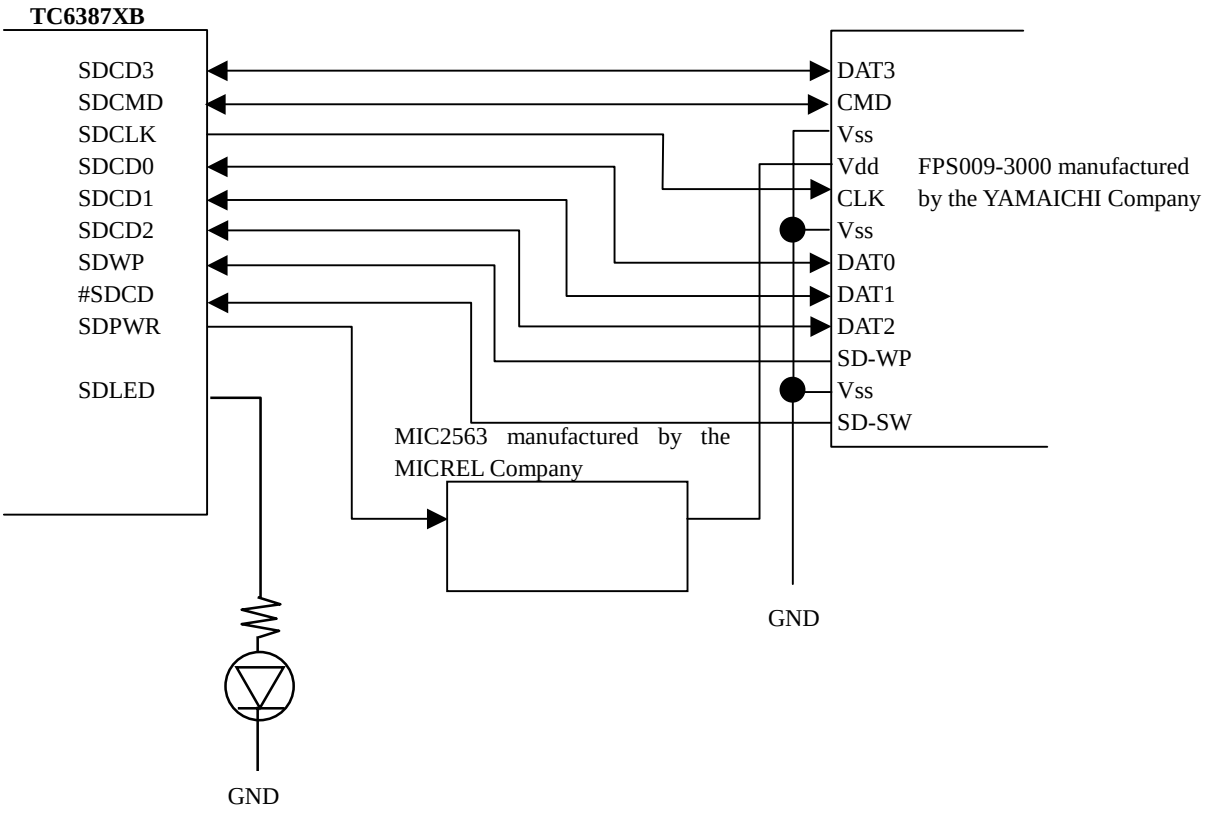
NAME	Pin	IO	Pull-up/ Pull-down	Pull-up Power	Res. Val.	FUNCTION/REMARKS
SDCD3	C2	IO	Pull-up	SDVCC	47KΩ	SD Card Slot /Data Bus
SDCD2	C3		Pull-up	SDVCC	100KΩ	
SDCD1	D3		Pull-up	SDVCC	100KΩ	
SDCD0	E1		Pull-up	SDVCC	100KΩ	
SDCMD	D2	IO	Pull-up	SDVCC	*1 : 33KΩ *2 : 100KΩ	SD Card Slot /Command *1 : Support MultiMedia Card *2 : Do not support MultiMedia Card
SDCLK	D1	O	-	-	-	SD Card Slot /Divided HCLK Clock
#SDCD	E2	I	Pull-up	VCC	10KΩ	SD Card Slot /Detection
SDWP	E3	I	Pull-up	VCC	10KΩ	SD Card Slot /Write Protection

4.10.3 System Interface

NAME	Pin	IO	Pull-up/ Pull-down	Pull-up Power	Res. Val.	FUNCTION/REMARKS
#HINT	G1	O (OD)	Pull-up	VCC	10KΩ	Interruption

4.11 Connection example of SD Card socket

It is shown that total 10 signal connections example of TC6387XB which have 9 signals of SD card interface and 1 signal of a power supply control for SD card. As for our company, using FPS009-3000 of theYAMAICHI Company did a movement confirmation of the SD card. An outside pull-up/down resistance that is mentioned on an item of the "4.10 Pull-up/down resistance" is not shown in a bottom figure. When you design a circuit, please refer to recommended resistance by an item of the "4.10 Pull-up/down " and a bottom figure.



5 Electrical Characteristic

5.1 Absolute Maximum Standard

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Condition	Note
Vcc	Supply Voltage Range	-0.3	5.0	V	GND=0V	1
Vin3	Input Voltage (3.3V)	-0.3	Vcc+0.3	V	GND=0V	
Vout	Output Voltage	-0.3	Vcc+0.3	V	GND=0V	
Tstg	Storage Temperature Range	-40	125	degree C		

Note 1: Vcc Power Supply

Note: Absolute Maximum Ratings indicates that stress greater than the values described above might cause permanent damages to the devices and does not guarantee all the performances within Absolute Maximum Ratings

5.2 DC Characteristic

5.2.1 Recommended Conditions for proper performances

Symbol	Parameter	Min	Typ	Max	Unit	Note
Vcc	Supply Voltage for Core Logic	3.0	3.3	3.6	V	
Topr	Ambient Temperature under bias	0	25	70	degree C	

5.2.2 Host Interface DC Characteristic

Host Interface DC Characteristic(Vcc =3.0-3.6V, Ta=0-70degree C)

Symbol	Parameter	Min	Max	Unit	Condition	Note
Vih	Input High Voltage	0.8Vcc	-	V		1-1
Vil	Input Low Voltage	-	0.2Vcc	V		1-1
Iilk	Input Leakage Current	-10	10	uA	0<Vin<Vcc	1-1
Voh	Output High Voltage	2.4	-	V	Iout=-4mA	1-2
Vol	Output Low Voltage	-	0.4	V	Iout=4mA	1-2

Note1-1: Applied for HD[15-0] ,HA[11-1], #HCS, #HOE, #HWE, #HBEL, #HBEH pins

Note1-2: Applied for HD[15-0], HRDY pins

5.2.3 SD Card Interface Pin DC Characteristic

SD Card Interface DC Characteristic: 3.3V Operation
(Vcc =3.0-3.6V, Ta=0-70degree C)

Symbol	Parameter	Min	Max	Unit	Condition	Note
Vih	Input High Voltage	0.7Vcc	Vcc+0.3	V		2-1
Vil	Input Low Voltage	Vss-0.3	0.175Vcc	V		2-1
Vih	Input High Voltage	0.8Vcc	-	V		2-2
Vil	Input Low Voltage	-	0.2Vcc	V		2-2
Voh1	Output High Voltage 1	0.75Vcc	-	V	Iout=-1mA 3.0V<Vcc<3.6V	2-3
Vol1	Output Low Voltage 1	-	0.125Vcc	V	Iout=1mA 3.0V<Vcc<3.6V	2-3
Voh2	Output High Voltage 2	2.4	-	V	Iout=-4mA	2-4
Vol2	Output Low Voltage 2	-	0.4	V	Iout=4mA	2-4
Iilk	Input Leakage Current	-10	10	uA	0<Vin<Vcc	2-1 2-2
Rdat3	Pull-up resistance inside card (pin1)	10	90	KΩ		

Note2-1 Applied for SDCD[3:0], SDCMD, SDWP pins

Note2-2 Applied for #SDCD pin

Note2-3 Applied for SDCD[3:0], SDCMD, SDCLK pins

Note2-4 Applied for SDLED pin

5.2.4 SD Card Power Supply Control DC Characteristic

SD Card Power Supply Control DC Characteristic: 3.3V Operation
(Vcc =3.0-3.6V, Ta=0-70degree C)

Symbol	Parameter	Min	Max	Unit	Condition	Note
Voh	Output High Voltage	2.4	-	V	Iout=-100uA 3.0V<Vcc<3.6V	2-5
Vol	Output Low Voltage	-	0.6	V	Iout=100uA 3.0V<Vcc<3.6V	2-5

Note2-5 Applied for SDPWR pin

5.2.5 System Interface Pin DC Characteristic

System Interface Pin DC Characteristic
(VCC =3.0-3.6V, Ta=0-70degree C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
Vih	Input High Voltage	0.8Vcc	-	V		3-1
Vil	Input Low Voltage	-	0.2Vcc	V		3-1
Iilk	Input Leakage Current	-10	10	uA	0<Vin<Vcc	3-1
Voh	Output High Voltage	2.4	-	V	Iout=-4mA	3-2
Vol	Output Low Voltage	-	0.4	V	Iout=4mA	3-2

Note3-1 Applied for HCLK, CLK32, #PCLR, #SUSPEND pins

Note3-2 Applied for #HINT pin

5.2.6 TEST Pin DC Characteristic

TEST Pin DC Characteristic
(Vcc =3.0-3.6V, Ta=0-70degree C)

Symbol	Parameter	Min	Max	Unit	Condition	Note
Vih	Input High Voltage	0.8Vcc	-	V		4-1
Vil	Input Low Voltage	-	0.2Vcc	V		4-1
Iilk	Input Leakage Current	-10	10	μA	0<Vin<Vcc	4-1

Note4-1 Applied for TST[2:0] pins

5.2.7 Power Consumption Characteristic

Power Supply Current

Symbol	Parameter	Min	Typ	Max	Unit	Condition
Iccstd 1	Power Supply Current, Standby				uA	HCLK=0, CLK32=0 VCC=3.6V #SUSPEND=low
Iccstd 2	Power Supply Current Standby				uA	HCLK=0, CLK32=32KHz VCC=3.6V #SUSPEND=low
IccSD/MMC	Power Supply Current, Operating SD Card or MultiMedia Card				mA	HCLK=33MHz, CLK32=32KHz VCC=3.6V

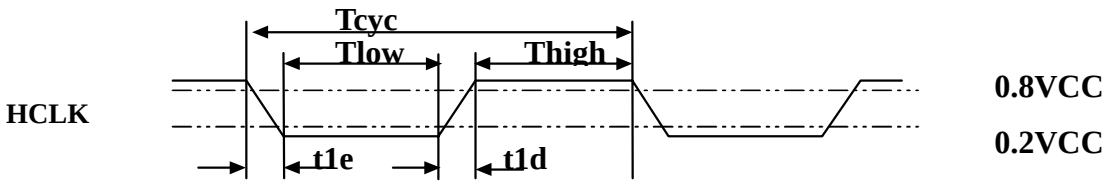
5.3 AC Characteristic

5.3.1 Host Interface Signal AC Characteristic

(1)System Clock AC Characteristic
(Vcc=3.0-3.6V, Ta=0-70degree C)

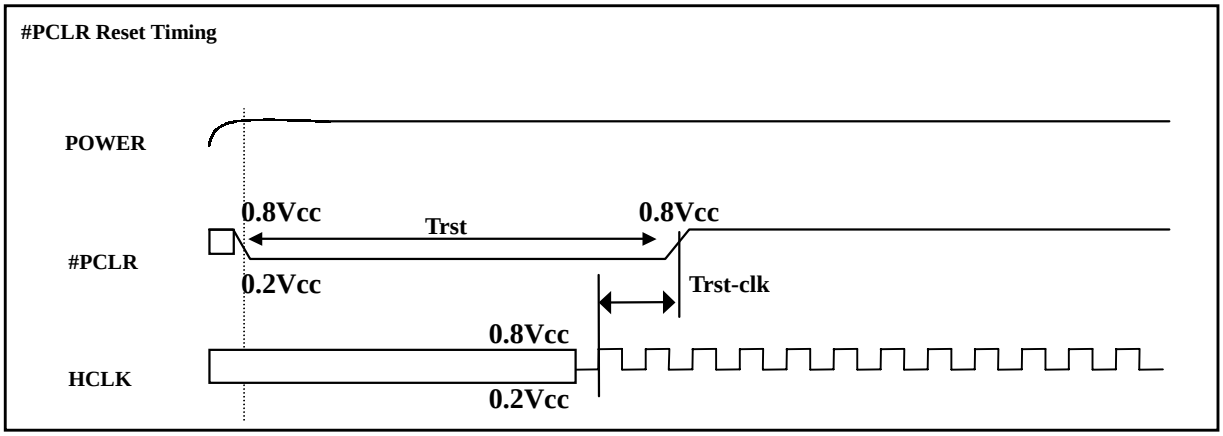
Symbol	Parameter	Min	Max	Unit	Notes
	HCLK				
Tcyc	CLK cycle time	30	∞	ns	
Thigh	CLK High time	10	-	ns	
Tlow	CLK Low time	10	-	ns	
t1d	HCLK Rising Time	-	5	ns	
t1e	HCLK Falling Time	-	5	ns	

HCLK Timing



(2)#PCLR Reset AC Characteristic
(Vcc=3.0-3.6V, Ta=0-70degree C)

Symbol	Parameter	Min	Max	Unit	Notes
	#PCLR				
Trst	Reset active time after power stable	1		ms	
Trst-clk	Reset active time after CLK stable	1		ms	



#PCLR Reset Timing

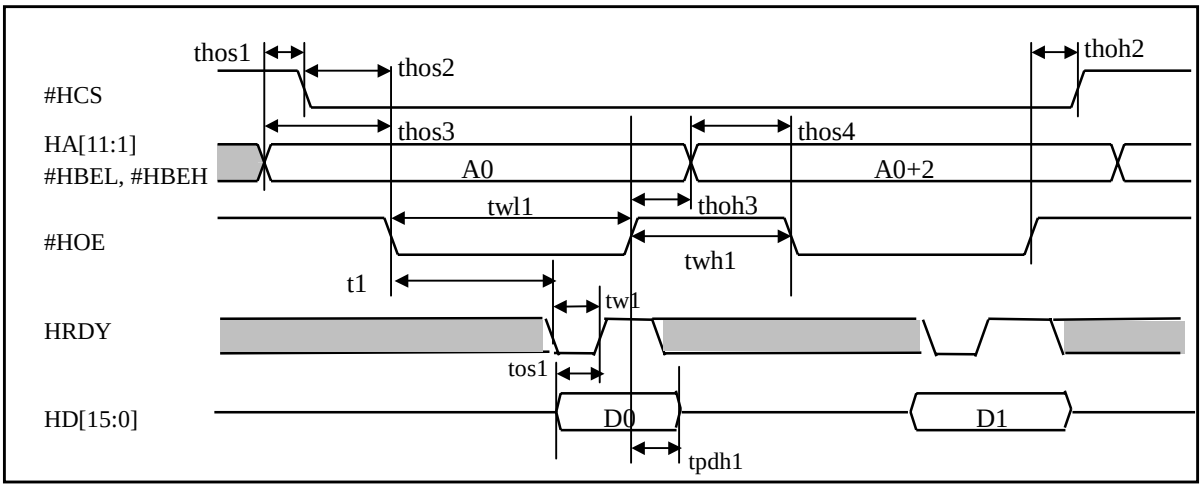
(3)Standard Memory Interface Signal AC Characteristic
(Vcc=3.0-3.6V,Ta=0-70degree C)

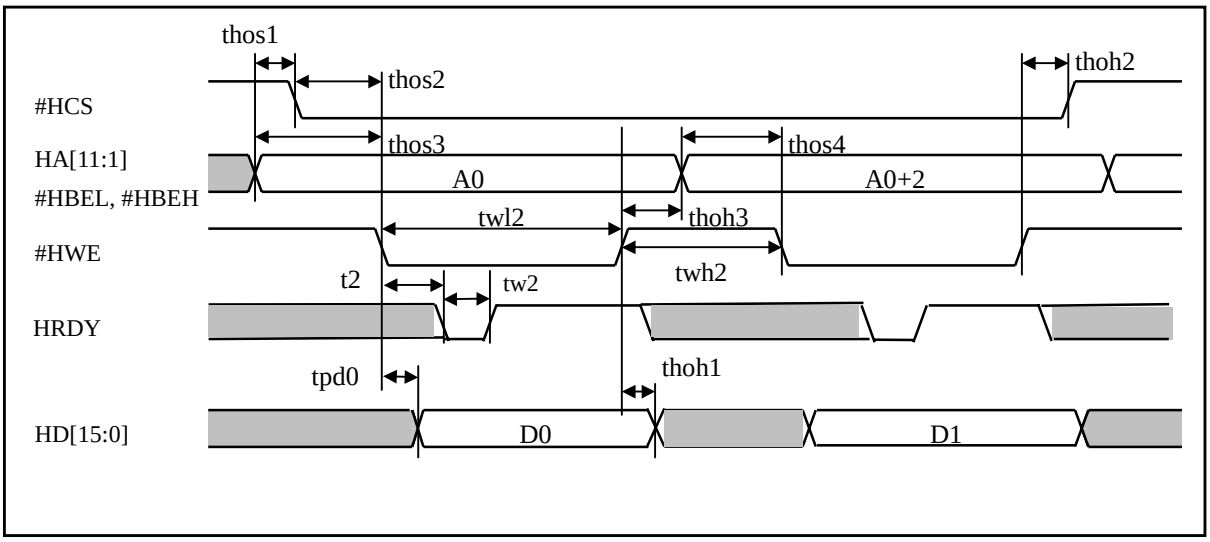
Symbol	Parameter	Min	Max	Unit	Notes
thos1	Address setup to #HCS	0	-	ns	
thos2	#HCS, #HBEL, #HBEH setup to #HOE or #HWE	20	-	ns	
thos3	Address setup to #HOE or #HWE low	20	-	ns	
thos4	Address setup to #HOE or #HWE low	20	-	ns	
tpd0	Data delay time after #HWE low	-	1HCLK	ns	
thoh1	Data hold after #HWE high	5	-	ns	
thoh2	#HCS, #HBEL, #HBEH hold asserted after #HOE or #HWE de-asserted	10	-	ns	
thoh3	Address Hold after #HOE or #HWE de-asserted	5	-	ns	
twh1	#HOE high time	3HCLK	-	ns	
twh2	#HWE high time	3HCLK	-	ns	
twl1	#HOE low time	3HCLK	-	ns	*1
twl2	#HWE low time	3HCLK	-	ns	*1
tos1	Data Setup for HRDY Release	1HCLK	-	ns	
tpdh1	#HOE,HD[15:0] hold time	5	-	ns	
t1	#HOE low to HRDY low time	15	-	ns	
t2	#HWE low to HRDY low time	15	-	ns	
tw1	HRDY low time	1HCLK	-	ns	
tw2	HRDY low time	1HCLK	-	ns	

*1 There are two ways to have wait modes.

A. External wait mode method(ie. not to use CPU generated wait time):
Please input #HOE/#HWE signal using pulse width of 3HCLK minimum. If this has been applied, HRDY of TC6380AF signal will be activated and read/write cycle will be extended to access registers. By this method, read/write access cycle will become 16HCLK maximum.

B. Internal wait mode method(ie. use CPU generated wait time):
Please input #HOE/#HWE signal using enough pulse width, which should be 16HCLK minimum. If this has been applied, HRDY signal is not necessary for TC6380AF register read/write operations.

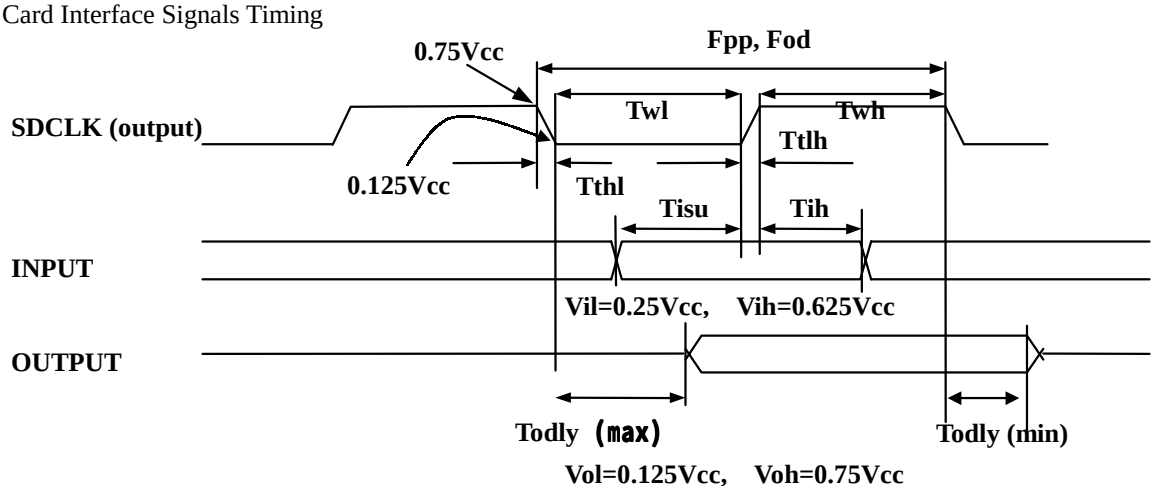

thos1
thos2
thoh2
#HCS
HA[11:1]
#HBEL, #HBEH
thos3
thos4
A0
A0+2
twl1
thoh3
#HOE
twh1
t1
tw1
HRDY
tos1
HD[15:0]
D0
D1
tpdh1


thos1
thos2
thoh2
#HCS
HA[11:1]
#HBEL, #HBEH
thos3
thos4
A0
A0+2
twl2
thoh3
#HWE
twh2
t2
tw2
HRDY
tpd0
thoh1
HD[15:0]
D0
D1

5.3.2 SD Card Interface Signal AC Characteristic
(Vcc=3.0-3.6V, Ta=0-70degree C)

Symbol	Parameter	Min	Max	Unit	Notes
	SDCD[3:0], SDCMD, SDCLK				
Fpp	Clock frequency Data Transfer Mode	0	25	MHz	Cl=25pF
Fod	Clock frequency Identification Mode	0	256	KHz	Cl=25pF
Twl	Clock Low time	10	-	ns	Cl=25pF
Twh	Clock High time	10	-	ns	Cl=25pF
Ttlh	Clock fall time	-	10	ns	Cl=25pF
Tthl	Clock rise time	-	10	ns	Cl=25pF
Tisu	Input set-up time	10	-	ns	Cl=25pF
Tih	Input hold time	10	-	ns	Cl=25pF
Todly	Output delay time	-	15	ns	Cl=25pF

SD Card Interface Signals Timing



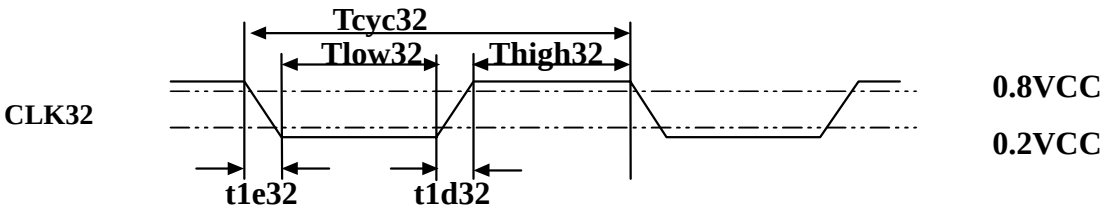
Timing for SD Card Interface Signals

5.3.3 System Interface Signal AC Characteristic
(Vcc=3.0-3.6V, Ta= 0-70degree C)

CLK32 AC Characteristic
(Vcc=3.0-3.6V, Ta=0-70degree C)

Symbol	Parameter	Min	Max	Unit	Notes
	CLK32				
Tcyc32	CLK cycle time	31	∞	us	
Thigh32	CLK High time	11	-	us	
Tlow32	CLK Low time	11	-	us	
t1d32	CLK32 Rising Time	10	-	ns	
t1e32	CLK32 Falling Time	10	-	ns	

CLK32 Timing



6 Caution in coding device driver

6.1 Regarding a SD card insertion and removal

If a SD card would be inserted or removed, you should perform software reset with SD Software Reset Register(Offset:0E0h, 1E0h).

*In SD card insertion

If a SD card would be inserted, you should perform software reset with SD Software Reset Register(Offset:0E0h, 1E0h). Then, you should release software reset and initialize a SD card.

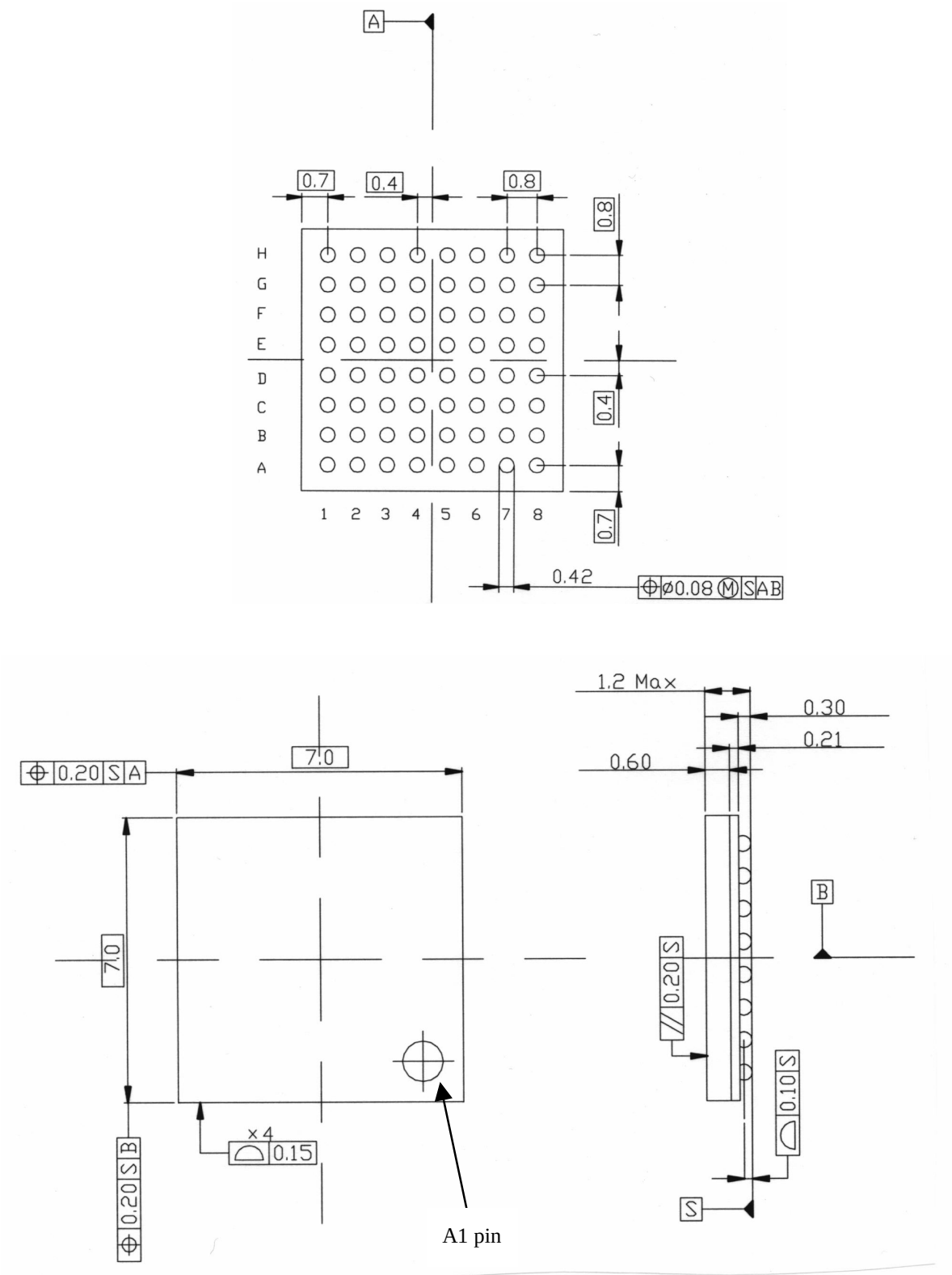
*In SD card removal

If a SD card would be removed, you should perform software reset with SD Software Reset Register(Offset:0E0h, 1E0h). Afterward, when a SD card would be inserted, you should release software reset and initialize a SD card.

6.2 Regarding controlling Stop Clock Control Register

Stop Clock Control Register(Config Offset:40h) is used to control internal clocks of TC6387XB. When you would set this register, you could not set different values between EMCK3 bit(D2) and EMCK1 bit(D0).

7 Package outline

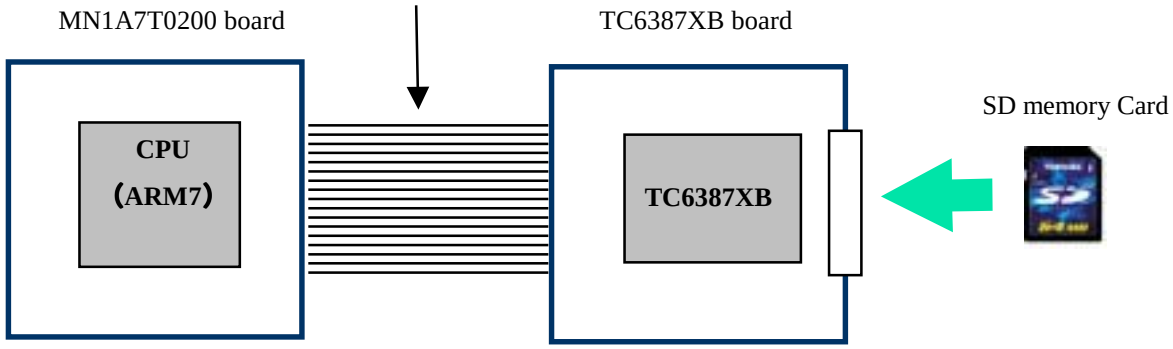


Appendix

A TC6387XB function confirmation with standard memory interface

TOSHIBA connected TC6387XB board to MN1A7T0200 board manufactured the COMPUTEX corporation. Then , TOSHIBA confirmed to the function of SD memory Card and MMC. The following indicates these circuits.

Standard memory interface connection



A.1 Sample soft for standard memory interface of TC6387XB

TOSHIBA developed the device driver of SD memory Card with above environment. TOSHIBA provide these driver source to you as sample soft of TC6387XB.

A.2 Wait mode specification

MN1A7T0200 board and TC6380A board support internal and external wait mode of 32/16/8 bit access. The correspondence list indicates as followings.

	MN1A7T0200 board	TC6387XB specification	TC6387XB board	Notes
32bit internal wait mode	Support	Not support	Not support	*1
16bit internal wait mode	Support	Support	Support	
8bit internal wait mode	Support	Support	Support	
32bit external wait mode	Support	Not support	Not support	*1
16bit external wait mode	Not support	Support	Support	*2
8bit external wait mode	Not support	Support	Support	*2

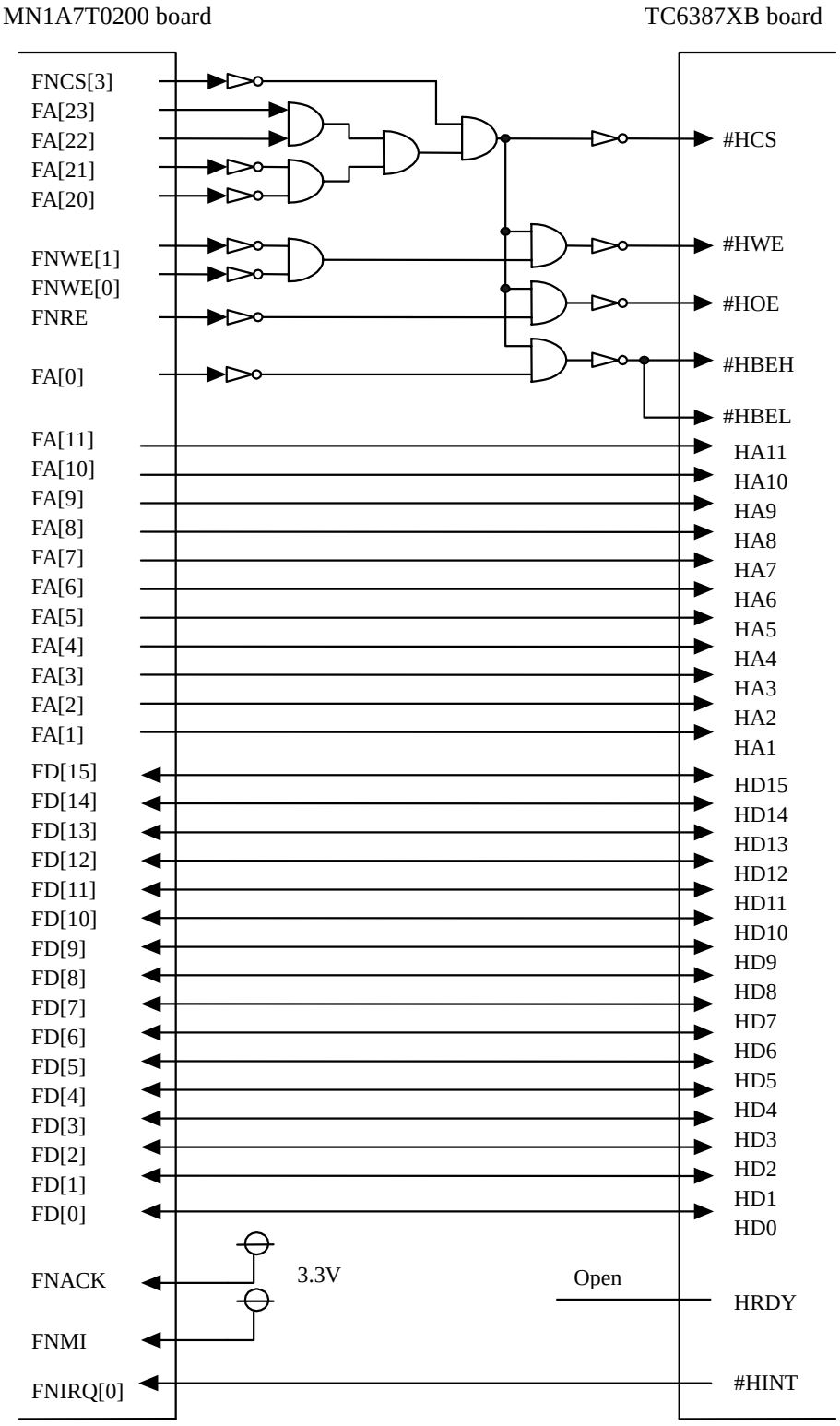
*1 Because TC6387XB supports 16 bit bus interface, TOSHIBA do not confirm this function.

*2 MN1A7T0200 board supports only external wait mode of 32 bit access. When TOSHIBA confirmed to the function of SD memory Card, SDIO Card and SmartMedia™ with external wait mode of 16bit and 8bit access, TOSHIBA deal with these mode by controlling #HCS, #HWE, #HRE, #HBEH, #HBEL, HA[11:1], HD[15:0] and HRDY with using FPGA LSI mounted to TC6387XB board. External wait access of 16 bit and 8 bit were realized by shifting address bits against external wait access of 32 bit from MN1A7T0200 board. These access(*3) can be switched by FPGA register.

*3 Internal wait access of 16 bit, external wait access of 16 bit and external wait access of 8 bit.

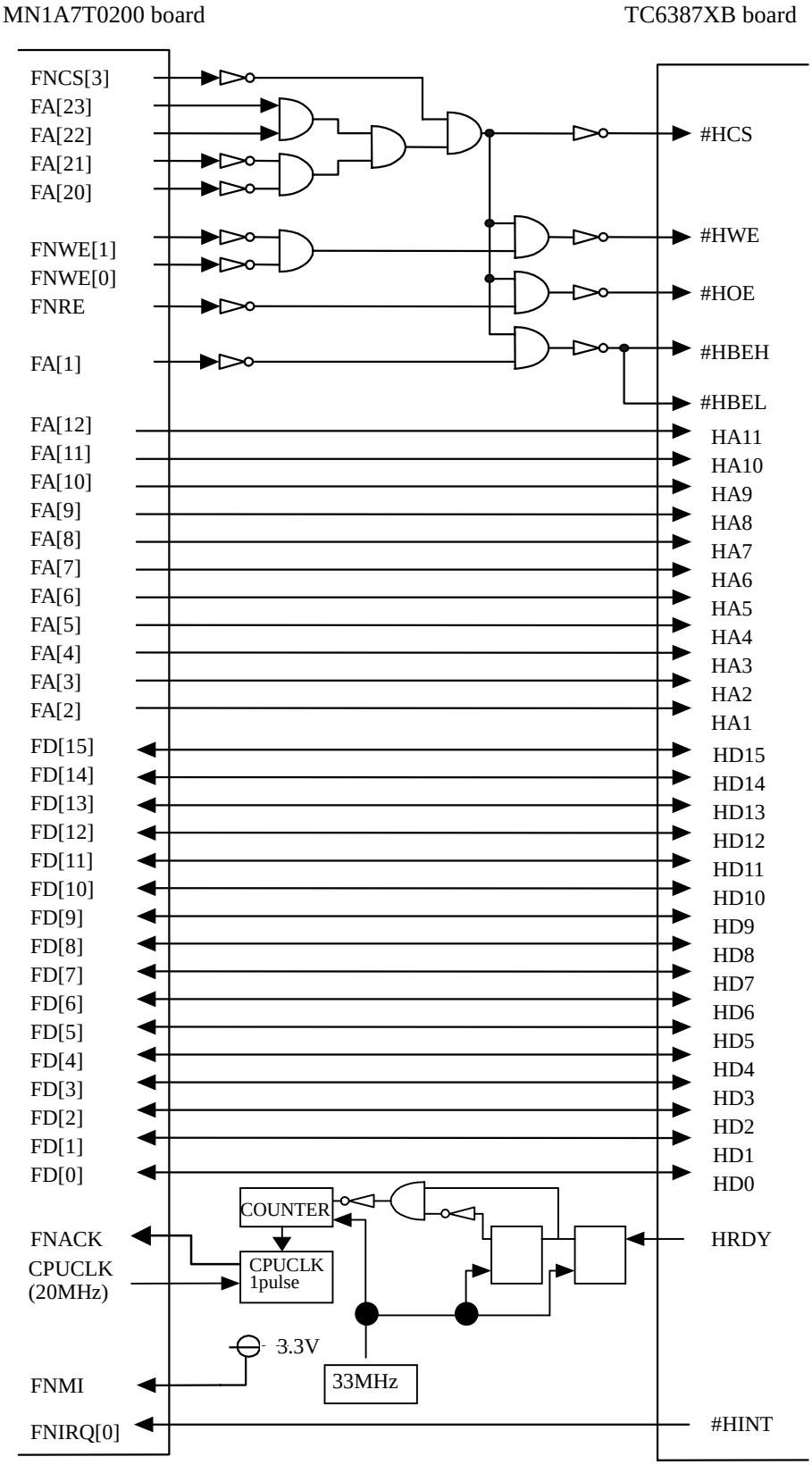
A.3 The wiring image of 16bit internal wait mode

In 16 bit internal wait mode, the connection of MN1A7T0200 board and TC6387XB is as following.



A.4 The wiring image of 16bit external wait mode

In 16 bit external wait mode, the connection of MN1A7T0200 board and TC6387XB is as following. MN1A7T0200 board access to TC6387XB board with 32 bit.



B Reference diagram