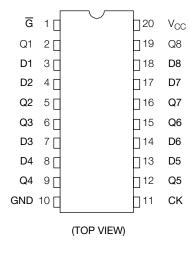
TC74AC Series TC74AC377

Features:

- High Speed: f_{MAX} = 140MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 8μA (max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min.)
- Symmetrical Output Impedance: II_{OH}I = I_{OL} = 24mA (min.). Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays: t_{DLH} = t_{DHL}
- Wide Operating Voltage Range: V_{CC} (opr.) = 2V~5.5V
- Pin and Function Compatible with 74F377
- Available in DIP, SOIC and SOP Packages

Pin Assignment



The TC74AC377 is an advanced high speed CMOS OCTAL D-TYPE FLIP-FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input (\overline{G}) .

The signal level applied to the D inputs are transferred to Q outputs during the positive going transition of CK.

When the \overline{G} is high, the eight outputs are in a high impedance state.

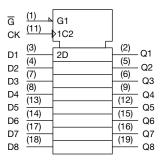
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Truth Table

	OUTPUT			
G	CLOCK	Q		
Н	Х	Х	NO CHANGE	
L		L	L	
L		Н	Н	
Х	7_	Х	NO CHANGE	

X: Don't care

IEC Logic Symbol



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Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT		
Supply Voltage Range	V _{CC}	-0.5~7.0	V		
DC Input Voltage	V _{IN}	-0.5~V _{CC} + 0.5	V		
DC Output Voltage	V _{OUT}	-0.5~V _{CC} + 0.5	V		
Input Diode Current	I _{IK}	±20	mA		
Output Diode Current	l _{OK}	±50	mA		
DC Output Current	I _{OUT}	±50	mA		
DC V _{CC} /Ground Current	Icc	±200	mA		
Power Dissipation	P_{D}	500 (DIP) */180 (SOP)	mW		
Storage Temperature	T _{stg}	-65~150	°C		
Lead Temperature 10sec	TL	300	°C		

^{* 500}mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{CC}	2.0~5.5	V
Input Voltage	V _{IN}	0~V _{CC}	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise and Fall Time	·		ns/v

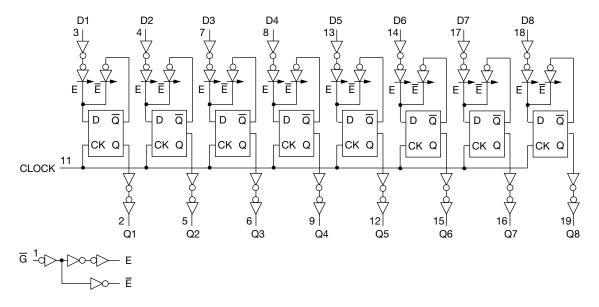
DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION V _{CC}			Ta = 25°C		Ta = -40~85°C		UNIT		
PANAMETEN	STWIDUL			Min.	Typ.	Max.	Min.	Max.	UNIT		
		_		2.0	1.50	<u> </u>	_	1.50	_	V	
High-Level Input Voltage	V _{IH}			3.0	2.10	_	_	2.10	_		
				5.5	3.85	_	_	3.85	_		
		_		2.0	_	_	0.50	_	0.50		
Low-Level Input Voltage	V _{IL}			3.0	_	_	0.90	_	0.90	V	
				5.5	_	_	1.65	_	1.65		
	V _{OH}	V_{OH} $V_{IN} = V_{IH}$ or V_{IL}	I _{OH} = -50μA	2.0	1.9	2.0	_	1.9	_	- V	
				3.0	2.9	3.0	_	2.9	_		
High-Level Output Voltage				4.5	4.4	4.5	_	4.4	_		
riigii-Levei Output voitage			I _{OH} = -4mA	3.0	2.58	_	_	2.48	_		
			I _{OH} = -24mA	4.5	3.94	_	_	3.80	_		
					I _{OH} = -75mA*	5.5	_	_	_	3.85	_
	V	$V_{IN} = V_{IH \text{ or }} V_{IL}$	I _{OL} = 50μA	2.0	_	0.0	0.1	_	0.1		
				3.0	_	0.0	0.1	_	0.1		
Low Lovel Output Voltage				4.5	_	0.0	0.1	_	0.1	\ _\ \	
Low-Level Output Voltage	V _{OL}		I _{OL} =12mA	3.0	_	_	0.36	_	0.44	V	
			I _{OL} = 24mA	4.5	_	_	0.36	_	0.44		
			I _{OL} = 75mA*	5.5	_	_	_	_	1.65		
Input Leakage Current	I _{IN}	$V_{IN} = V_{CC}$ or GND		5.5	_	_	±0.1	_	±1.0		
Quiescent Supply Current	I _{CC}	$V_{IN} = V_{CC}$; or GND	5.5	_	_	8.0	_	80.0	μΑ	

 $^{^{\}star}$ This spec indicates the capability of driving 50 Ω transmission lines. One output should be tested at a time for a 10ms maximum duration.

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System Diagram



Timing Requirements (Input $t_r = t_f = 3n$)

PARAMETER	OVERDOL	TEST CONDITION		Ta=25°C		Ta= −40~85°	UNIT
	SYMBOL TEST CONDITION		V _{CC}	Тур.	Max.	Max.	
Minimum Pulso Width (CK)	Minimum Bulgo Width (CK)		3.3±0.3	_	8.0	8.0	
Minimum Pulse Width (CK)	t _{W(H)}	_	5.0±0.5	_	5.0	5.0	
Minimum Set-up Time (D–CK)	t _{W(L)}	_	3.3±0.3	_	8.0	8.0	1
			5.0±0.5	_	4.0	4.0	
Minimum Set-up Time (G–CK) t _s			3.3±0.3	_	9.0	9.0	ns
	ι _S	_	5.0±0.5	_	4.0	4.0	
Minimum Hold Time			3.3±0.3	_	1.0	1.0	
	ι _h	_	5.0±0.5	_	1.0	1.0	

AC Electrical Characteristics (C $_{L}$ = 50pF, R $_{L}$ = 500 $\!\Omega,$ Input t_{r} = t_{f} = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -4	UNIT	
		TEST CONDITION	V _{CC}	Min.	Typ.	Max.	Min.	Max.	ONII
Propagation Delay Time (CK-Q)	t _{pLH}		3.0±0.3	_	10.6	17.6	1.0	20.0	no
	t _{pHL}	_	5.0±0.5	_	7.4	10.6	1.0	12.0	ns
Maximum Clock Frequency	f		3.0±0.3	50	95	_	50	_	MHz
	T _{MAX}	_	5.0±0.5	80	140	_	80	_	IVIIIZ
Input Capacitance	C _{IN}	_	_	_	5	10	_	10	25
Power Dissipation Capacitance	C _{PD} ¹	_	_	_	30	_	_	_	- pF

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC \text{ (opr)}} = C_{PD} \bullet V_{CC} \bullet f_{\text{IN}} + I_{CC} / 8 \text{ (per F/F)}.$ And the total C_{PD} when n pcs. of Flip-Flop operate can be gained by the following equation: $C_{PD} \bullet V_{CC} \bullet f_{\text{IN}} + I_{CC} / 8 \text{ (per F/F)}.$

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