TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC8830F

C²MOS VOICE RECORDING/REPRODUCING LSI

TC8830F

11 July, 1986

Revision 1 June, 1987

[1] GENERAL

The TC8830F is a single chip C MOS LSI for voice recording and reproducing LSI using the ADM (Adpative Delta Modulation) system. Voice recording and reproducing can be made by externally connecting S-RAM for voice data recording.

- Features

(1) S-RAM is used to record voice data.
Maximum 4 units of 64 Kbit or 256 Kbit S-RAM can be connected directly.

(2) Recording and reproducing of up to 16 phrases are possible (at the manual control). At the CPU control, number of phrases can be further increased.

(3) Direct access to phrases (instantaneous reproducing of phrase heads) is possible.

(4) CPU control type and manual control type are selectable.

(5) 4 kinds of bit rates (32 Kbps, 16 Kbps, 11 Kbps, 8 Kbps) are selectable.

(6) A microphone is connectable directly as the microphone amplifier has been built in.

(7) Built-in band-pass filter for cutting unnecessary band of synthesized voice.

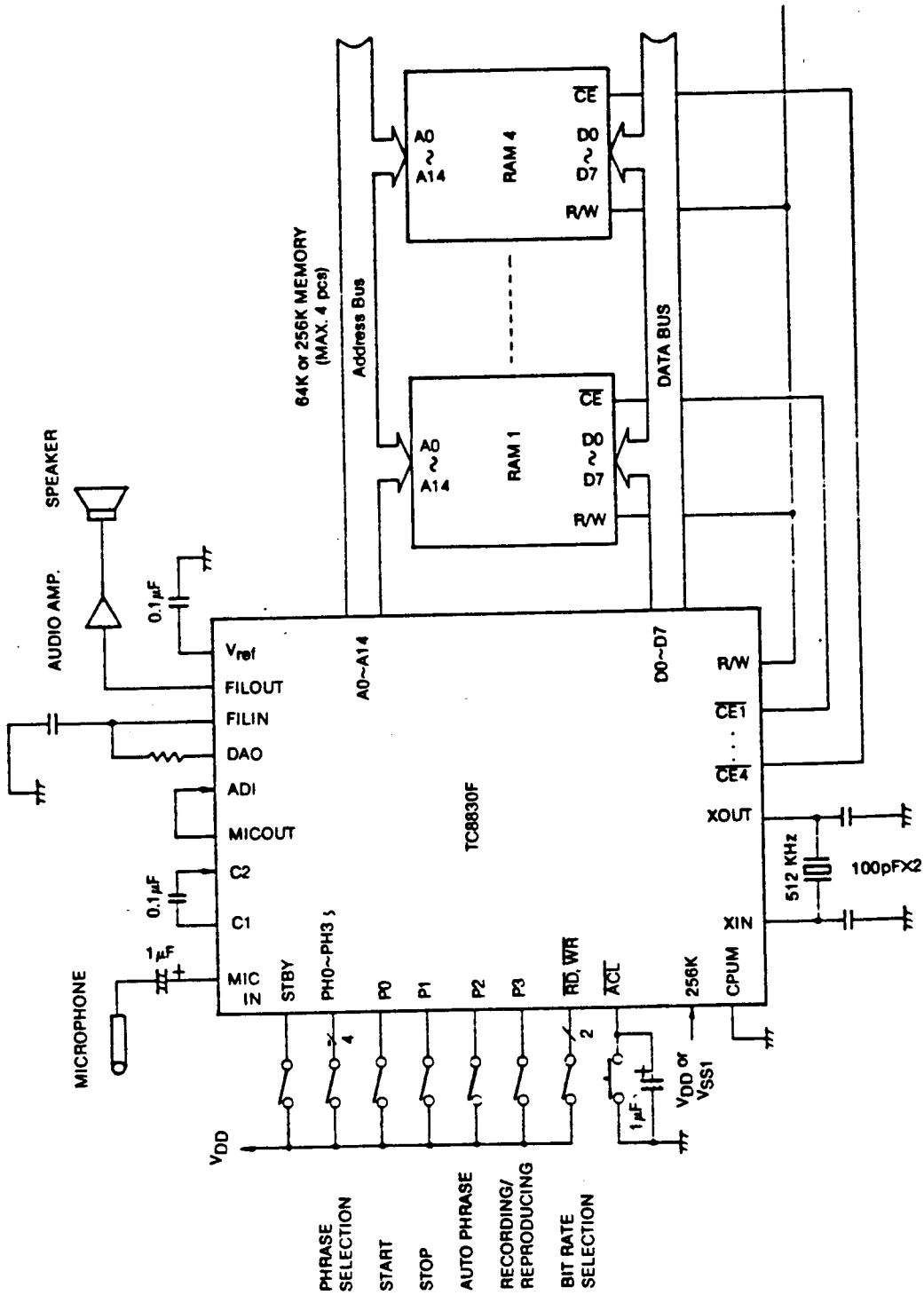
(3) Standby function making voice data reproducing possible.

(9) Built-in oscillation circuit for ceramic vibrator.

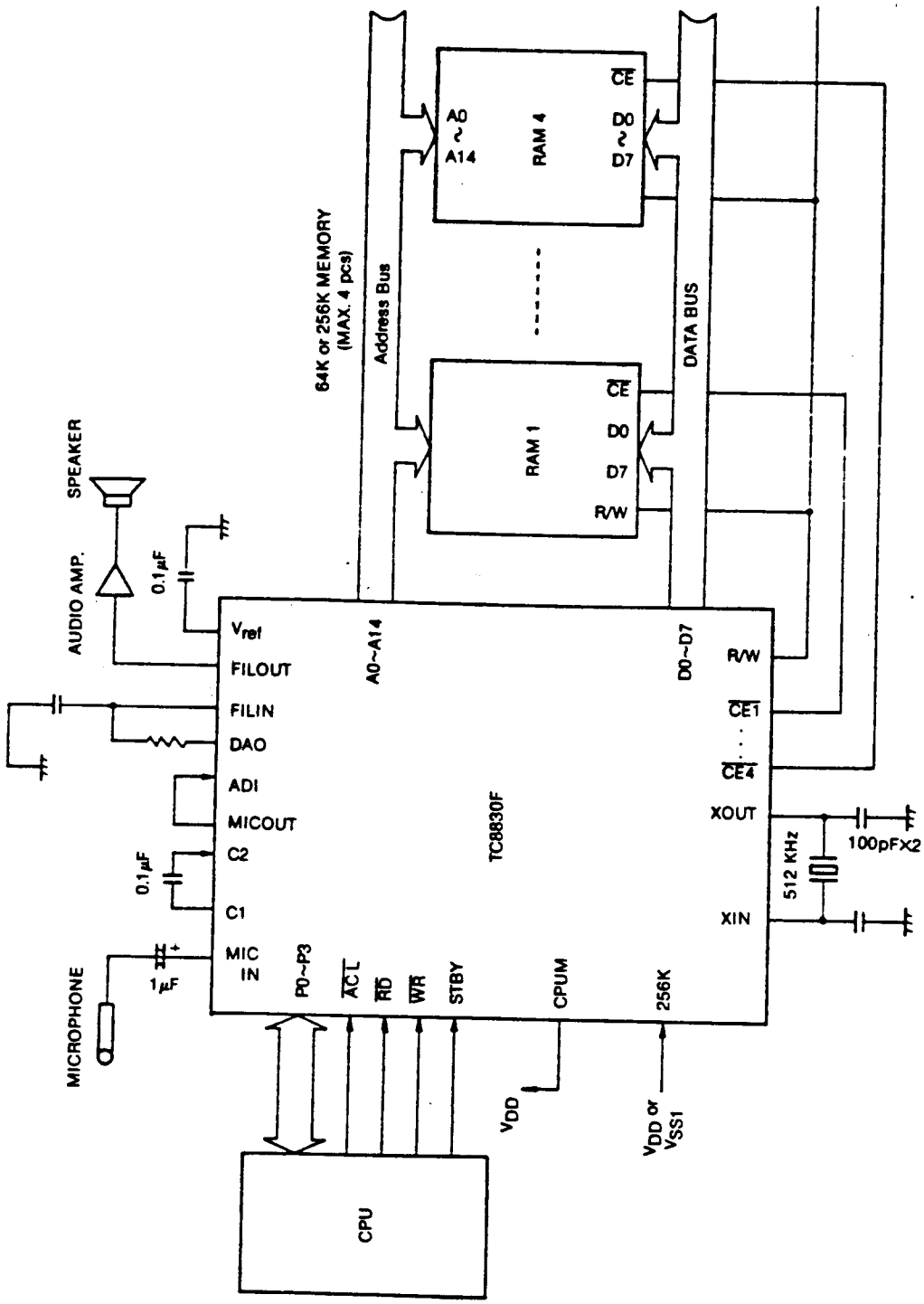
(10) 5V single power supply operation.

[2] EXAMPLE OF VOICE RECORDING/REPRODUCING DEVICE LSI SYSTEM CONFIGURATION

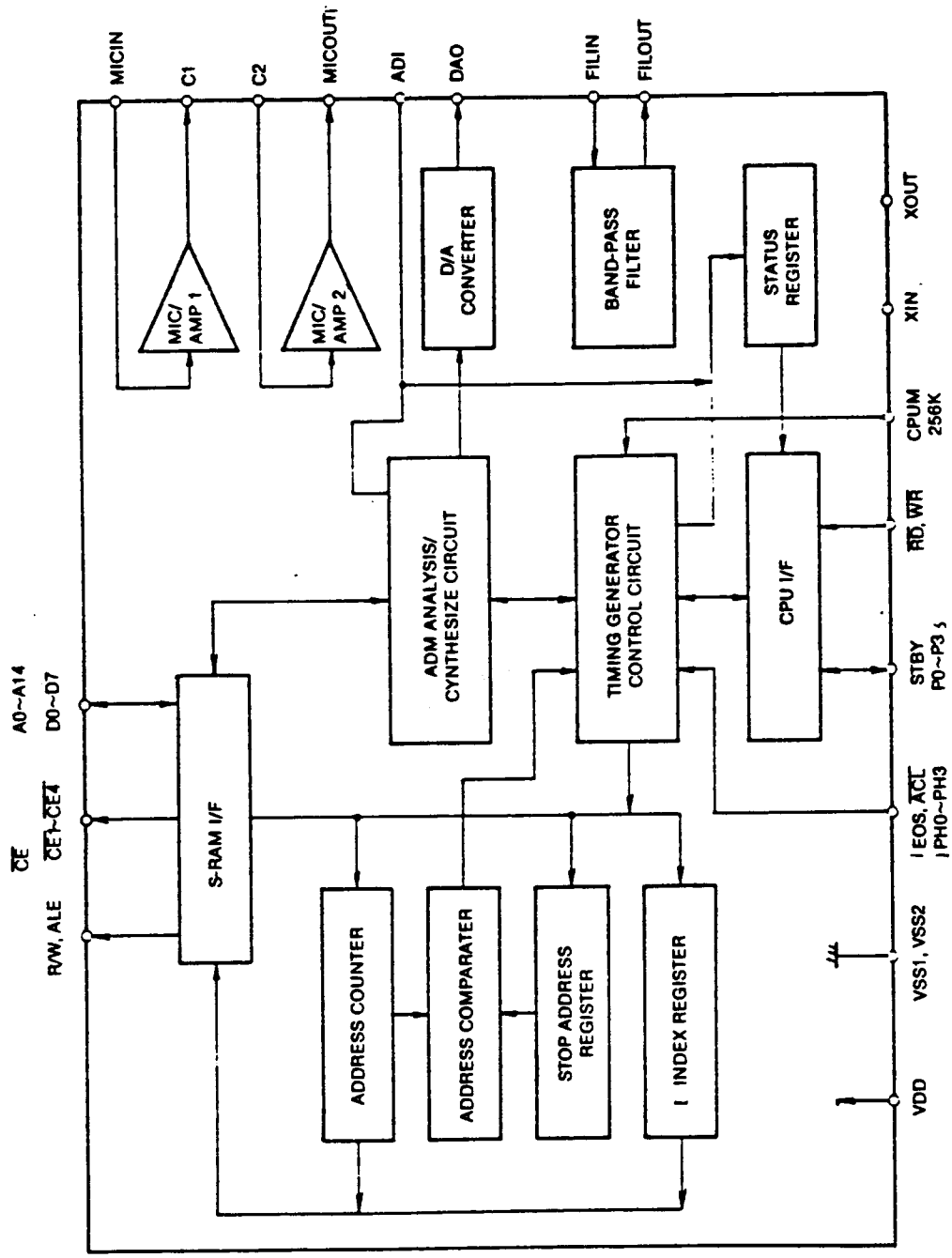
2.1 Example of manual control system configuration



2.2 Example of CPU control system configuration



[3] BLOCK DIAGRAM



3.1 Block diagram

Address counter	The 20-bit counter to show external S-RAM address. Address value is increased by one per 8 samplings during the recording and reproducing operations. At the CPU control, a value can be set by command and further, that value can also be read out.
Stop address register	The 20-bit register to show address to stop the recording operation and reproducing operation.
Address comparator	Detects matching of the address counter and the stop address register. When detected matching, directs stop of the address counter.
Index register	Shows address of the index area on S-RAM in the label index mode.
Status register	The 4-bit register showing the internal status. When RT pin is set to LOW level at time of the CPU control, contents of this register are output to P0 ∿ P3 pins.
CPU I/F	The interface circuit with external CPU or peripheral device I/O ports. Forther, this circuit contains the chattering preventive circuit which becomes valid only in the manual mode
S-RAM I/F	The interface circuit for externally connecting S-RAM.
Microphone Amp 1	The microphone amplifier for directly connecting.
Microphone Amp 2	A microphone. Output from the microphone amplifier defects around analog reference voltage (Vref).
Band-pass filter	The band-pass filter to cut off unnecessary bands at reproducing. This filter consists of a primary high-pass filter and a secondary low-pass filter.

[4] SPECIFICATION

Voice analyzing/ synthesizing system	ADM (Adpative Delta Modulation) system
Bit rate	32 Kbps/16 Kbps/11 Kbps/8 Kbps
Number of maximum	In manual control ..... 16 In manual control (Auto phrase function) ..... 63 Direct mode in CPU control ..... No restriction Lable index mode in CPU control 63
Operating frequency	512 kHz (Typ.)

[5] OPERATIONAL DESCRIPTION

When composing a voice recording and reproducing system using the TC8830F, there are two controls; the manual control which perform the control by directly connecting switches, etc. and the CPU control which performs the control by connecting external CPU or I/O ports of peripheral device to the TC8830F.

5.1 Manual control (CPUM pin="L")

The input pins for controlling the TC8830F are 14 pins of P0, P1, P2, P3, $\overline{WR}$, $\overline{RD}$, PH0, PH1, PH2, PH3, STBY, CPUM, 256K and $\overline{ACL}$.

When the CPUM pin out of these pins is set at "L" level, the TC8830F is set at the manual control.

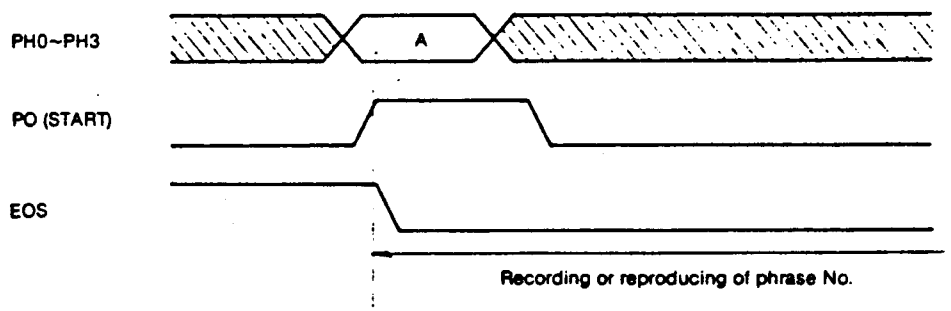
5.1.1 Selection of phrases

16 phrases from phrase No. 0 to phrase No. 15 can be recorded by setting 4 input pins of PH0 ∿PH3. Likewise, the direct access (instantaneous reproducing of phrase heads) reproducing of 16 phrases from phrase No. 0 to phrase No. 15 by setting 4 input pins of PH0 ∿PH3. In addition, recording and reproducing up to 63 phrases are possible by using the auto-phrase function which is described later.

Selection of Phrases

Phrase No. \ Pin name	MSB PH3	PH2	PH1	LSB PH0
No. 0	0	0	0	0
No. 1	0	0	0	1
No. 2	0	0	1	0
↓	↓	↓	↓	↓
No.15	1	1	1	1

1="H" level
0="L" level



[Note] When recording multiples number of phrases, set up phrase Nos. in order of smaller numbers as shown in example 1.

Example 1 ○
- No.0 → No.1 → No.2 → No.3
- No 2 → No.4 → No.15

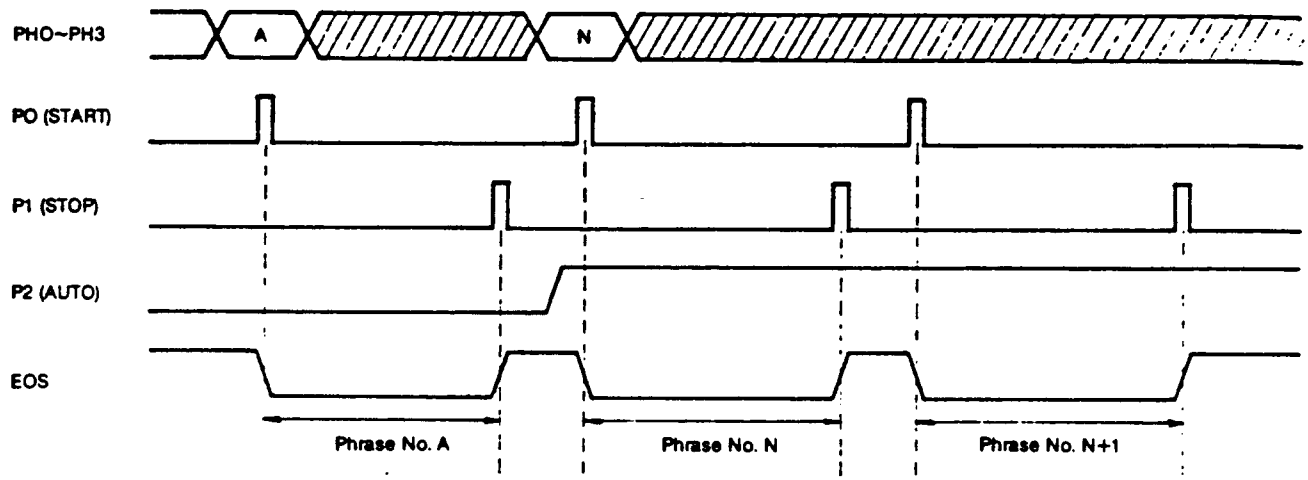
Example 2 ×
- No.15 → No.14 → No.13 → No.12
- No.0 → No.4 → No.1

Further, when reproducing recorded phrases, desired phrases can be reproducing as many as desired in any order.

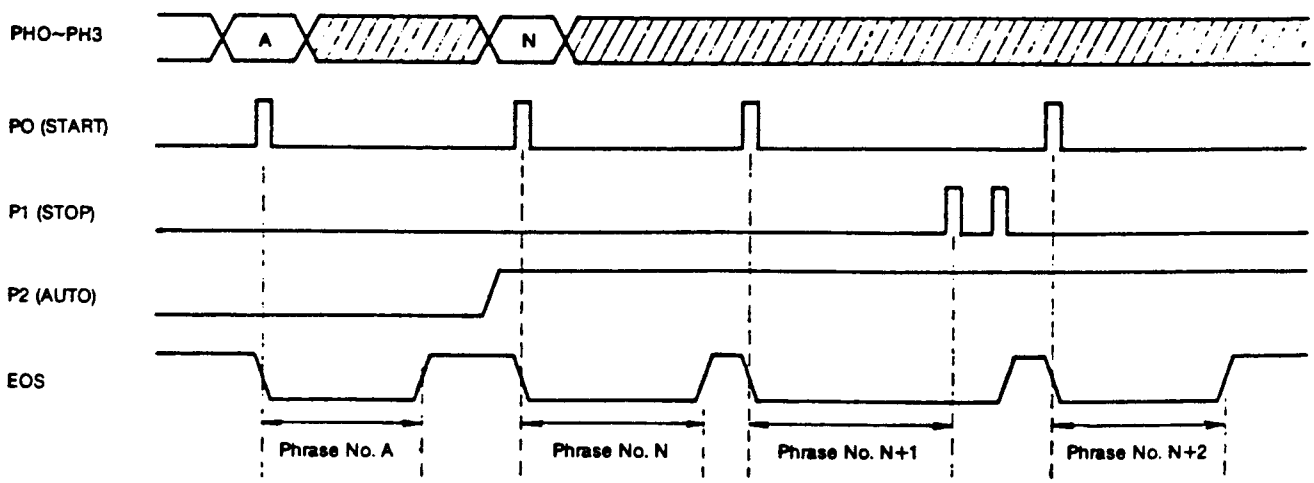
5.1.2 Auto-phrase function P2 (AUTO) pin="H"

Phrase No. can be increased automatically by one at a time when P2 pin is set to "H" level. At this time, initial value of phrase No. is decided by phrase No. shown by PH0 ~ PH3 pin when P2 pin is changed from "L" level to "H" level.

Recording Mode P3(REC)="H"



Reproducing Mode P3(REC)="L"



[NOTE] 1: When P2 pin is at "H" level, setup of PH0 ~ PH3 pin has no meaning.

2: Setup of phrases by the auto-phrase function is valid from phrase No. 0 to phrase No. 62. If phrases in excess of phrase No. 62 are recorded, erroneous data are recorded on RAM. Therefore, be careful not to record phrases by exceeding phrase No. 62.

3: Direct access reproducing (instantaneous reproducing of phrase heads) is not possible for phrases from phrase No. 16 through phrase No. 62.

5.1.3 Selection of bit rates

Bit rate is selectable from 4 kinds; 32Kpbs, 16Kbps, 11Kbps and 8Kbps by setting up the $\overline{RD}$ and $\overline{WR}$ pins.

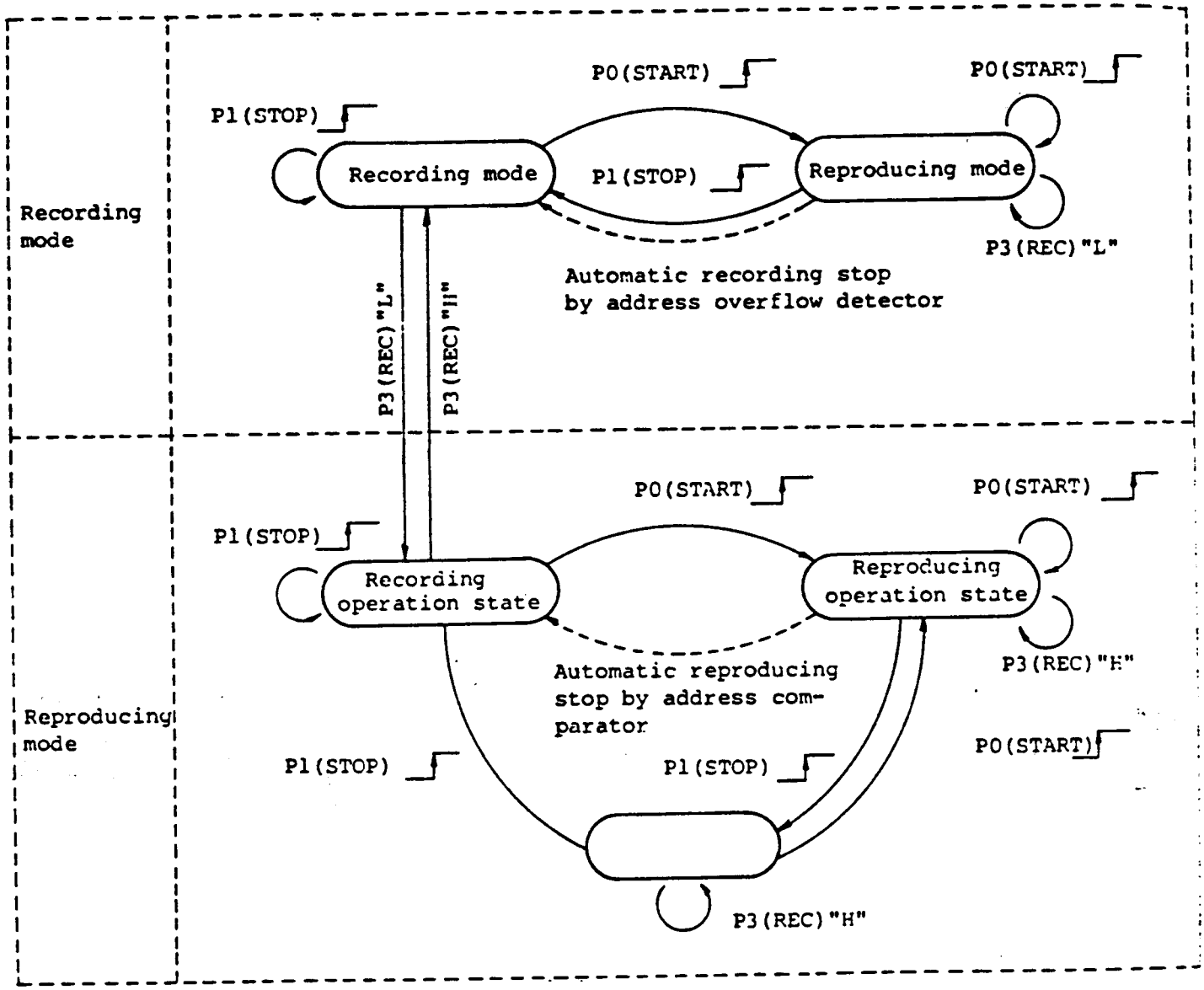
Selection of bit rate

Bit rate	Division Ratio from original oscillation	$\overline{WR}$	$\overline{RD}$
8K bps	64	0	0
11K	48	0	1
16K	32	1	0
32K	16	1	1

0 ... "L" level
1 ... "H" level

[NOTE] The $\overline{WR}$ and $\overline{RD}$ pins should be set up before starting the recording/reproducing, and under the state of recording/reproducing operations, they should be kept in HOLD data.

5.1.4 Status change at manual control



5.1.5 Setting up recording mode, reproducing mode

The recording and reproducing are changed over by the P3 pin.

The TC8830F if set in the recording mode when the P3 pin is at "H" level and in the reproducing mode at "L" level.

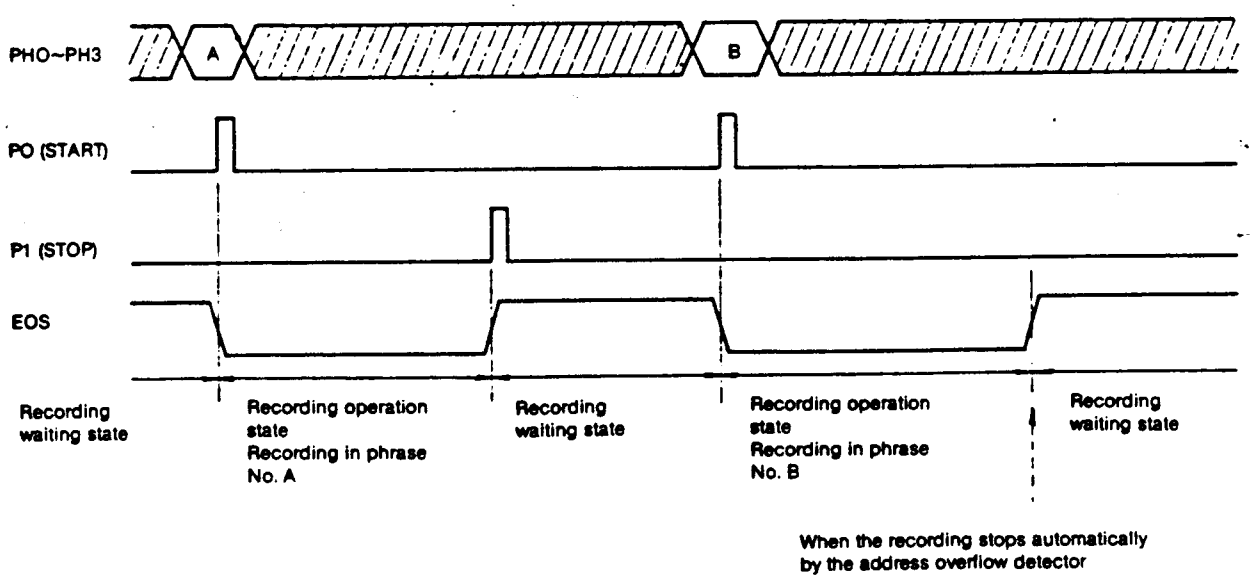
5.1.6 Recording P3(REC) pin="H"

When the P0 pin is set to "H" level in the recording mode, the recording starts. During the recording state, the TC8830F writes voice analysis data onto external RAM. Addresses at this time are controlled by the internal address counter.

To halt the recording, set the P1 pin to "H" level. This ends the recording of one phrase. When multiple phrases are to be recorded, refer to 5.1.2 "Selection of Phrases".

Further, when the address counter reaches the final address of RAM in the recording state, the recording is stopped automatically by the address overflow detector which is built in the TC8830F. Though the final address of RAM differs depending upon number of RAMs to be connected, the TC8830F copes with automatically.

P3(REC)="H"



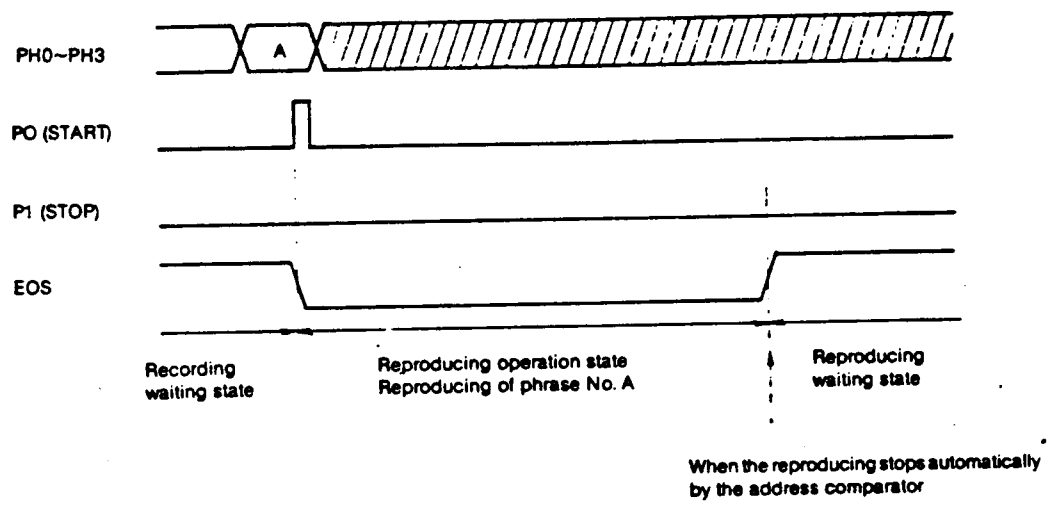
[NOTE] • During the recording operation, input to the P0 pin is not accepted.

• When the address overflow detector detects the final address of RAM and stops the recording automatically, the recording operation cannot be started unless the TC8830F is initialized by the ACL input.

5.1.7 Reproducing P3(REC) pin="L"

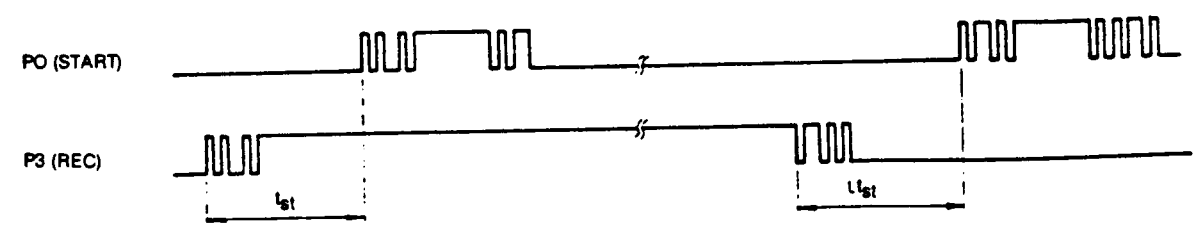
When the P0 pin is changed over to "H" level from "L" level in the reproducing mode, the reproducing starts. Under the reproducing operation state, the TC8830F reads data, which were analyzed and recorded in the recording state, from external RAM, synthesizes and reproduces voices. When reproducing of one phrase ends, the TC8830F is places automatically in the reproducing waiting state for reproducing next phrase. Further, when selecting phrases to be reproduced, refer to "5.1.2 selection of phrases".

P3(REC)="L"



[NOTE] • During the reproducing operation, input to the P0 pin is not accepted.

• When the recording operation and the reproducing operation starts, there is the following restriction between the P0 pin input and the P1 input.

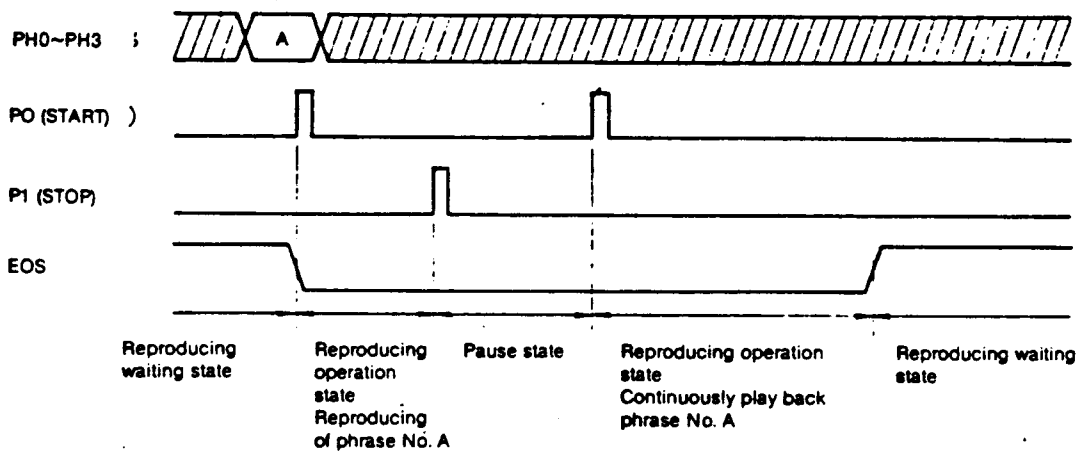


$t_{st} \geqq 32$ ms (f_{OSC}=512kHz)

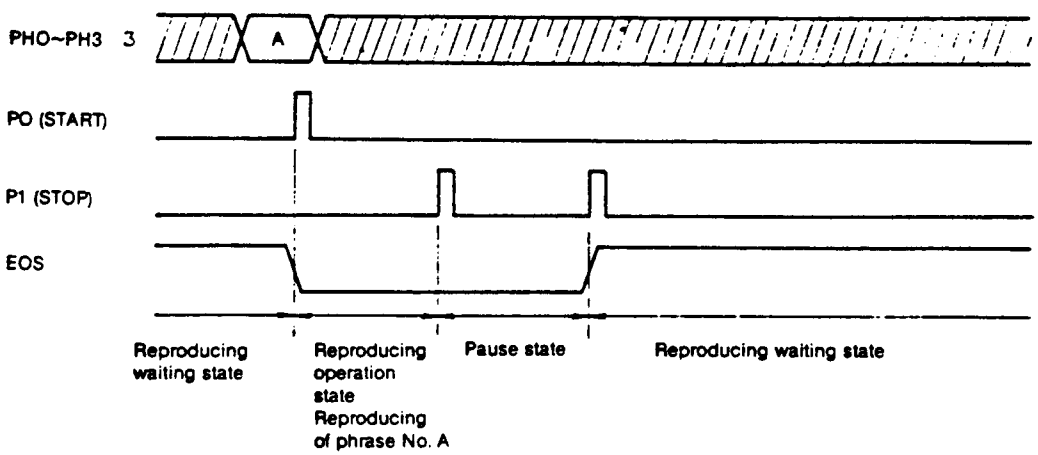
5.1.8 Pause function

In the reproducing mode it is possible to pause the reproducing during the reproducing operation by setting the P1 pin to "H" level. To reproduce the paused phrase continuously, set the P0 pin to "H" level. Further, if the P1 pin is once more set at "H" level in the pause state, the TC8830F is ready to accept the reproducing operation.

P3(REC)="L"



P3(REC)="L"



5.1.9 Recording/reproducing time

Recording/reproducing time is determined by type and quantity of RAMs to connected to the TC8830F and bit rate.

Recording/reproducing time

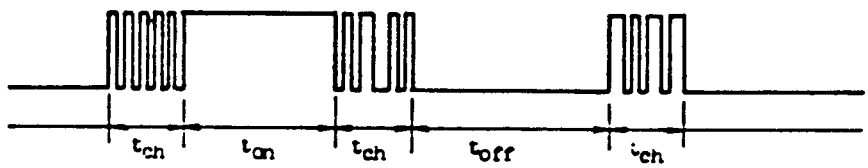
External RAM \ Recording/reproducing time	Recording/reproducing time (sec)			
	Bit rate			
	32Kpbs	16Kbps	11Kbps	8Kbps
64K S-RAM 1 pc	2	4	6	8
2 pcs	4	8	12	16
3 pcs	6	12	18	24
4 pcs	8	16	24	32
256K S-RAM 1 pc	8	16	24	32
2 pcs	16	32	48	64
3 pcs	24	48	72	96
4 pcs	32	64	96	128

Maximum 4 units of 64K S-RAM of 256K S-RAM can be connected directly to the TC8830F. To connect 64K S-RAM, set the 256K pin at "L" level, and to connect 256K S-RAMs, fix the 256K pin at "H" level.

[NOTE] • In the recording operation and reproducing state, do not change the level of the 256K pin.

5.1.10 Chattering preventive circuit

To prevent the malfunction by chattering of switches connected to the P0 ∿ P3 pins at the manual control, the chattering preventive circuit acts. The chattering preventive time is about 64ms (f_{osc}=512kHz).



$t_{ch} \leqq 64$ ms $\quad t_{on} \geqq 64$ ms $\quad t_{off} \geqq 64$ ms

(f_{osc} = 512 kHz)

5.2 CPU control [CPUM Pin="H"]

When the CPUM pin is set at "H" level, the TC8830F is set at the CPU control, the operation of the TC8830F can be controlled by 11 kinds of commands using the P0 ∿ P3, $\overline{RD}$ and $\overline{WR}$ pins. At this time, there are 2 kinds of control modes; the direct mode in which the start and end addresses of the address counter are set up by commands and the label index mode in which this address setting is performed by the TC8830F itself. Further, the built-in 4-bit status register allows to read the status of the TC8830F externally as required.

[NOTE] In the recording operation and reproducing state, do not change the level of the CPUM pin.

5.2.1 Explanation of commands

List of commands

Command Name	Code PPPP 3210	Functions
NOP	0001	Sets up the reproducing mode. In addition, resets OVER bit of the status register.
START	0010	Starts the recording or reporducing operation in the direct mode from the address shown by the address counter.
STOP	0010	Stops the recording or reproducing operation. When this command is input to stop the recording started by the LABEL command, an operation to write a value of the address counter at time of the stop into the index area of RAM is performed. Further, when this command is input during the reproducing by the LABEL command, the pause state is resulted. When the START command is input successively, the TC8830F is placed in the reproducing state and input of the STOP command puts the TC8830F in the reproducing waiting state.
ADLD1	0100	Sets address in the address counter by 5 nibble data following this command. After executing this command, the TC8830F is placed in the display waiting state.
CNDT	0110	Designates bit rate and validity/invalidity of the address overflow detector by 1 nibble data following this command. After executing this command, the TC8830F is placed in the display waiting state.
LABLE	0111	Designating phrase No. (0 ~ 62) by 2 nibble data following this command, starts the recording/reproducing. Input of this command in the recording mode writes contents of the address counter into the index area of RAM and then, starts the recording. In case of the reproducing mode, starts the reproducing after reading start address and stop address from the index area of RAM.

ADRD	1000	Reads out contents of the address counter by 4 bits at a time in turn from the lower order by 5 successive read accesses. During this period, contents of the status register cannot be read. After executing this command, the TC8830F is ready to accept the reproducing operation.
REC	1001	Sets up the recording mode.
DTRD	1010	Reads data out of RAM by 2 successive read accesses. Readout address at this time is shown by the address counter. Further, this command does not change the address counter value. After executing this command, the TC8830F is ready to accept the reproducing operation.
DTWR	1011	Writes successive 2-nibble data onto RAM. Write address at this time is shown by the address counter. Further, this command does not change the address counter value. After executing this command, the TC8830F is ready to accept the reproducing operation.

[NOTE] 1) Do not input other codes than those shown on the list of commands (0000, 1100, 1101, 1110 and 1111).

2) During the recording operation as well as the reproducing operation, do not input other commands than the stop command.

Command Data Format

Command	1st nibble PPPP 3210	2nd nibble PPPP 3210	3rd nibble PPPP 3210	4th nibble PPPP 3210	5th nibble PPPP 3210	6th nibble PPPP 3210
NOP	0001	———	———	———	———	———
START	0010	———	———	———	———	———
STOP	0011	———	———	———	———	———
ADLD1	0100	A3 A2 A1 A0	A7 A6 A5 A4	A11 A10 A9 A8	A15 A14 A13 A12	A19 A18 A17 A16
ADLD2	0101	A3 A2 A1 A0	A7 A6 A5 A4	A11 A10 A9 A8	A15 A14 A13 A12	A19 A18 A17 A16
CNDT	0110	0 C BR1 BR0	———	———	———	———
LABEL	0111	PH3 PH2 PH1 PH0	X X PH5 PH4	———	———	———
ADRD	1000	A3 A2 A1 A0	A7 A6 A5 A4	A11 A10 A9 A8	A15 A14 A13 A12	A19 A18 A17 A16
RLC	1001	———	———	———	———	———
DTRD	1010	D3 D2 D1 D0	D7 D6 D5 D4	———	———	———
DTWR	1011	D3 D2 D1 D0	D7 D6 D5 D4	———	———	———

[NOTE] CNDT Command data

Bit rate setting

Bit rate	P1 (BR1)	P0 (BR0)
8K bps	0	0
11K bps	0	1
16K bps	1	0
32K bps	1	1

Selection as to whether the address overflow detector performs the automatic recording stop by detecting the final address of RAM.

Auto recording stop	P3	P2 (C)
Performs	0	1
Not performs	0	0

(Does not set P3 at "1")

5.2.2 Change of internal blocks

Internal block		ACL Input	Command input											Instruction according to internal block	
		ACL	NOP	START	STOP	ADLD1	ADLD2	COND	LABEL	ADRD	REC	DTRD	DTWR	Address comparator	Address overflow detector
Index register		R							S					*1 (+1)	
Address counter		R → S (100H)		START	STOP	S			S START					STOP	*2 (STOP)
Stop address register		R					S		S						
Address over-flow detector		ENABLE						ENABLE/ DISABLE							
Bit rate register		R (8K bps)						S							
REC mode flag		R	R			R	R	R		R	S	R	R		
EOS		S		R	S									S	*2 (C)
Status register	OVER flag	R	R												*2 (C)
	EOS flag	R		S	R									R	*2 (R)

S : SET
R : RESET
START: Address counter starts increment
STOP: Address counter stops increment
No entry: No change

*1. In the recording operation in the direct mode, address of the index area shown by the index register is increased by one phrase when the recording is stopped automatically by the address comparator.

*2. Becomes valid when the address overflow detector is enabled by the COND command.

[NOTE] Operation of address counter

Setting of start address	Direct mode ..... Start address is set up by the ADLD1 command. Label index mode ... In the recording mode, a value when the LABEL command is input becomes the start address. In the reproducing mode, the start address recorded in the index area of RAM is automatically set up.
Start	Direct mode ..... Started by the START command. Label index mode ... Started by the LABEL command.
Increment	Address is increased by one per 8 samplings.
Stop	Direct mode ..... Stops automatically when the address comparator detected match of the stop address register with the address counter. Label index mode ... In the recording mode, stops when the STOP command is input. When the address comparator detected match of the stop address register with the address counter. Common to direct mode and label index mode ..... When the address overflow detector detects RAM end in the recording mode, stops automatically.

5.2.3 Control in direct mode

The direct mode is a control mode to set start address and end address of the address counter by commands.

——— Recording in direct mode ———

(1) Set start address in the address counter by the ADLD1 command (Fig. 1).

(2) Set end address in the stop address register by the ADLD3 command (Fig. 2).

(3) Set the TC8830F in the recording mode by the REC command.

(4) Start the recording by the START command. The contents of the address counter is increased and voice analysis data is written in the data area of S-RAM (Fig. 3).

The address comparator detects match of the address counter value with the stop address register value and automatically stops the recording. The address counter value at this time is written in the index area of S-RAM (Fig. 4).

[NOTE] Set up start address and end address so that voice analysis data is not written in the index area.

Fig. 1

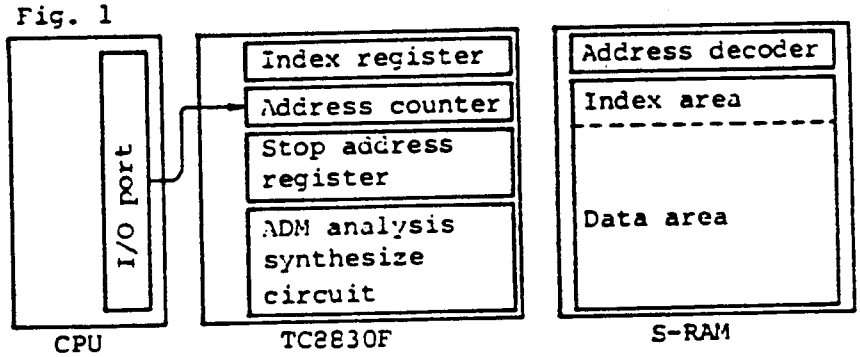


Fig. 2

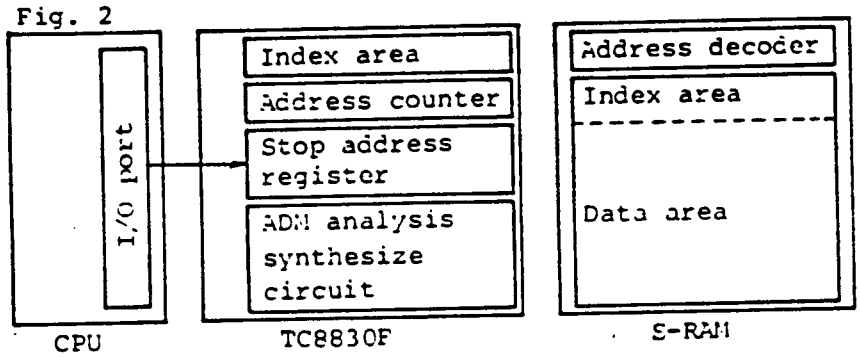


Fig. 3

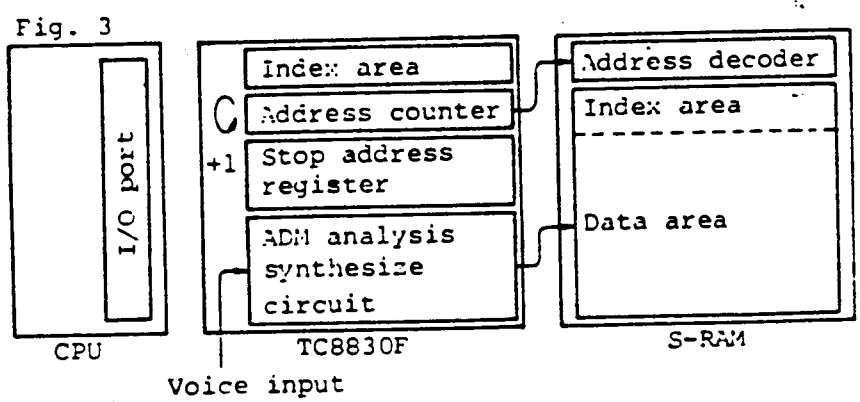
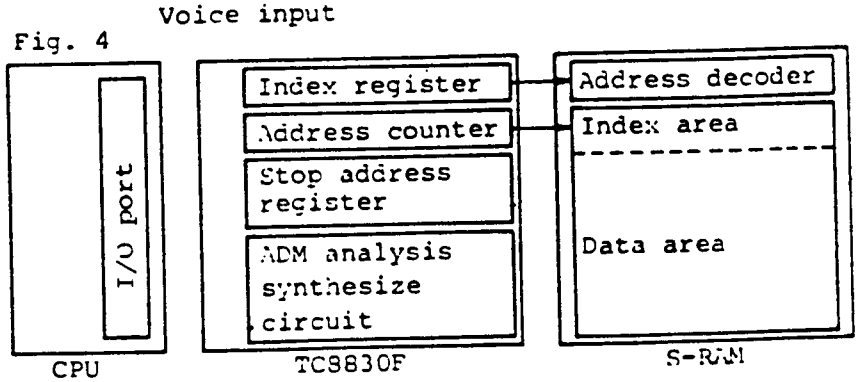


Fig. 4



— Reproducing in direct mode —

(1) Set start address in the address counter by the ADLD1 command (Fig. 1)

(2) Set end address in the stop address register by the ADLD2 command (Fig. 2)

(3) Start the reproducing by the START command. The contents of the address counter is increased and voice analysis data written in the data area of S-RAM is loaded. (Fig. 3)

The address comparator detects match of the address counter value with the stop address register value and automatically stops the reproducing.

Fig. 1

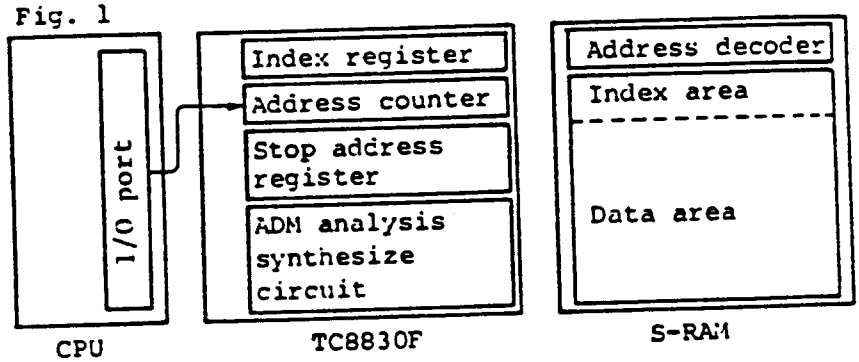


Fig. 2

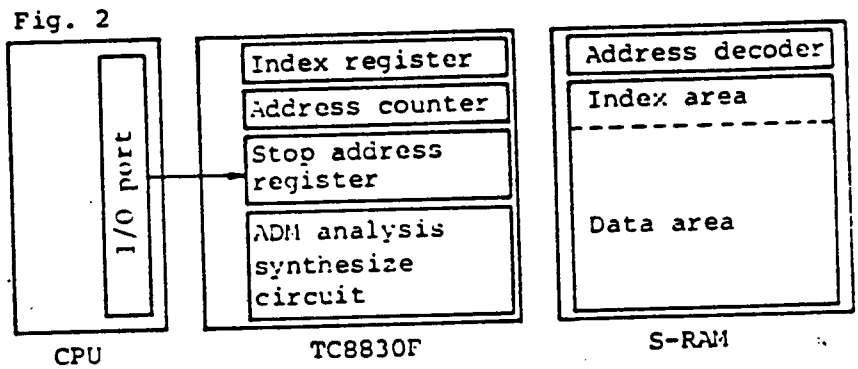
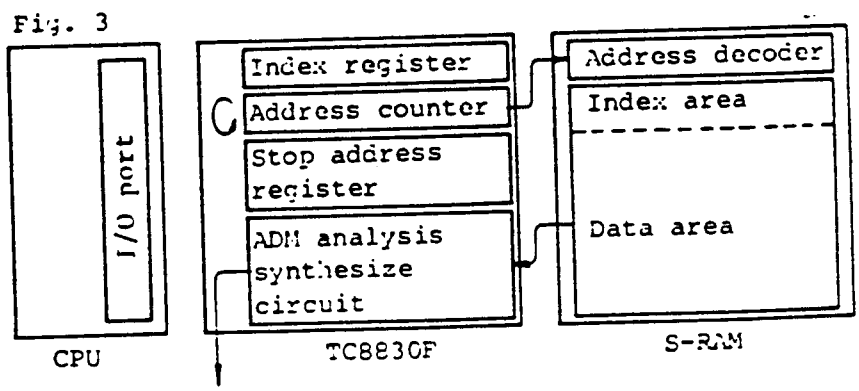


Fig. 3



[NOTE]

(1) Behavior of the index register in the direct mode.

When the recording of one phrase ends in the direct mode (when the address comparator detected match of the address counter value and the stop address register value and automatically stopped the recording), the TC8830F writes the address counter value at that time into the index area of S-RAM. The write address at this time is controlled by the index register. The operations of the index register in the direct mode are described below.

- As a result of the initialization by the $\overline{ACL}$ input, address in the index area corresponding to phrase No. is set.
- When the recording is stopped automatically by the address comparator during the recording operation in the direct mode, address of the index area shown by the index register is increased for one phrase.
- When the reproducing is made by the LABEL command, address of the index area corresponding to phrase No. designated at that time is set.

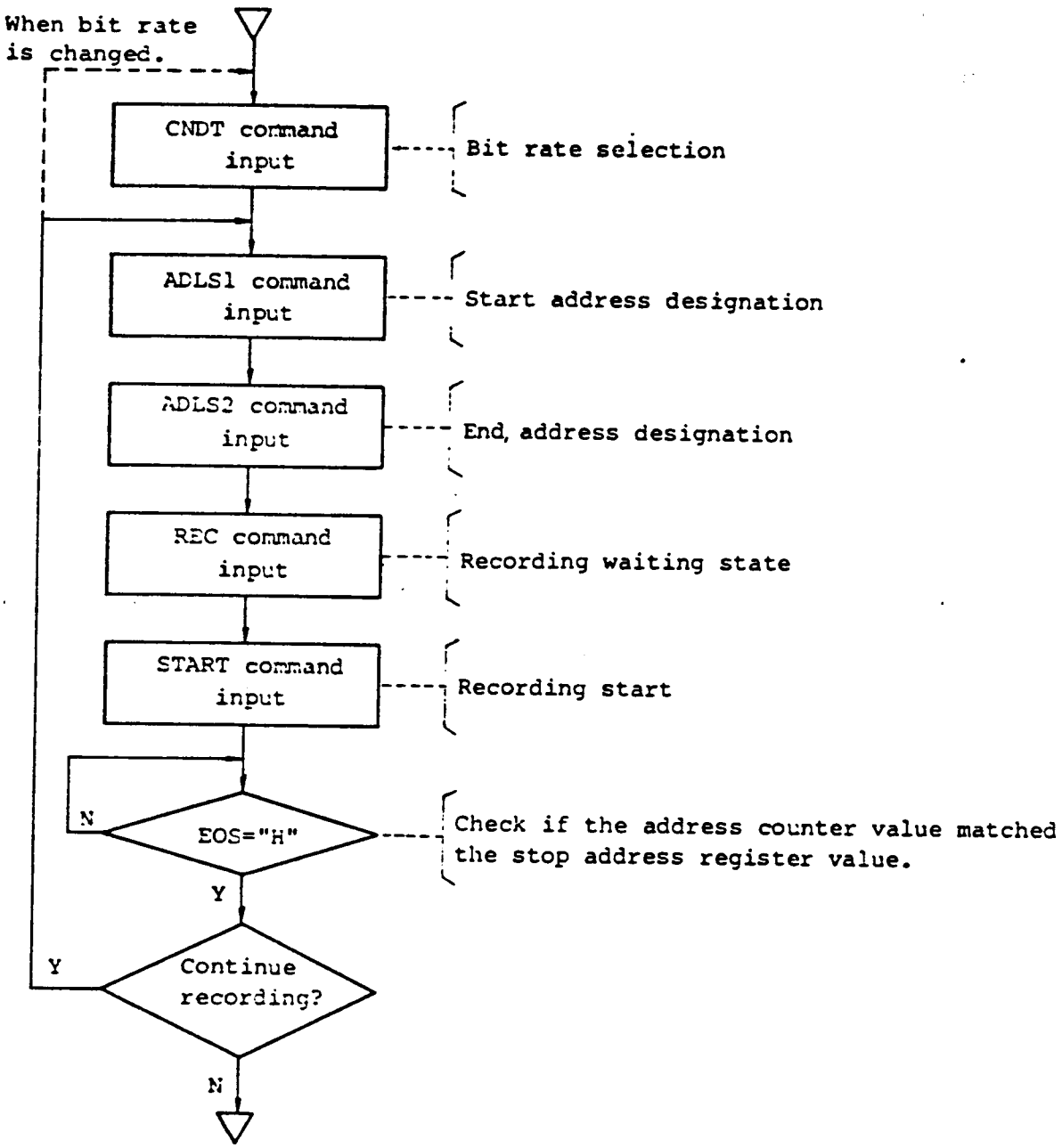
Refer to "Memory map of index area" described later for addresses of the index area, corresponding to respective phrase Nos. (From the above, it is necessary to pay attention not to write voice data into the index area.)

(2) Forced stop of recording in the direct mode

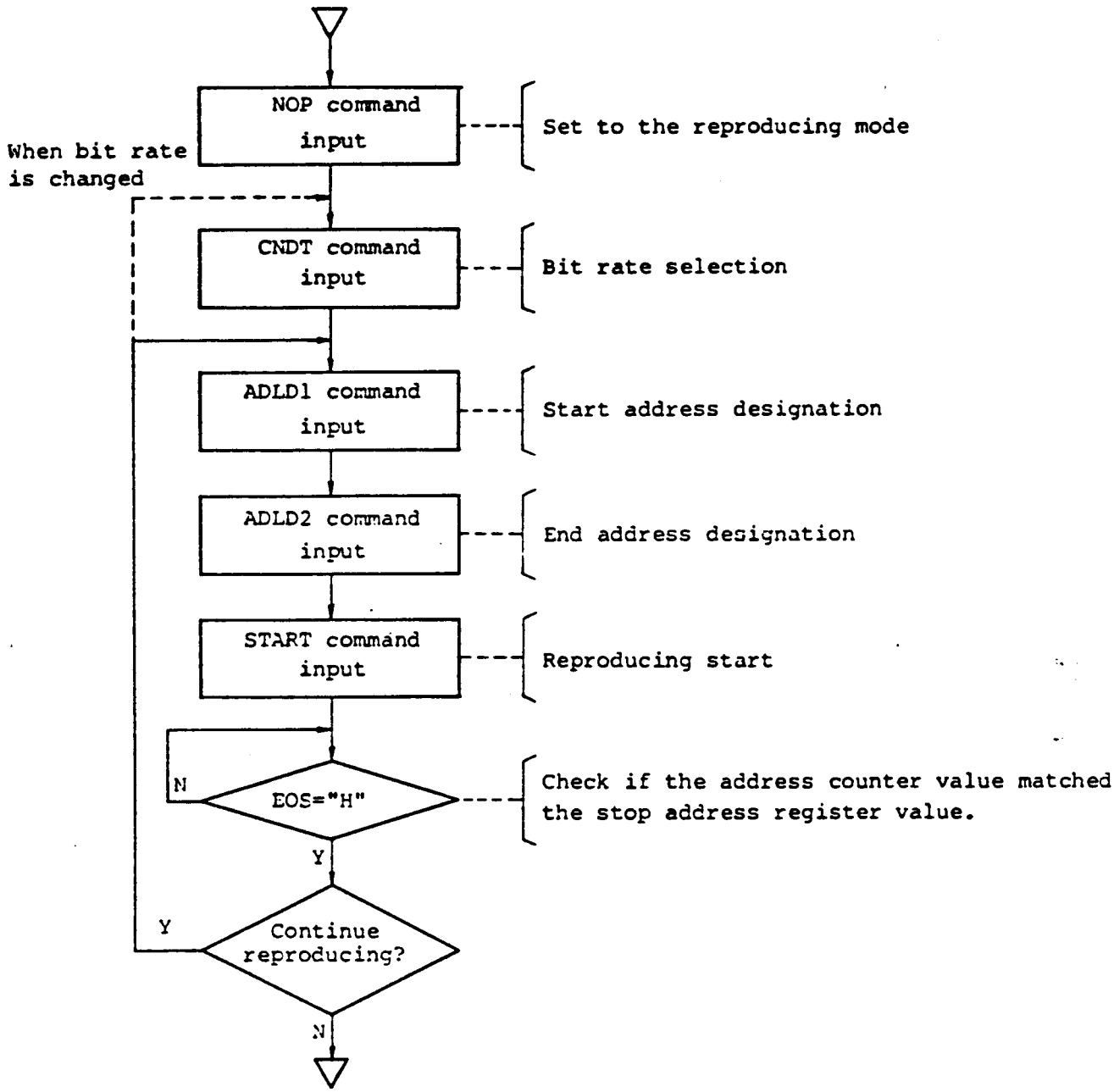
During the recording operation in the direct mode, it is possible to stop the recording by force. The address counter value when the recording was stopped by force can be read out by the ADRD command. Further, writing of end address into the index area is not performed at this time.

5.2.4 Control flowchart in the direct mode

(1) Recording



(2) Reproducing



5.2.5 Control by label index mode

The label index mode is a control mode in which the TC8830F itself writes start address and end address of the address counter into the index area of S-RAM. It is therefore possible to perform the recording/reproducing from CPU (CPU peripheral I/O port) without designating start address and end address.

—— Recording in Label Index Mode ——

(1) Set the TC8830F in the recording mode by the REC command.

(2) Designating phrase No. by the LABEL command, instruct to strat the recording.

Write start address in the index area of RAM corresponding to the designated phrase No. (Fig. 1).

The address counter is increased and voice analysis data is writen in the data area of S-RAM (Fig. 2)

(3) Instruct to stop the recording by the STOP command. The address counter stops and writes a value at the time into the index area of S-RAM corresponding to phrase No. (Fig. 3)

Fig. 1

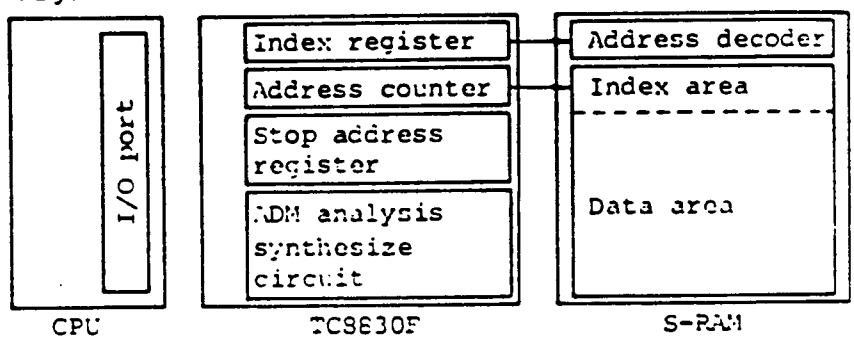


Fig. 2

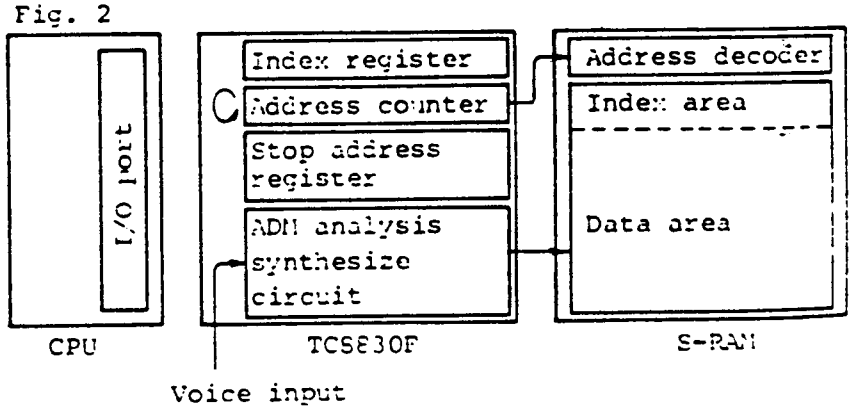
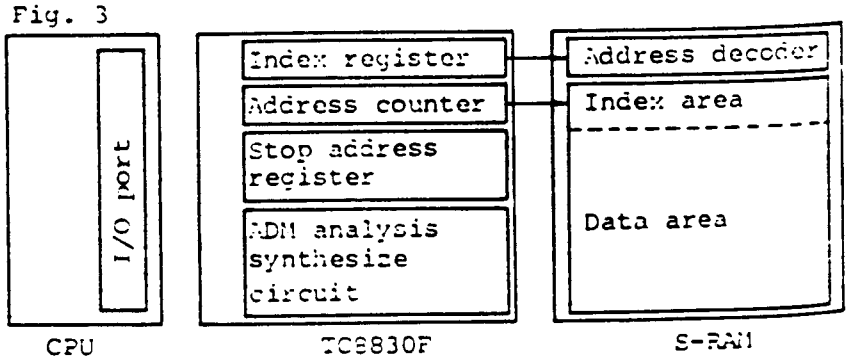


Fig. 3



—— Reproducing in label index mode ——

(1) Set the TC8830F in the reproducing mode by the NOP command.

(2) Designating phrase No. by the LABEL command, instruct to start the reproducing.

Load the start address from the index area of S-RAM corresponding to the designated phrase No. and set the address counter. (Fig. 1)

Load the end address from the index area of S-RAM corresponding to the designated phrase No. and set the stop address register. (Fig. 2)

The address counter is increased and the voice analysis data written in the data area of S-RAM is loaded. (Fig. 3)

The address comparator match of the address counter value with the stop address register value and automatically stops the reproducing.

Fig. 1

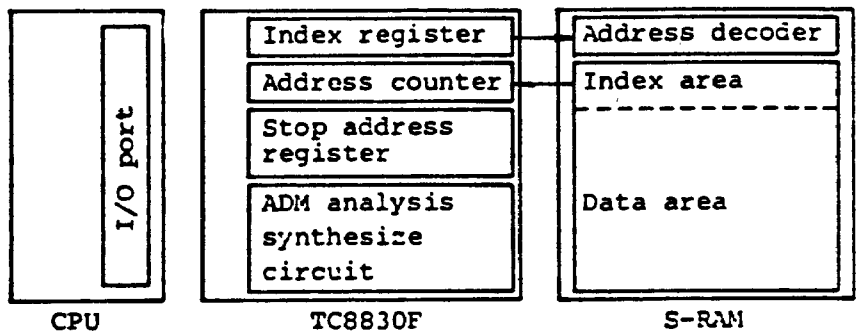


Fig. 2

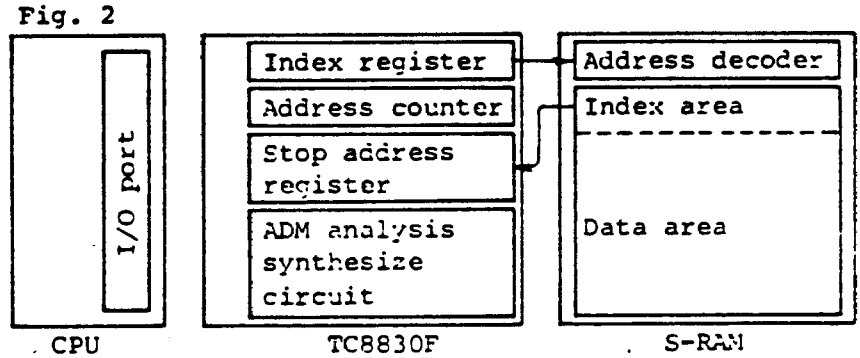
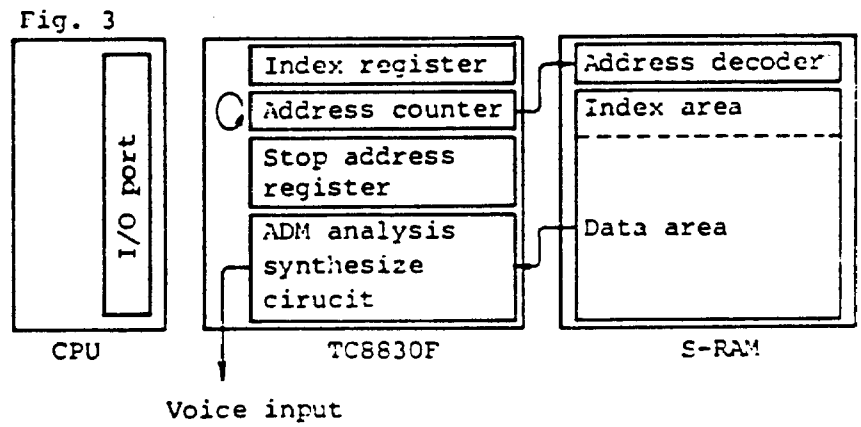
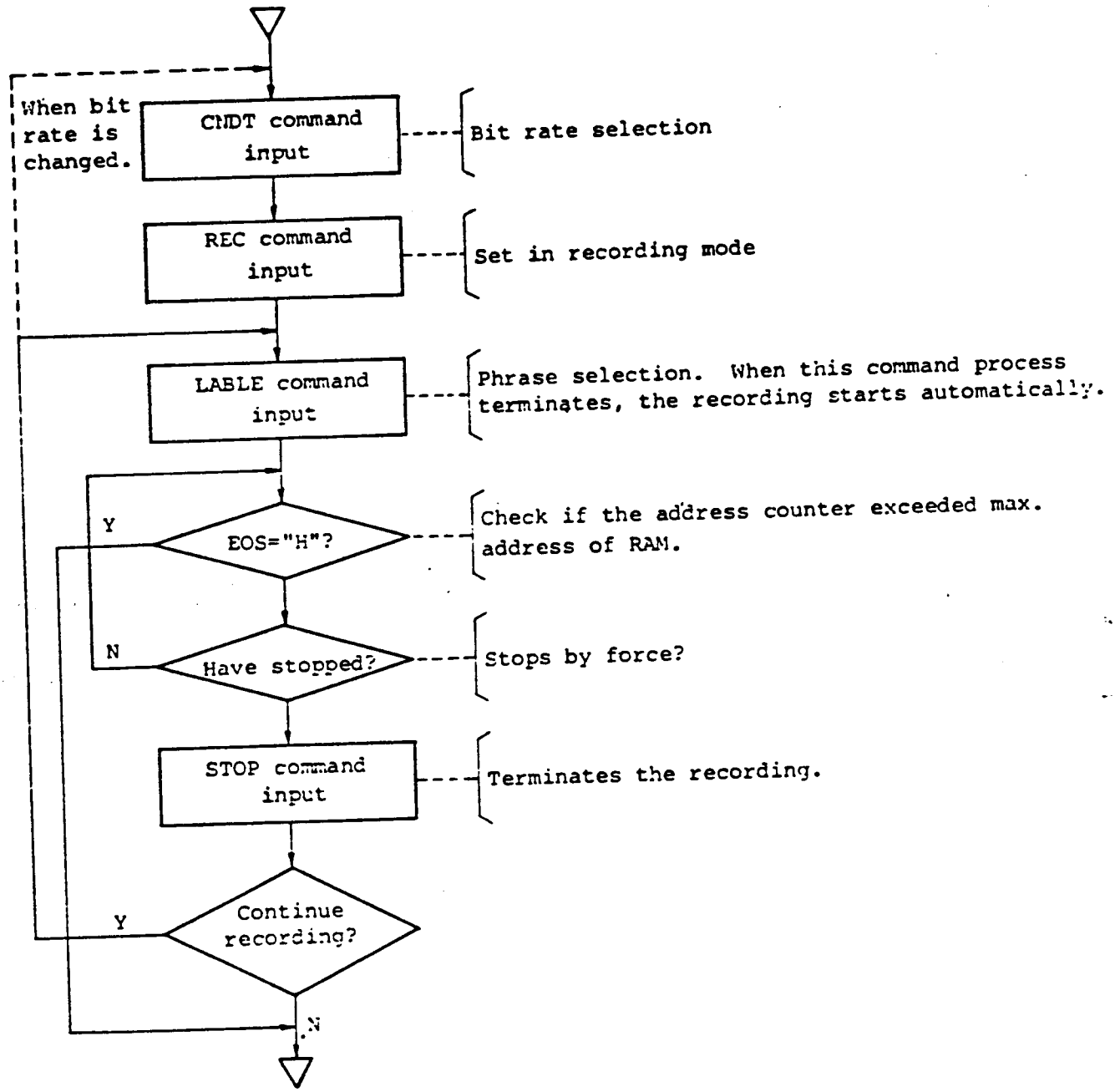


Fig. 3

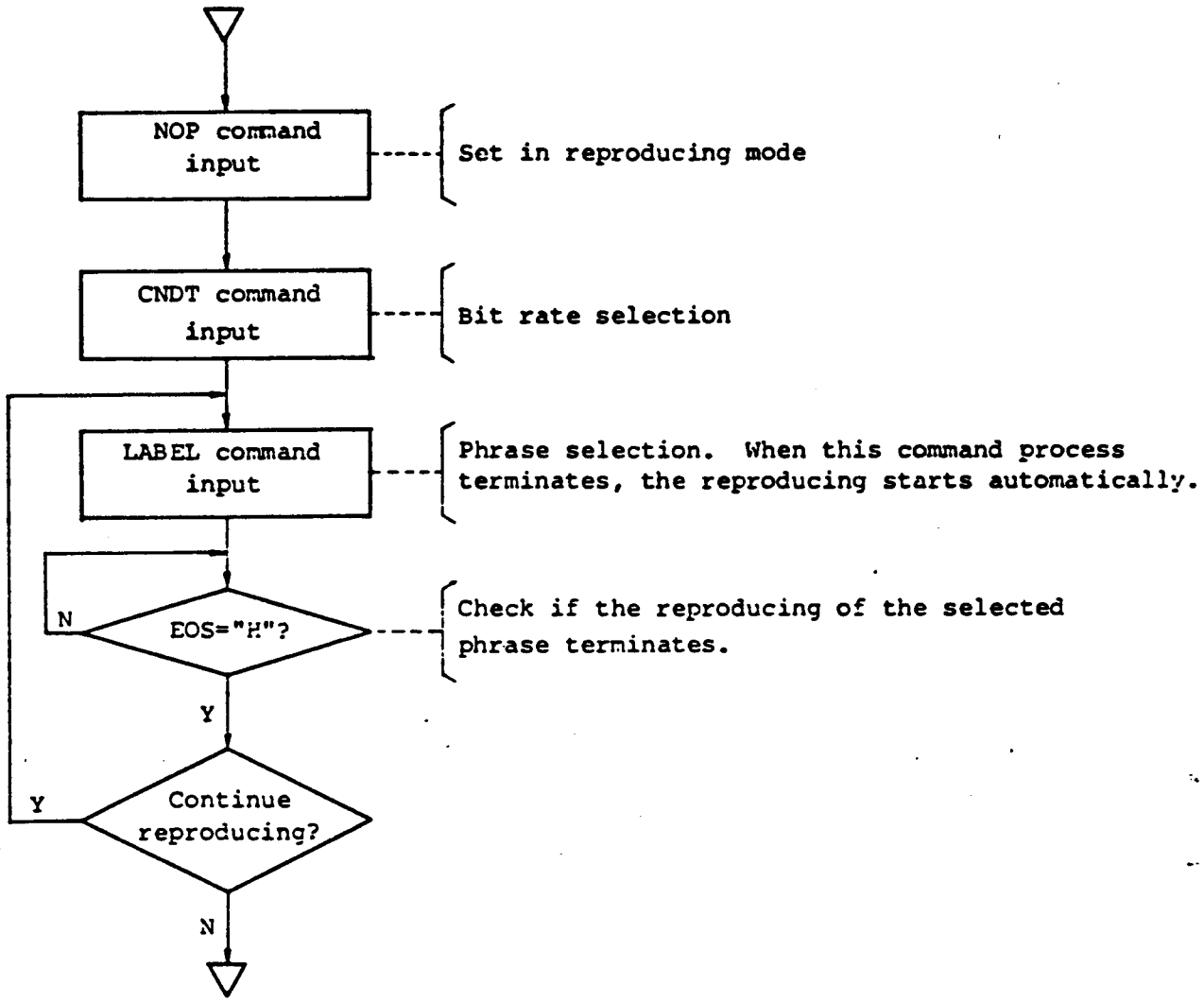


5.2.6 Example of control flowchart in label index mode

(1) Recording



(2) Reproducing



5.2.7 Status register

The status register is a 4-bit register showing the internal status of the TC8830F at time of CPU control. Data of the status register is output to the P0 ∿ P3 pin by setting the $\overline{RD}$ pin to "L" level.

Pin name	P3	P2	P1	P0
Bit name	TRIG	OVER	BUSY	$\overline{EOS}$

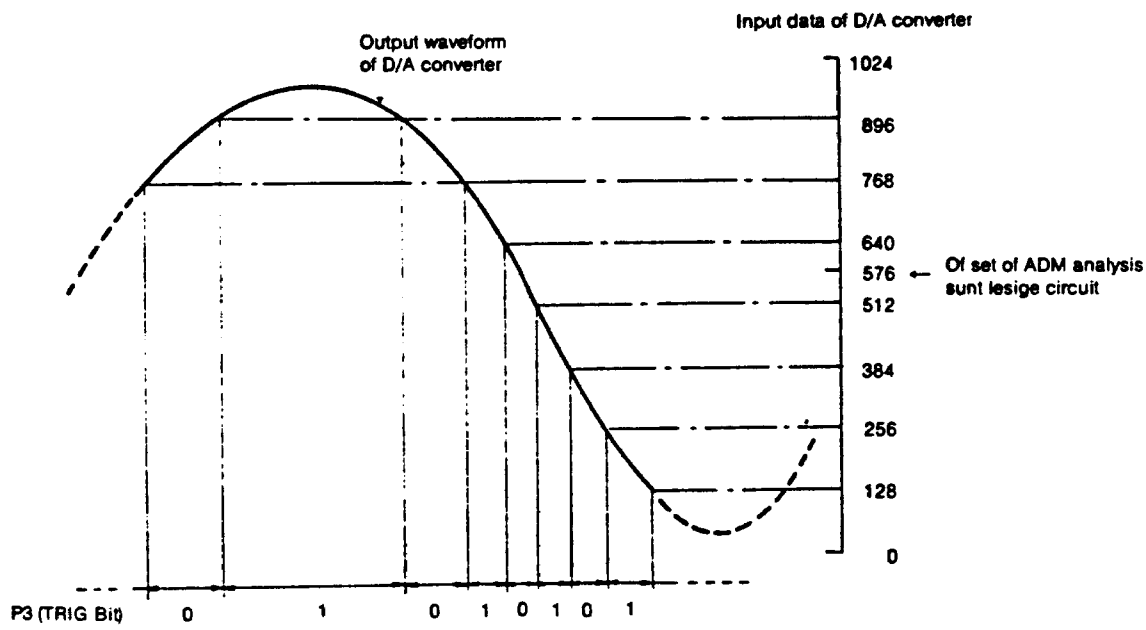
(1) TRIG

The TC8830F has a built-in ladder resister type 10 bit D/A converter. What shows state of amplitude of analyzed voice in the recording operation is TRIG bit. Since this flag shows the third bit input data from the MBS of the D/A converter, TRIG bit will becomes "H" level only when input data for the D/A converter are as follows:

128/1024 ∿ 256/1024, 384/1024 ∿ 512/1024

640/1024 ∿ 768/1024, 896/1024 ∿ 1024/1024

Further, this flag is not kept held.



(2) OVER

This bit becomes "H" level when the recording is automatically stopped by detecting the final address of RAM. This flag is kept held until the TC8830F is reset by the NOP command.

(3) BUSY

This bit becomes "H" level during the command processing or the initialization. When this flag is kept held, do not input any command.
When the ADLD1, ADLD2, CNDT, LABEL or command is input, until input of required data ends, this flag is not released.

(4) $\overline{\text{EOS}}$

This bit becomes "H" level during the recording operation and the reproducing operation. (Inversion output of the EOS pin.)

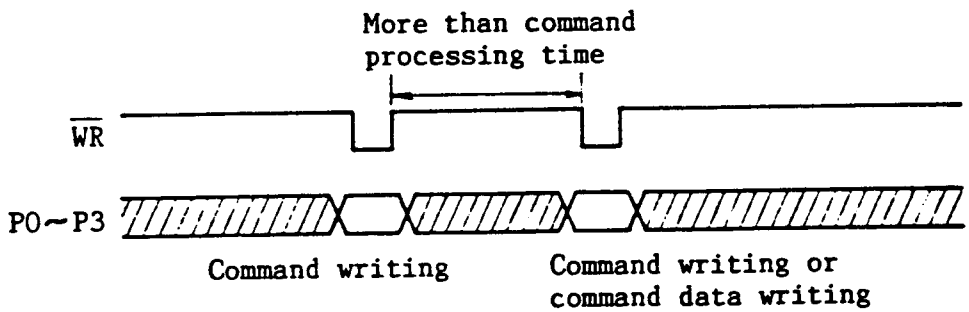
5.2.8 Command writing method

- After setting a command at the P0 ∿ P3 pin, write the command by the $\overline{WR}$ pulse.
- For the ADLD1, ADLD2, CNDT, LABEL and DTWR commands, write data following the command writing.
- For the ADRD and DTRD commands, read out data through the read access by the RD pulse following the command writing.
- Times required for processing commands are shown below. When inputting commands successively, input them at intervals of more than these command processing times.

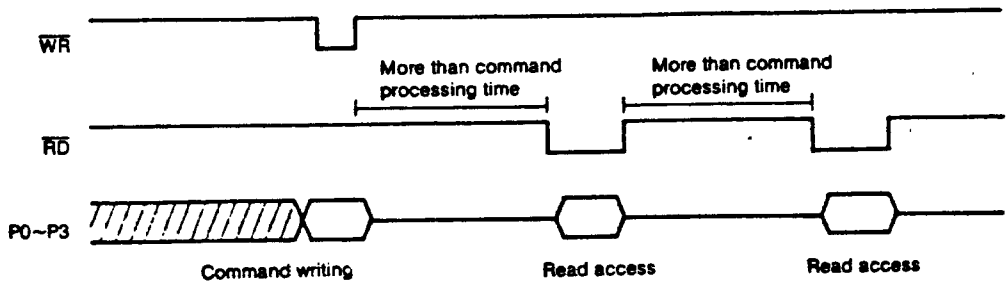
Command name	Command processing time
NOP, START, STOP, ADLD1 ADLD2, COND, REC, DTWR ADLD1, ADLD2, COND, Data input of DTWR	2T
LABEL, DTRD, ADRD Data input of LABEL Read access of DTRD and ADRD	4T

T=31.3[μs](fosc=512[kHz])

(Example 1)



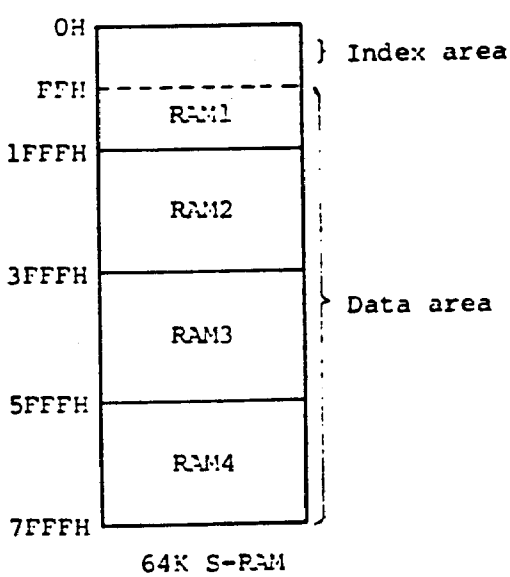
(Example 2)

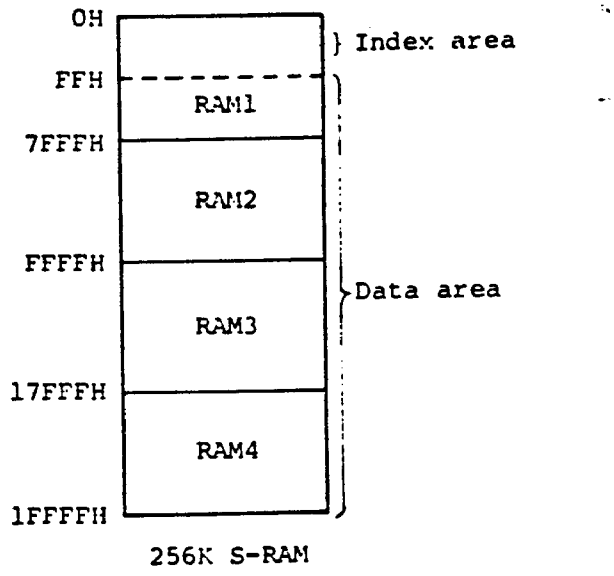


(NOTE) The $\overline{WR}$ and $\overline{RD}$ pulses should be in undisturbed waveforms. Input of disturbed waveform due to power source noise, ringing, etc. can cause malfunction.

5.2.9 Memory map

The memory configurations of RAMs to be connected to the TC8830F are shown below.



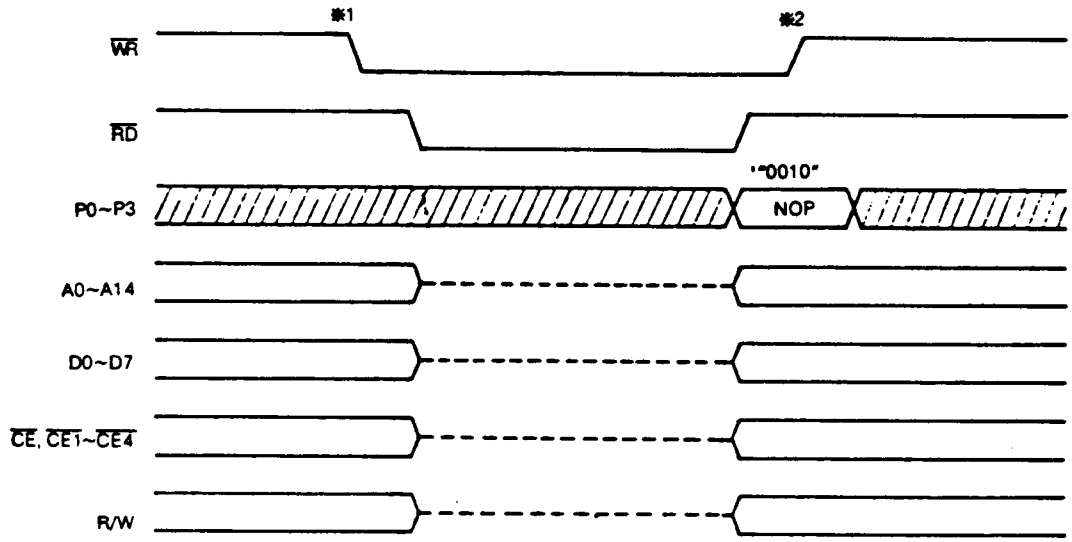


Memory map of index area

	RAM Address (HEX)	RAM Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Start address of phrase No.0	0	A7	A6	A5	A4	A3	A2	A1	A0
	1	A15	A14	A13	A12	A11	A10	A9	A8
	2	-	-	-	-	A19	A18	A17	A16
	3	-	-	-	-	-	-	-	-
End address of phrase No.0	4	A7	A6	A5	A4	A3	A2	A1	A0
	5	A15	A14	A13	A12	A11	A10	A9	A8
Strat address of phrase No.1	6	-	-	-	-	A19	A18	A17	A16
	7	-	-	-	-	-	-	-	-
End address of phrase No.1	8	A7	A6	A5	A4	A3	A2	A1	A0
	9	A15	A14	A13	A12	A11	A10	A9	A8
Start address of phrase No.2	A	-	-	-	-	A19	A18	A17	A16
	B	-	-	-	-	-	-	-	-
End address of phrase No.60	F4	A7	A6	A5	A4	A3	A2	A1	A0
	F5	A15	A14	A13	A12	A11	A10	A9	A8
Start address of phrase No.61	F6	-	-	-	-	A19	A18	A17	A16
	F7	-	-	-	-	-	-	-	-
End address of phrase No.61	F8	A7	A6	A5	A4	A3	A2	A1	A0
	F9	A15	A14	A13	A10	A11	A10	A9	A8
Start address phrase No.62	FA	-	-	-	-	A19	A18	A17	A16
	FB	-	-	-	-	-	-	-	-
End address of phrase No.62	FC	A7	A6	A5	A4	A3	A2	A1	A0
	FD	A15	A14	A13	A12	A11	A10	A9	A8
	FE	-	-	-	-	-	-	-	-
	FF	-	-	-	-	-	-	-	-

5.3 DMA function

When both the $\overline{RD}$ and $\overline{WR}$ pins are set to "L" level at time of the CPU mode, the A0 ∿A14, D0 ∿D7, $\overline{CE}$, $\overline{CE1}$ ∿ $\overline{CE4}$ and R/W pins are placed in the high impedance state. This makes is possible to release the connected RAM from the TC8830F.



[NOTE] • Use the DMA function in the reproducing waiting state or the recording waiting state.

• ※1. Set the $\overline{RD}$ pin at "L" level only after setting the $\overline{WR}$ pin at "L" level. If the $\overline{RD}$ pin is first set at "L" level, the P0 ∿ P3 pins are placed in the output state until the $\overline{WR}$ pin becomes "L" level.

• ※2. Set the $\overline{WR}$ pin at "H" level after setting the $\overline{RD}$ pin at "H" level. At this time, write the NOP command into the TC8830F.

5.4 Standby function

When the STBY pin is at "H" level, the TC8830F is in the standby state. Details of the standby function are described below.

(1) By stopping oscillation, stops all the internal operations.

(2) Sets the $\overline{CE}$ and $\overline{CE1}$ ∿ $\overline{CE4}$ pins at "H" level and places external RAM in the minimum standby current mode.

(3) Separates the built-in pull-down resistor from each of the P0 ∿ P3, $\overline{RD}$, $\overline{WR}$, and PH0 ∿ PH3 pins.

(4) Stops power consumption in the D/A converter.

(5) Stops power consumption in the microphone amp. 1, microphone amp 2, and band-pass filters.

[NOTE] • The TC8830F cannot be shifted from the recording operation/reproducing operation state to the standby state. Do not set the STBY pin at "H" level during the recording/reproducing operation.

• Under the STBY state, the DAO and FILOUT pins are placed in the high impedance state.

5.5 Initializing operation

When LOW pulse is input to the $\overline{ACL}$ pin, the TC8830F stops all operations and then, performs the initializing operation. Details of the initializing operation are described below.

(1) Time required for the initializing operation is 32[msec](TYP.) (f_{OSC}=512[kHz]).

(2) Clears RAM addresses 0H ∿ FEH (Index area) and presets the address counter at address 100H.

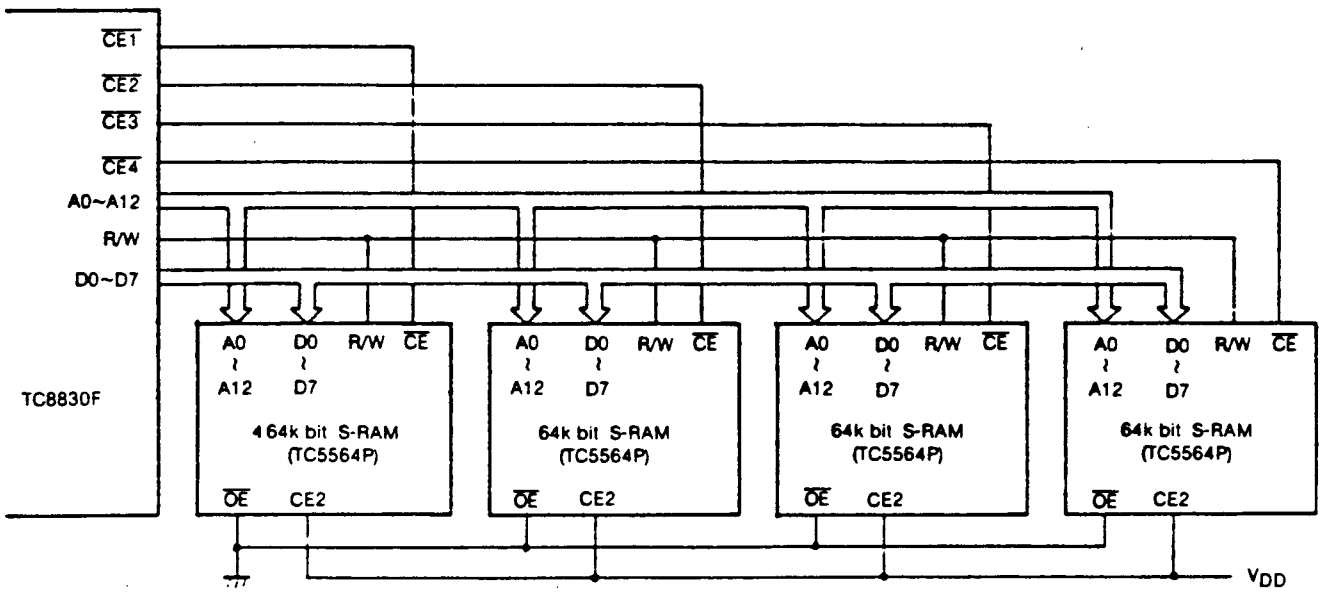
(3) At time of the CPU control, sets the TC8830F in the reproduceing mode.

(4) At time of the CPU control, sets the bit rate at 8 Kbps.

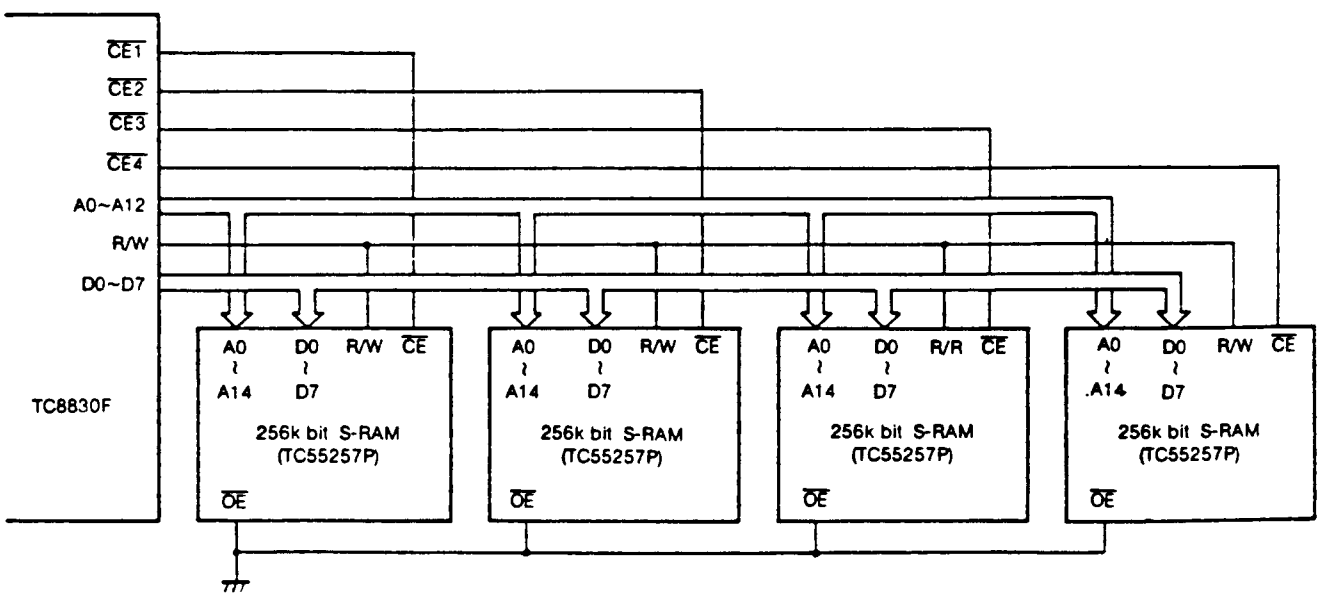
(5) At time of the CPU control, clears OVER bit of the status register.

5.6 S-RAM connecting method

To connect 64Kbit S-RAM 256K pin="L"



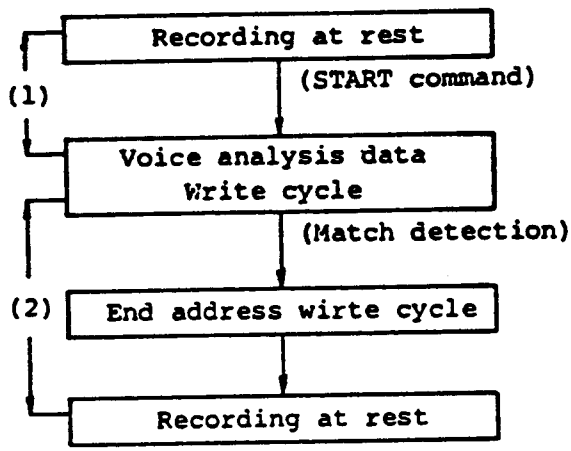
To connect 256Kbit S-RAM 256K pin="H"

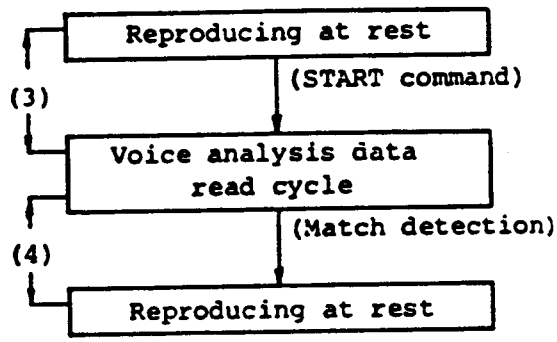


5.7 S-RAM interface timing

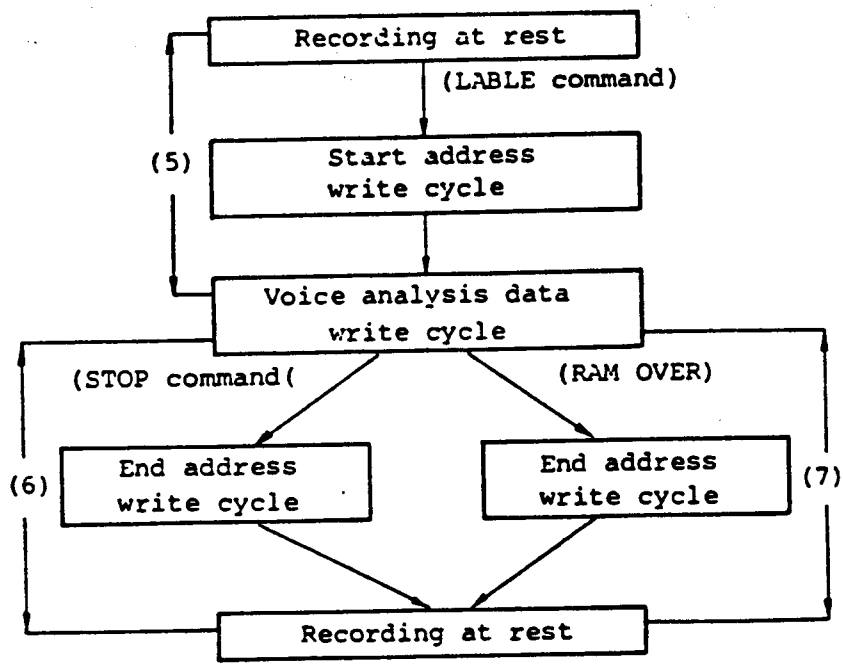
Timings for numerals in parentheses in the following flowchart are illustrated from next page.

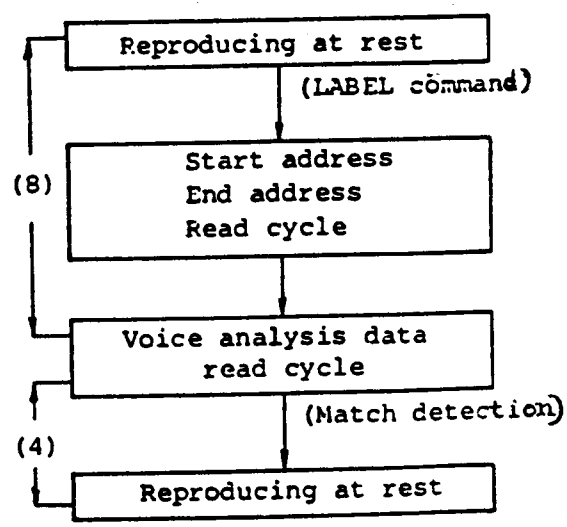
Recording/reproducing in direct mode



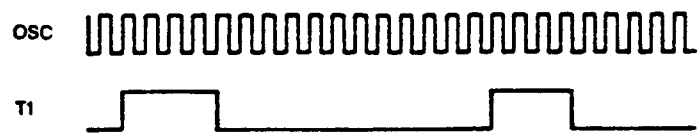


Recording/reproducing in label index mode

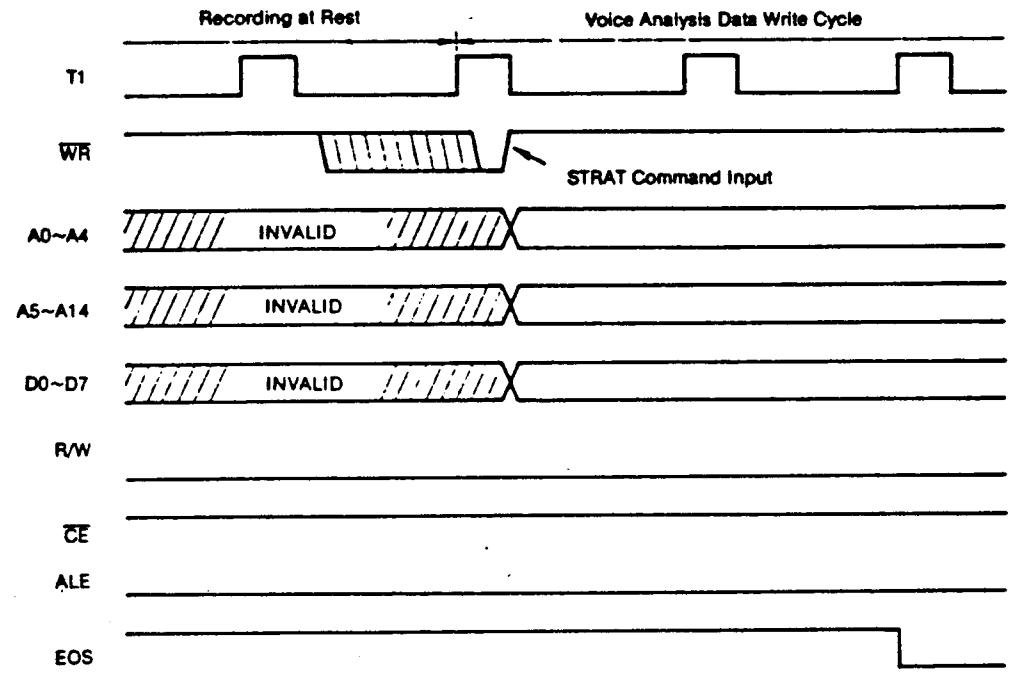




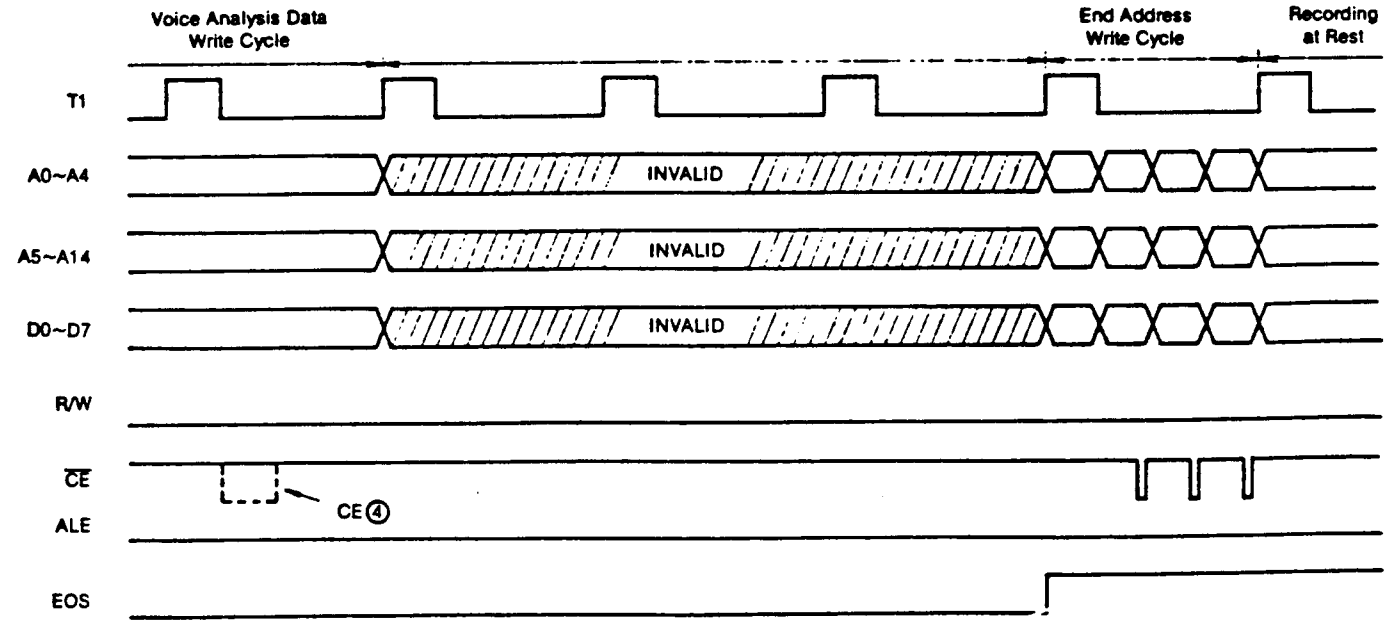
Relation between internal cycle signal and



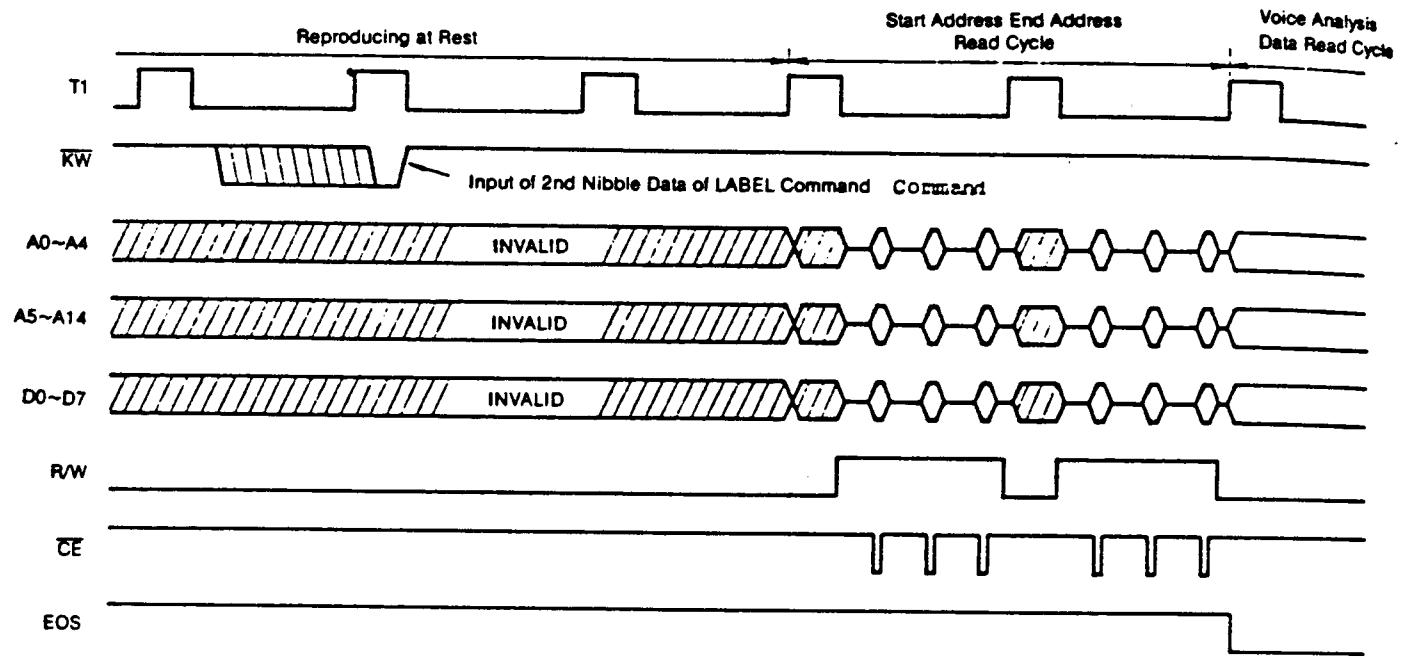
((1))



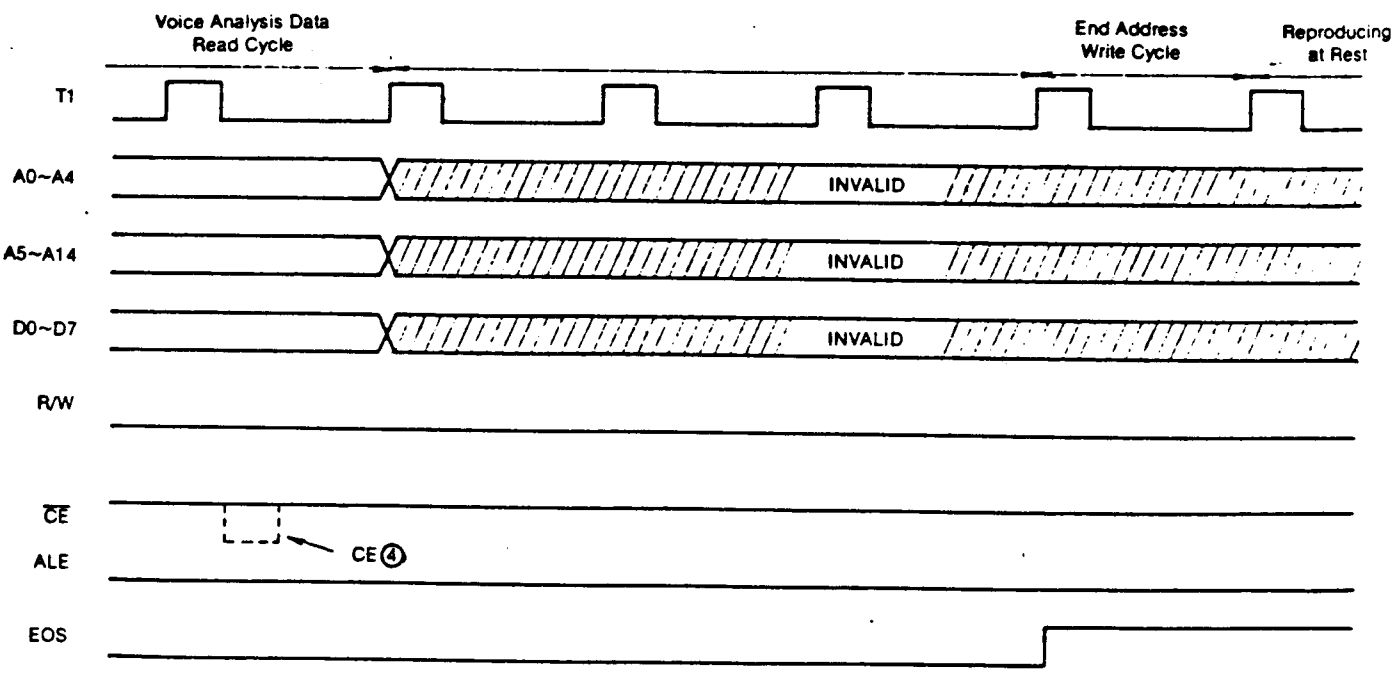
((2))



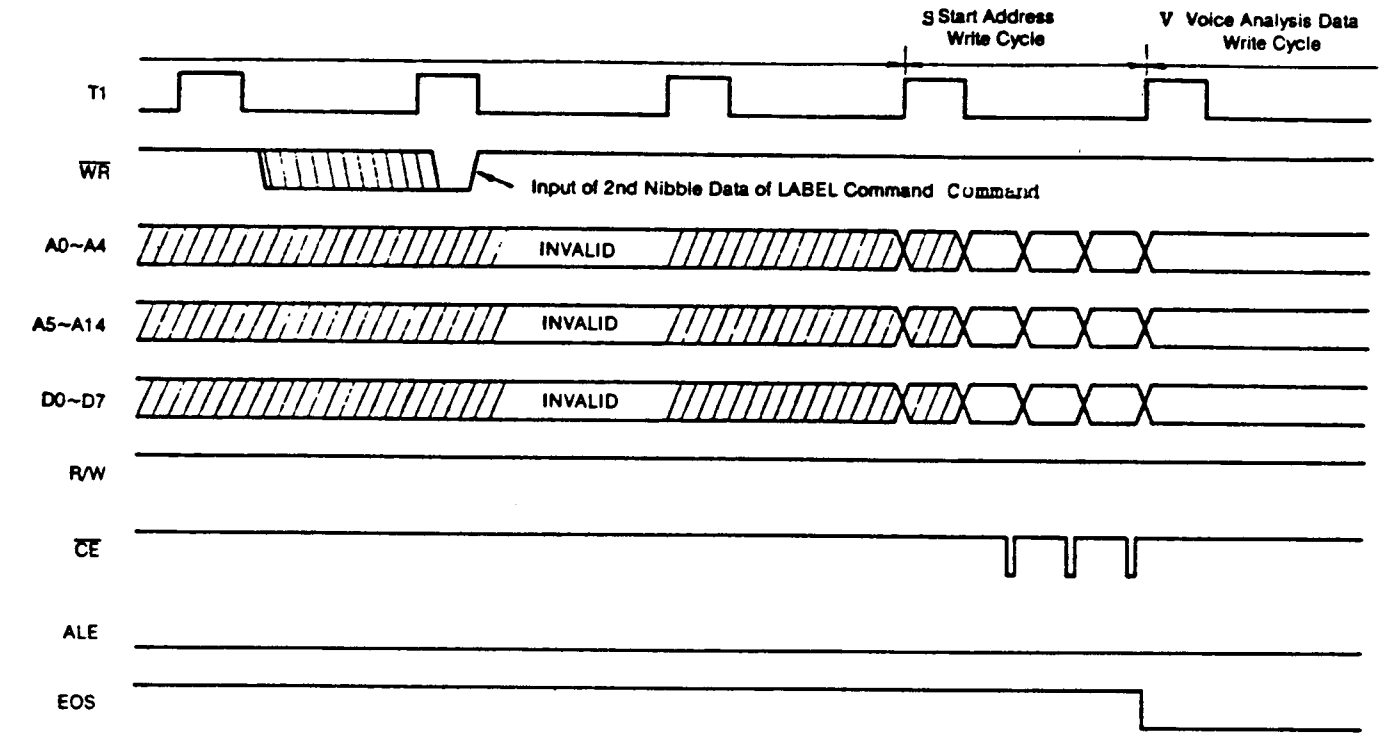
((3))


Reproducing at Rest
Start Address End Address Read Cycle
Voice Analysis Data Read Cycle
T1
KW
Input of 2nd Nibble Data of LABEL Command
Command
A0~A4
INVALID
A5~A14
INVALID
D0~D7
INVALID
R/W
CE
EOS

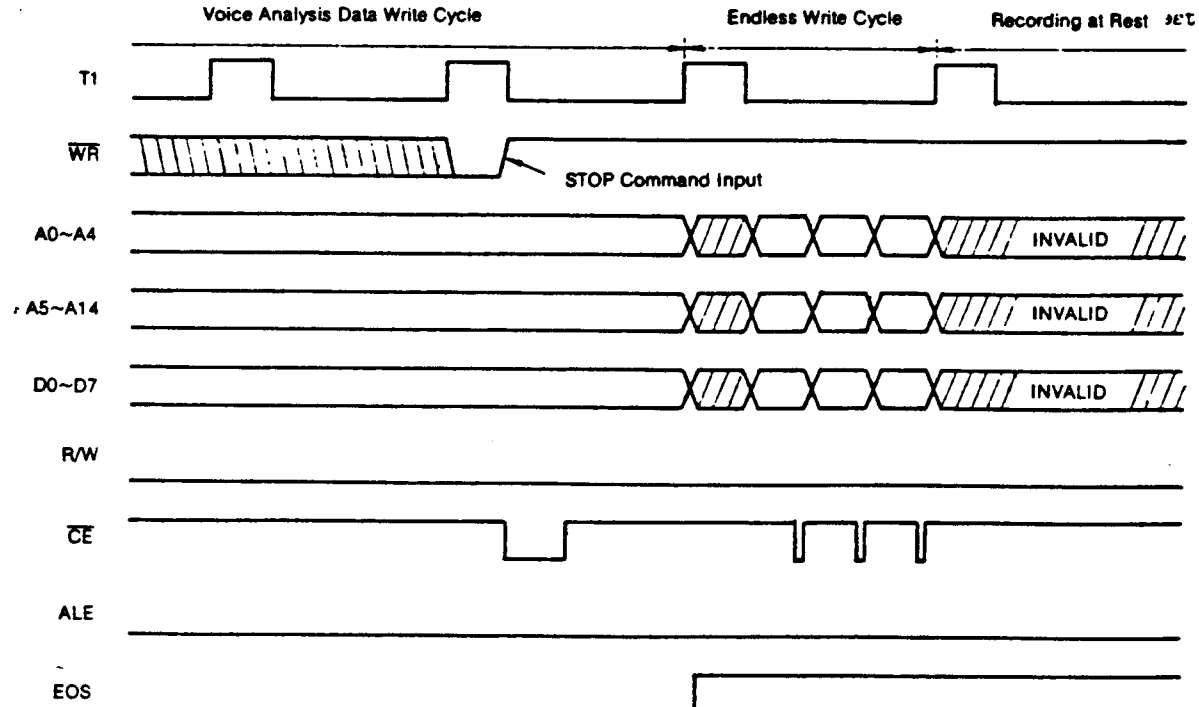
((4))

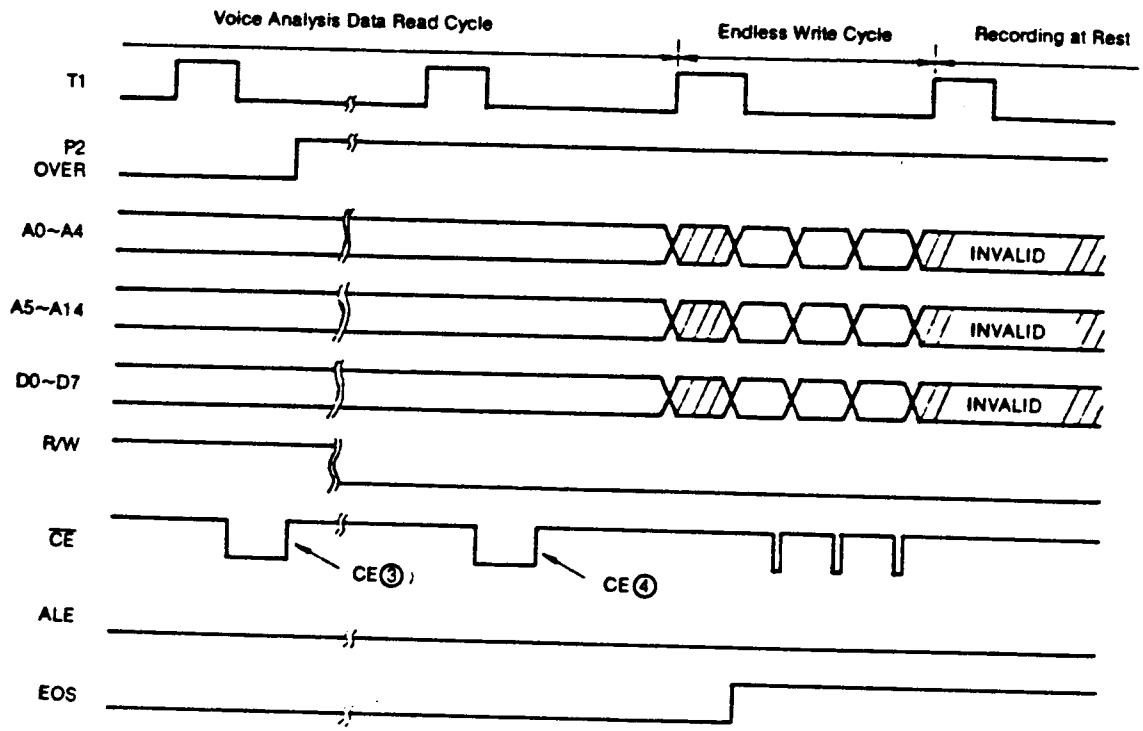

Voice Analysis Data Read Cycle
End Address Write Cycle
Reproducing at Rest
T1
A0~A4
INVALID
A5~A14
INVALID
D0~D7
INVALID
R/W
CE
CE④
ALE
EOS

(5)

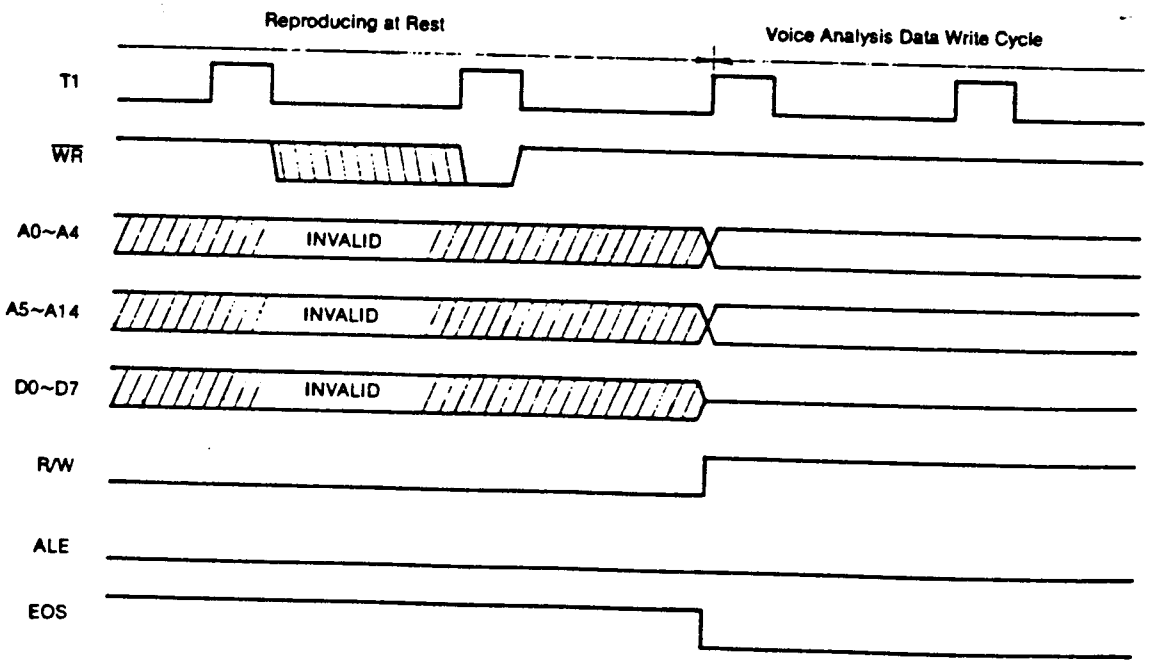

S Start Address Write Cycle
V Voice Analysis Data Write Cycle
T1
WR
Input of 2nd Nibble Data of LABEL Command Command
A0~A4
INVALID
A5~A14
INVALID
D0~D7
INVALID
R/W
CE
ALE
EOS

(6)

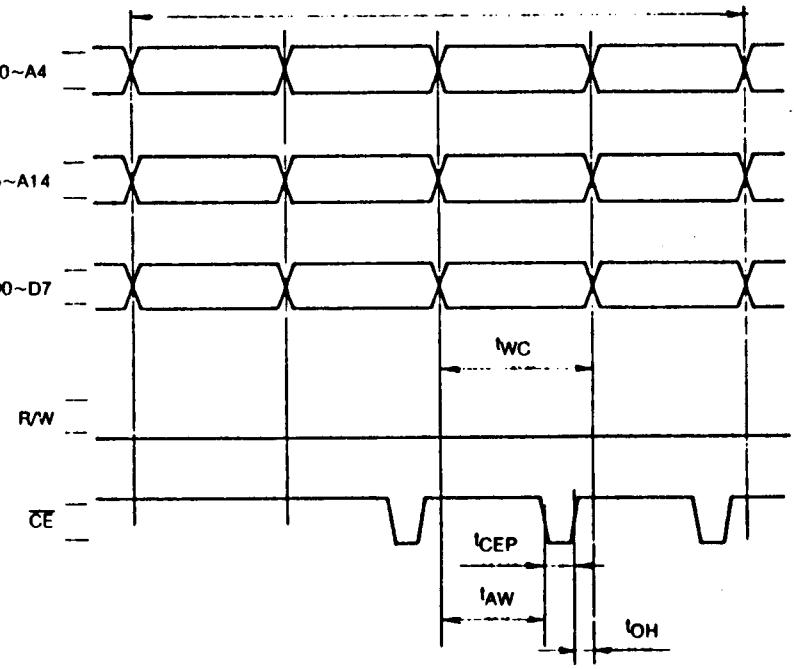

Voice Analysis Data Write Cycle
Endless Write Cycle
Recording at Rest
T1
WR
STOP Command Input
A0~A4
INVALID
A5~A14
INVALID
D0~D7
INVALID
R/W
CE
ALE
EOS


Voice Analysis Data Read Cycle
Endless Write Cycle
Recording at Rest
T1
P2
OVER
A0~A4
A5~A14
D0~D7
R/W
CE
CE③
CE④
ALE
EOS
INVALID
INVALID
INVALID

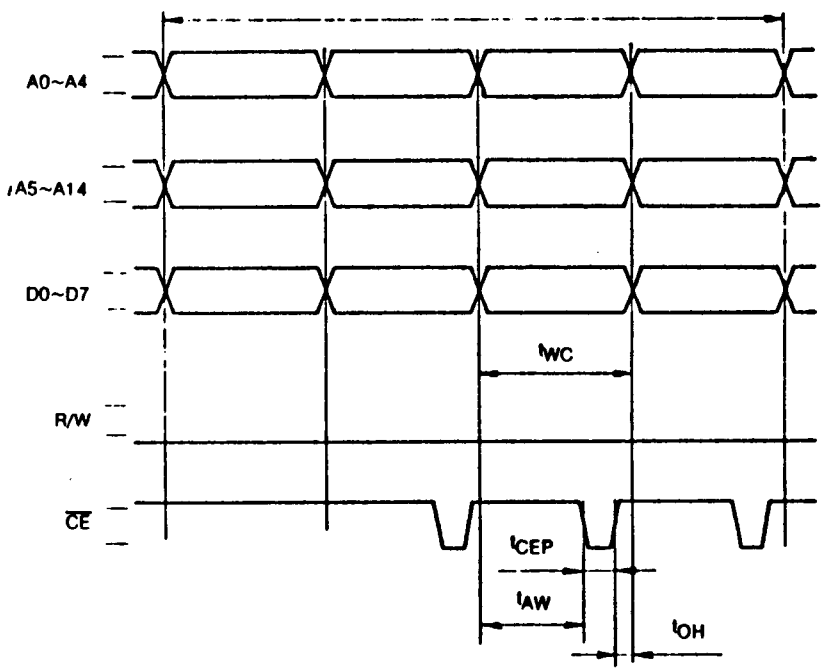
(8)


Reproducing at Rest
Voice Analysis Data Write Cycle
T1
WR
A0~A4
A5~A14
D0~D7
R/W
ALE
EOS
INVALID
INVALID
INVALID

Start address write cycle



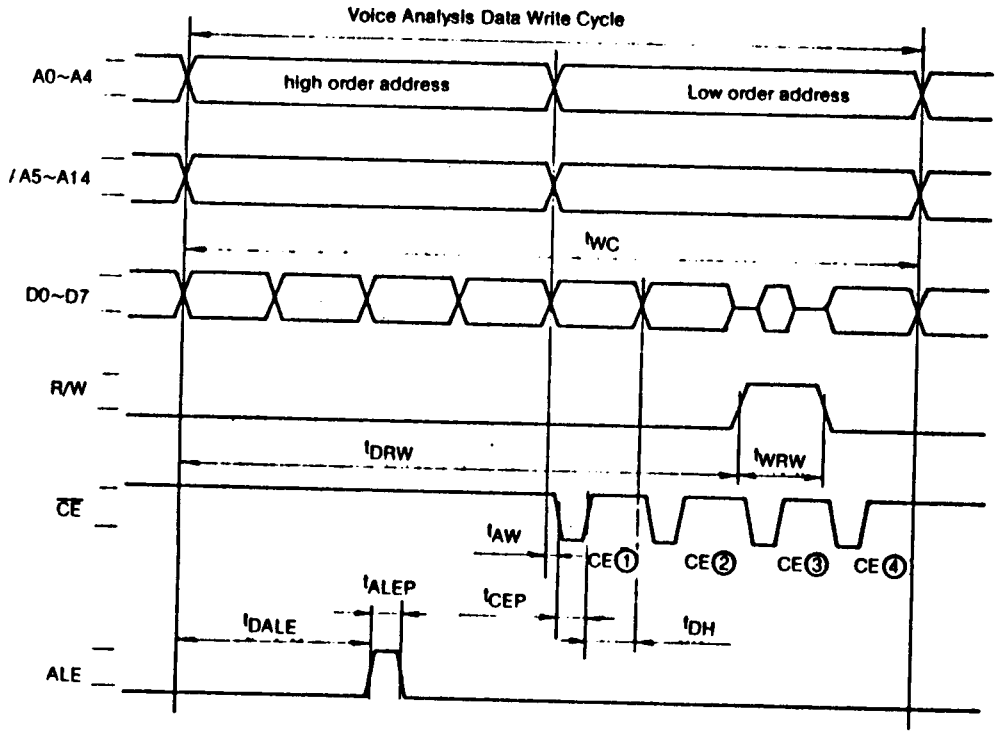
End address write cycle



SYMBOL	ITEM	TYPICAL VALUE
t_{WC}	Write cycle time	8 tϕ
t_{CEP}	CE pulse width	1 tϕ
t_{AW}	Address setup time	6 tϕ
t_{DH}	Data hold time	1 tϕ

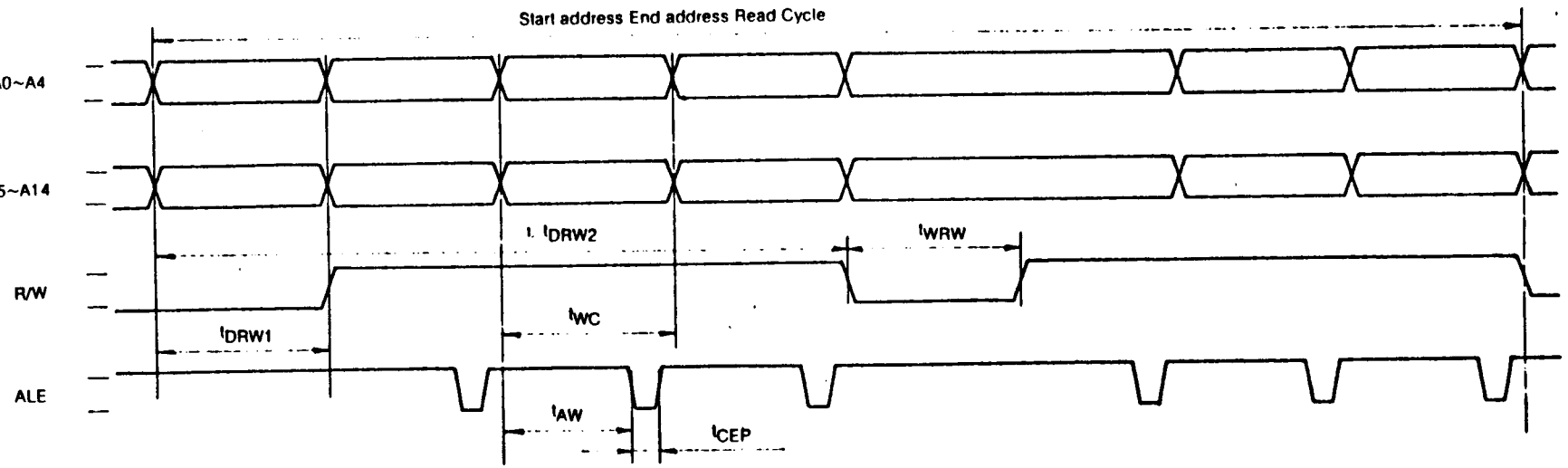
SYMBOL	ITEM	TYPICAL VALUE
t_{WC}	Write cycle time	8 tϕ
t_{CEP}	CE pulse width	1 tϕ
t_{AW}	Address setup time	6 tϕ
t_{DH}	Data hold time	1 tϕ

tϕ=0.98 [μs](f_{OSC}=512[kHz])



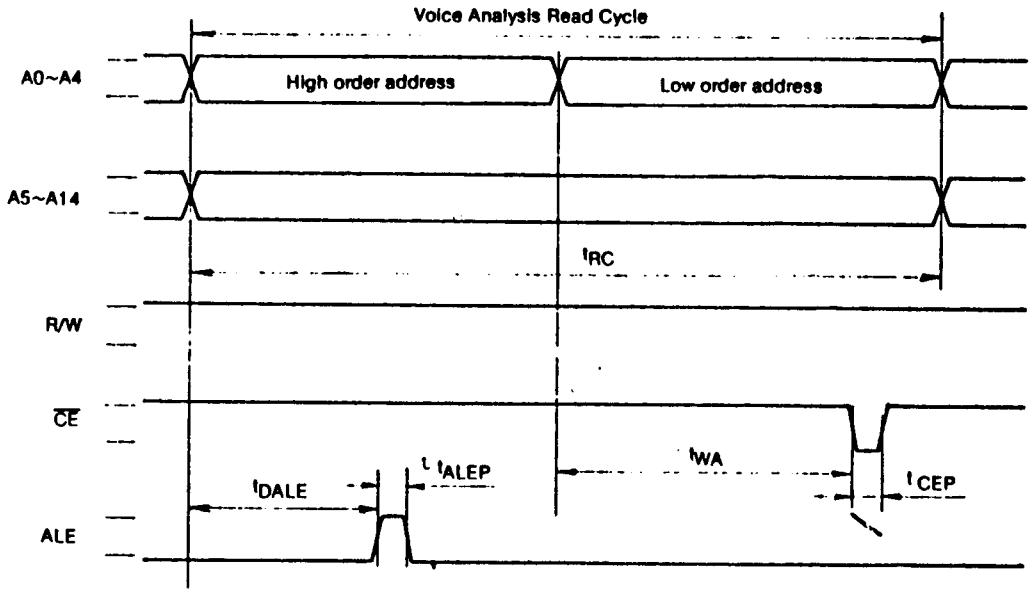
SYMBOL	ITEM	TYPICAL VALUE			
		32kbps	16kbps	11kbps	8kbps
t_{WC}	Write cycle time	256 tϕ	512 tϕ	768 tϕ	1024 tϕ
t_{CEP}	CE pulse width	8 tϕ	8 tϕ	8 tϕ	8 tϕ
t_{AW}	Address setup time	8 tϕ	8 tϕ	8 tϕ	8 tϕ
t_{DH}	Data hold time	16 tϕ	48 tϕ	80 tϕ	112 tϕ
t_{DALE}	ALE Delay time	72 tϕ	136 tϕ	200 tϕ	264 tϕ
t_{ALEP}	ALE Pulse width	8 tϕ	8 tϕ	8 tϕ	8 tϕ
t_{DRW}	R/W Delay time	192 tϕ	384 tϕ	576 tϕ	768 tϕ
t_{WRW}	R/W Rise width	32 tϕ	64 tϕ	96 tϕ	128 tϕ

tϕ=0.98 [μs] (f_{OSC}=512[kHz])



SYMBOL	ITEM	TYPICAL VALUE
t_{WC}	Read cycle time	8 tϕ
t_{CEP}	$\overline{CE}$ pulse width	1 tϕ
t_{AW}	Address setup time	6 tϕ
t_{DRW1}	R/W delay time 1	8 tϕ
t_{DRW2}	R/W delay time 2	32 tϕ
t_{WRW}	R/W rise width	8 tϕ

$t\phi = 0.98[\mu s]$ ($f_{OSC} = 512[kHz]$)



SYMBOL	ITEM	TYPICAL VALUE			
		32kbps	16kbps	11kbps	8kbps
t_{RC}	Read cycle time	256 t_ϕ	512 t_ϕ	768 t_ϕ	1024 t_ϕ
t_{CEP}	$\overline{CE}$ pulse width	8 t_ϕ	8 t_ϕ	8 t_ϕ	8 t_ϕ
t_{AW}	Address setup time	104 t_ϕ	200 t_ϕ	296 t_ϕ	392 t_ϕ
t_{DALE}	ALE delay time	72 t_ϕ	136 t_ϕ	200 t_ϕ	264 t_ϕ
t_{ALEP}	ALE pulse width	8 t_ϕ	8 t_ϕ	8 t_ϕ	8 t_ϕ

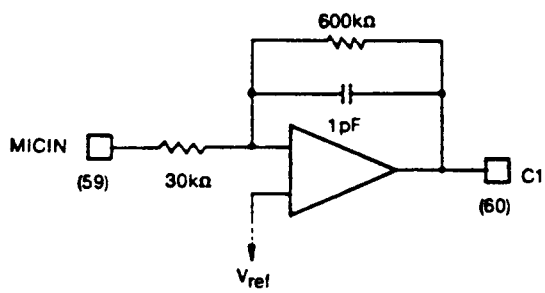
t_ϕ=0.98[μs] (f_{OSC}=512[kHz])

[6] ANALOG PART

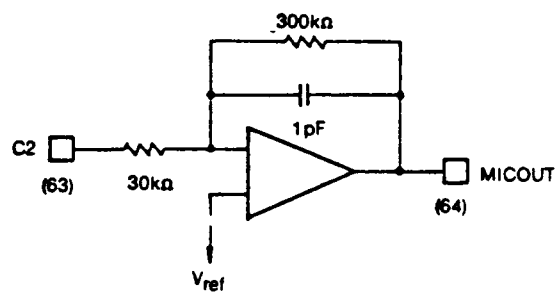
The TC8830F has the built-in two-stage microphone amplifiers and band-pass filters. Therefore, a microphone is directly connectable and no external filter is required.

6.1 Microphone amplifiers

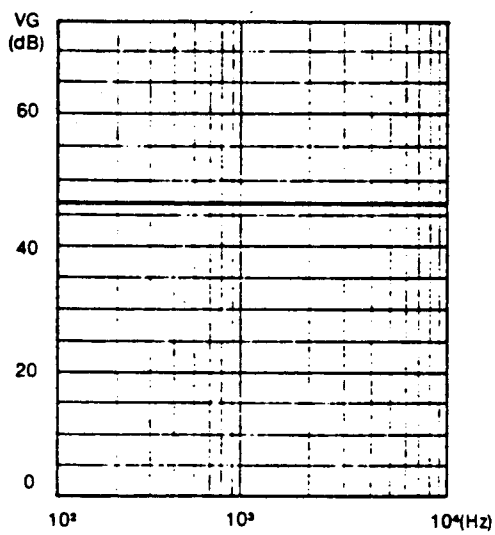
The TC8830F contains the two-stage microphone amplifiers; MIC AMP1 gain: 20 times (TYP.), MIC AMP2 gain: 10 times (TYP.). Therefore, gain up to 200 times can be obtained.



Equivalent circuit of MIC AMP1



Equivalent circuit of MIC AMP2

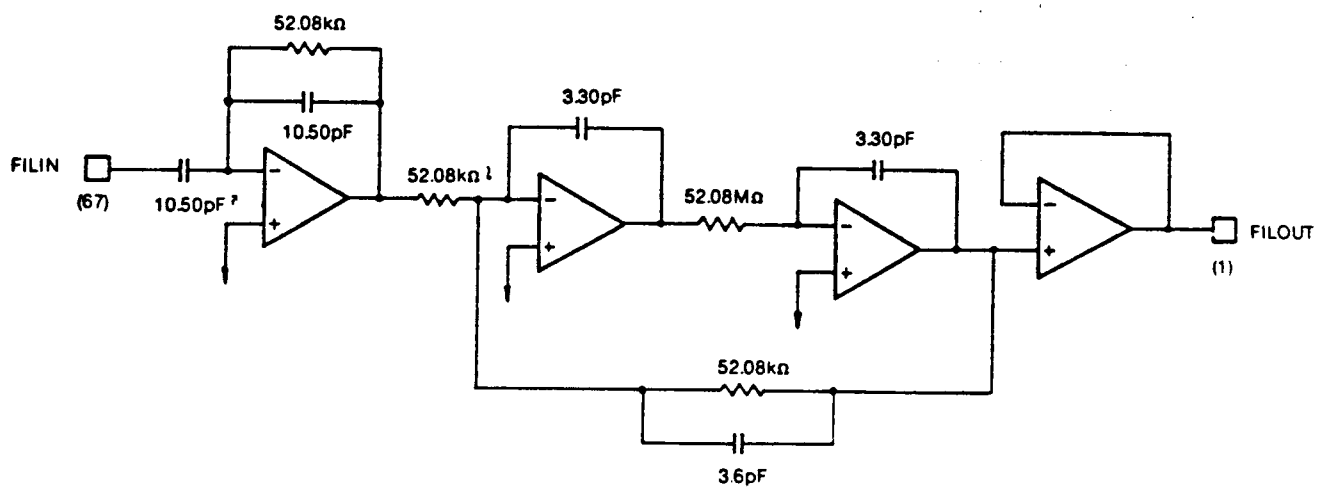


Frequency characteristics of microphone amplifier

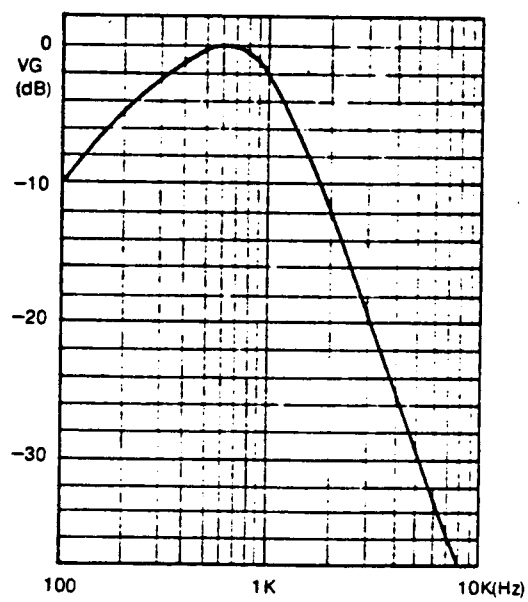
[NOTE]
- Frequency characteristic of the microphone amplifier is that measured between the MICIN pin and MICOUT pin with the C1 pin and C2 pin coupled by a 0.1uF luminated ceramic capacitor.
- MIC AMP2 becomes valid (power ON) only in the recording operation state.

6.2 Band-pass filter

The band-pass filter consists of the primary high-pass filter and the secondary low-pass filter.



Equivalent circuit of band-pass filter



Frequency characteristic of band-pass filter

Frequency characteristic of the band-pass filter is that measured between the FILIN pin and FILOUT Pins.

[7] PIN NAMES AND PIN DESCRIPTION

PIN NAME	PIN NO.	CONSTRUCTION				FUNCTION
		MANUAL CONTROL		CPU CONTROL		
		I/O	PULL-UP PULL-DOWN	I/O	PULL-UP PULL-DOWN	
P0	54	Input	Internal pull-down	I/O	None	At time of the CPU control, serves as the two-way data bus for exchanging commands and data with external CPU. At time of the manual control, serves as the input terminal (containing PULL DOWN resistor) with the functions shown below.
						START input terminal. The recording/ reproducing starts when this pin is set to "H" level.
P1	53					STOP input terminal. The recording/ reproducing stops when this pin is set to "H" level.
P2	52					Auto phrase input terminal. The auto phrase function becomes valid when this pin is set to "H" level.
P3	51					Recording/reproducing selector terminal. The recording mode at "H" level and the reproducing mode at "L" level.
$\overline{RD}$	46	Input	Internal pull-down	Input	None	Read pulse input terminal at time of the CPU control. Serves as the bit rate selection input terminal at time of the manual control.
$\overline{WR}$	45	Input	Internal pull-down	Input	None	Write pulse input terminal at the CPU control. Serves as the bit rate selection input terminal at time of the manual control mode.

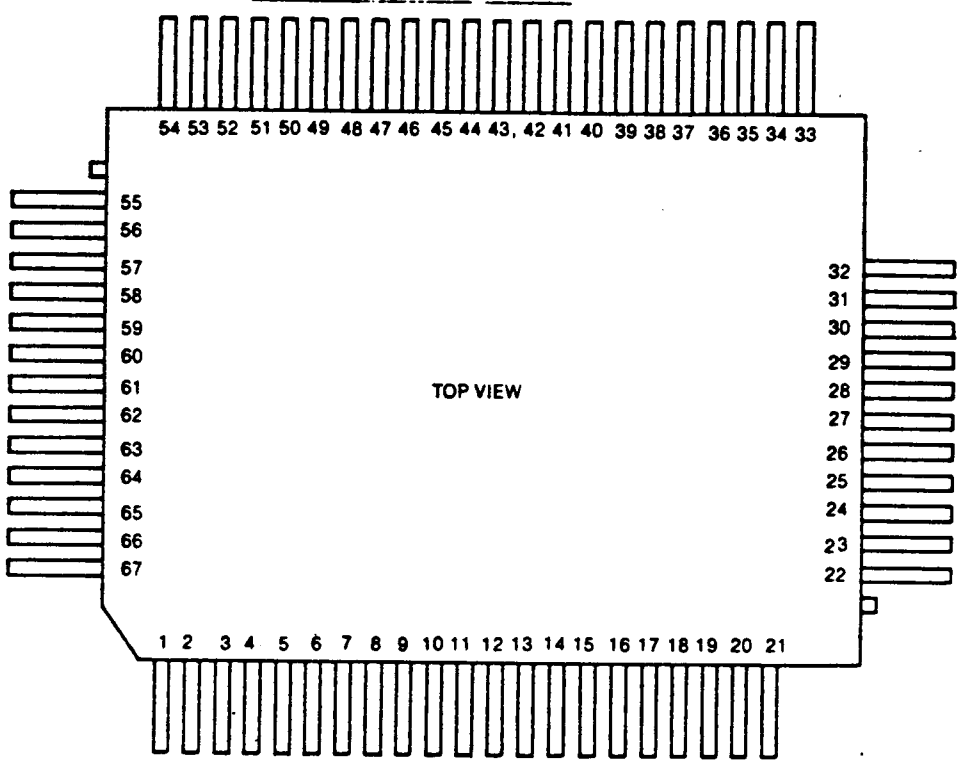
PIN NAME	PIN NO.	CONSTRUCTION				FUNCTION
		MANUAL CONTROL		CPU CONTROL		
		I/O	PULL-UP PULL-DOWN	I/O	PULL-UP PULL-DOWN	
EOS	55	Output	-	Output	-	End of Speech output terminal. This pin is at "H" level in the recording waiting state and the reproducing waiting state, while it becomes "L" level in the recording operation and the reproducing operation state.
CPUM	57	Input	None	Input	None	Manual control/CPU control selector terminal. The manual control when this pin is at "L" level and the CPU control at "H" level.
PH0 PH1 PH2 PH3	50 49 48 47	Input	Internal pull-down	Input	Internal pull-down	Phrase selection input terminals. Max. 16 phrases are selectable at 4-bit codes. (PH0=LSB, PH3=MSB) Valid only in the manual control mode and becomes invalid in the CPU control mode.
256K	42	Input	None	Input	None	Sets at "L" level when 64kbit S-RAM is used and at "H" level for 256kbit S-RAM.
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14	33 32 31 30 29 28 26 25 24 23 22 21 19 18 17	Output	-	Output	-	RAM address output, terminals. Connect to S-RAM address inputs. When 64kbit S-RAM is used, use only A0 ∿ A12 pins. A0 ∿ A4 pins output A0 ∿ A4 or A15 ∿ A19 at time sharing. At time of the CPU control, these pins are placed in the high impedance state by the DMA function.

PIN NAME	PIN NO.	CONSTRUCTION				FUNCTION
		MANUAL CONTROL		CPU CONTROL		
		I/O	PULL-UP PULL-DOWN	I/O	PULL-UP PULL-DOWN	
D0 D1 D2 D3 D4 D5 D6 D7	16 15 14 13 10 8 6 4	I/O	None	I/O	None	RAM data input/output terminals. Connect to S-RAM data terminals. At time of the CPU control, these pins are placed in the high impedance state by the DMA function.
$\overline{CE1}$ $\overline{CE2}$ $\overline{CE3}$ $\overline{CE4}$	35 36 37 38	Output	-	Output	-	RAM chip enable output terminals. According to quantity of S-RAM to be used, use these in order of CE1 ~ CE4 pins. At time of the CPU control, these pins are placed in the high impedance state.
$\overline{CE}$	34	Output	-	Output	-	RAM chip enable output terminal. Used at time of memory expansion. At time of the CPU control, this pin is placed in the high impedance state by the DMA function.
R/W	43	Output	-	Output	-	RAM read/write output terminal. Connect to S-RAM R/W pin. At time of the CPU control, this pin is placed in the high impedance state by the DMA function.
ALE	44	Output	-	Output	-	Memory expansion output terminal. Indicates output timing of the internal address counter A15 ~ A19 of the TC8830F to the A0 ~ A4 pins.
STBY	39	Input	None	Input	None	Standby input terminal. The TC8830F is placed in the standby state when this pin is set at "H" level.

PIN NAME	PIN NO.	CONSTRUCTION				FUNCTION
		MANUAL CONTROL		CPU CONTROL		
		I/O	PULL-UP PULL-DOWN	I/O	PULL-UP PULL-DOWN	
XIN XOUT	40 41	Input Output	None -	Input Output	None -	Oscillation circuit input/output terminals. Connect a 512kHz ceramic oscillator and a capacitor. In case of external clock input, supply it to the XIN pin and keep the XOUT pin open.
$\overline{ACL}$	56	Input	Pull-up	Input	Pull-up	Reset signal input terminal.
MICIN	59	Input	None	Input	None	MIC AMP1 input terminal.
C1	60	Output	-	Output	-	MIC AMP1 output terminal.
C2	63	Output	None	Input	None	MIC AMP2 input terminal.
MICOUT	64	Output	-	Output	-	MIC AMP2 output terminal.
ADI	65	Input	None	Input	None	Voice analysis circuit input terminal.
DAO	66	Output	-	Output	-	D/A converter output terminal.
FILIN	67	Input	None	Input	None	Band-pass filter input terminal.
FILOUT	1	Output	-	Output	-	Band-pass filter output terminal.
Vref	58	Output	-	Output	-	Analog circuit reference voltage output terminal.
TEST	3	Input	Pull-up	Input	Pull-down	Test circuit terminal. Connect nothing to this pin.
VDD	27 61	Power supply	-	Power supply	-	Power supply terminal. Supply +5V.
VSS1 VSS2	20 62	Power supply	-	Power supply	-	Power supply terminal. Connect to GND of power source. VSS1 is for the digital circuit, while VSS2 is for the analog circuit.

[8] PIN CONNECTIONS

FLAT PACKAGE 67 PIN

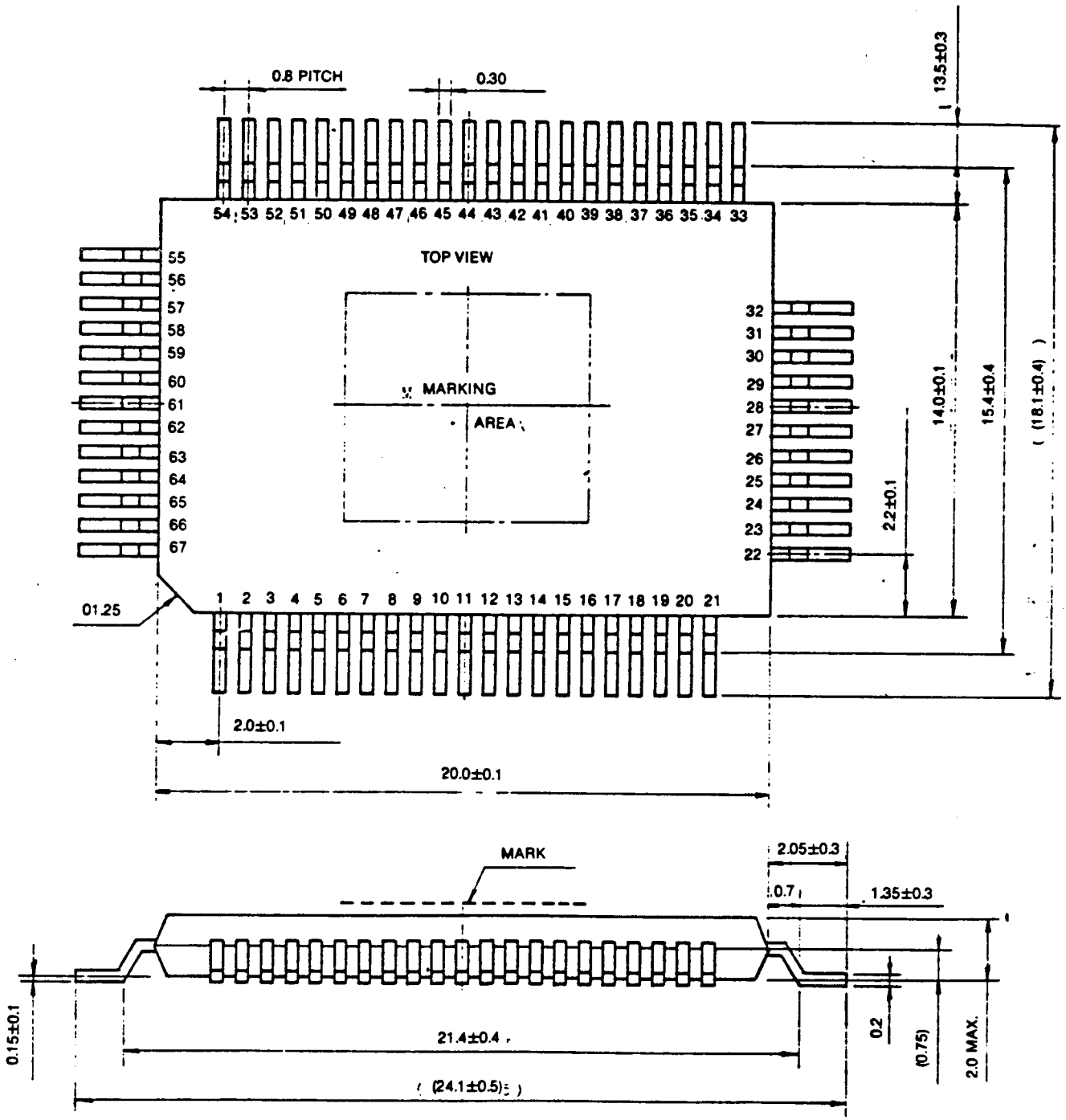


1	FILOUT	18	A13	35	$\overline{CE1}$	52	P2
2	N.C.	19	A12	36	$\overline{CE2}$	53	P1
3	TEST	20	VSS1	37	$\overline{CE3}$	54	P0
4	D7	21	A11	38	$\overline{CE4}$	55	EOS
5	N.C.	22	A10	39	STBY	56	$\overline{ACL}$
6	D6	23	A9	40	XIN	57	CPUM
7	N.C.	24	A8	41	XOUT	58	Vref
8	D5	25	A7	42	256K	59	MICIN
9	N.C.	26	A6	43	R/W	60	C1
10	D4	27	VDD	44	ALE	61	VDD
11	N.C.	28	A5	45	$\overline{WR}$	62	VSS2
12	N.C.	29	A4	46	$\overline{RD}$	63	C2
13	D3	30	A3	47	PH3	64	MICOUT
14	D2	31	A2	48	PH2	65	ADI
15	D1	32	A1	49	PH1	66	DAO
16	D0	33	A0	50	PH0	67	FILIN
17	A14	34	$\overline{CE}$	51	P3		

[9] OUTLINE DRAWINGS

67 PIN FLAT PACKAGE (67-4-BS)

Unit: mm



[10] ELECTRICAL CHARACTERISTICS

10.1 Absolute maximum raring

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply Voltage	$-0.3 \sim 6.5$	V
V_{IN}	Input Voltage	$-0.3 \sim V_{DD}+0.3$	V
V_{OUT}	Output Voltage	$-0.3 \sim V_{DD}+0.3$	V
T_{OPR}	Operating Temperature	$-10 \sim 55$	°C
T_{STG}	Storage Temperature	$-55 \sim 125$	°C

10.2 DC Characteristics (Unless otherwise specified, V_{DD}=5V 10%, Ta=25°C, V_{SS1}=V_{SS2}=0

SYMBOL	ITEM	APPLIED TERMINAL	TEST CONDITION	STANDARD VALUE MIN.	TYP.	MAX.	UNIT
f_{OPR}	Operating frequency		V_{DD}=4.5~6.5V	400	512	600	kHz
V_{OPR}	Operating supply voltage		f=400~600kHz	4.5	-	6.5	V
I_{DD1}	Consumption current (1)	V_{SS1} (Logic part)	At no load/ no signal	-	-	3.0	mA
I_{DD2}	Consumption current (2)	V_{SS2} (Analog part)	At no load/ no signal	-	-	3.0	
I_{DD3}	Consumption current at standby		At no load/ no signal*	-	-	3.0	μA
V_{IH}	Input high voltage	All input terminals		3.4	-	-	V
V_{IL}	Input low voltage			-	-	0.60	
V_{OH}	Output High voltage	P0~P3, D0~D7, ALE EOS, R/W, A0~A14 $\overline{CE}$, $\overline{CE1}$~$\overline{CE4}$	No load	4.2	-	-	
V_{OL}	Output low voltage		No load	-	-	0.3	
I_{OH}	Output high current	ALE, EOS, A0~A14 D0~D7, P0~P3, $\overline{CE}$ $\overline{CE1}$~$\overline{CE4}$, R/W	V_{OH}=2.4V TEST=256K=V_{DD}	0.4	-	-	mA
I_{OL}	Output low current	ALE, EOS, A0~A14 D0~D7, P0~P3, $\overline{CE}$ $\overline{CE1}$~$\overline{CE4}$, R/W	V_{OL}=0.4V TEST=V_{DD}	0.4	-	-	
I_{IH1}	Input high current (1)	P0~P3, PH0~PH3 $\overline{RD}$, $\overline{WR}$	V_{IH}=V_{DD} CPUM=V_{SS}	10	50	150	μA
I_{IH2}	Input high current (2)	P0~P3, PH0~PH3 $\overline{RD}$, $\overline{WR}$	V_{IH}=V_{DD} CPUM=V_{DD}	-	-	1.0	
I_{IH3}	Input high current (3)	TEST	V_{IH}=V_{DD}	50	100	500	
I_{IH4}	Input high current (4)	256K, STBY, CPUM	V_{IH}=V_{DD}	-	-	1.0	
I_{IH5}	Input high current (5)	A0~A14, D0~D7, $\overline{CE}$ $\overline{CE1}$~$\overline{CE4}$, R/W	V_{IH}=CPUM=V_{DD} $\overline{RD}$=$\overline{WR}$=V_{SS}	-	-	1.0	
I_{IL1}	Input low current (1)	P0~P3, PH0~PH3, RD, WR, TEST, 256K STBY, CPUM	V_{IL}=V_{SS}	-	-	1.0	
I_{IL2}	Input low current (2)	$\overline{ACL}$	V_{IL}=V_{SS}	-	-	1.0	
I_{IL3}	Input low current (3)	D0~D7	V_{IL}=V_{SS}	10	50	150	
I_{IL4}	Input low current (4)	A0~A14, D0~D7, $\overline{CE}$ $\overline{CE1}$~$\overline{CE4}$, R/W	CPUM=V_{DD} V_{IL}=$\overline{RD}$=$\overline{WR}$=V_{SS}	-	-	1.0	
V_{OUT1}	Output voltage (1)	VREF		-	2.8	-	V

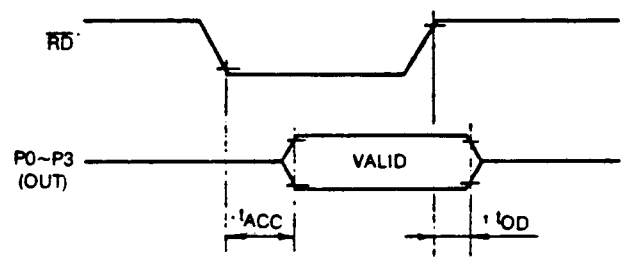
* STBY pin: V_{DD}+0.0[V], -0.2[V]

[NOTE] Max. and Min. values given are defined by their absolute values.

10.3 AC Characteristics

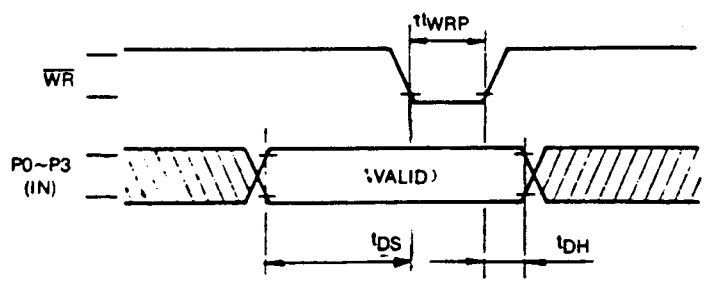
10.3.1 At data read

SYMBOL	ITEM	MIN.	MAX.	UNIT
t_{ACC}	Access time	400	-	ns
t_{OD}	Output disable time	-	300	ns



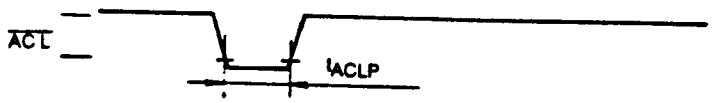
10.3.2 At data write

SYMBOL	ITEM	MIN.	MAX.	UNIT
t_{DS}	Data setup time	600	-	μs
t_{DH}	Data hold time	0	-	μs
t_{WRP}	$\overline{WR}$ pusle width	400	-	ns



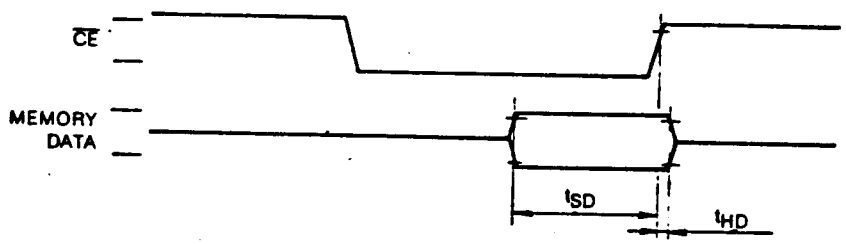
10.3.3 $\overline{ACL}$ pulse width

SYMBOL	ITEM	MIN.	MAX.	UNIT
t_{ACLP}	$\overline{ACL}$ pulse width	1	-	μs



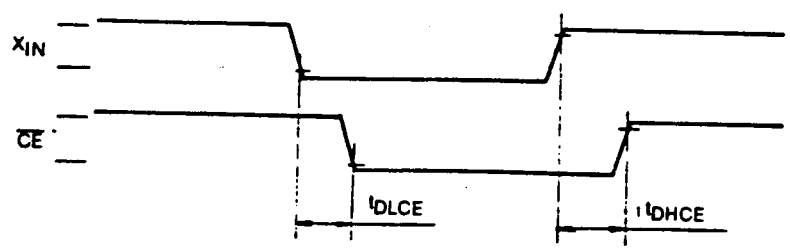
10.3.4 At memory data access

t_{SD}	Memory data setup time to $\overline{CE}$ rise	800	-	ns
t_{HD}	Memory data hold time	0	-	ns



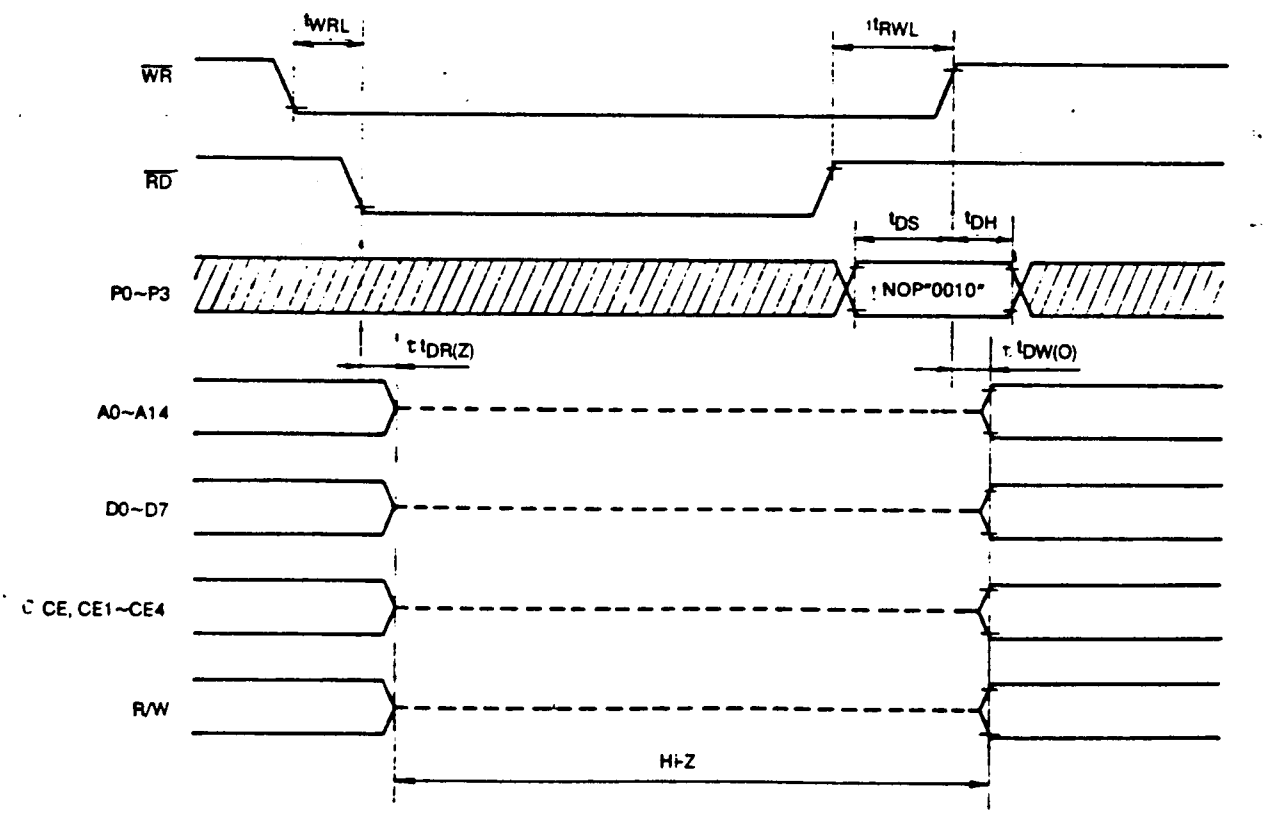
10.3.5 $\overline{CE}$ signal delay time

SYMBOL	ITEM	MIN.	MAX.	UNIT
t_{DLCE}	Delay time up to $\overline{CE}$ "L" to clock fall	-	400	ns
t_{DHCE}	Delay time up to $\overline{CE}$ "H" to clock rise	-	400	ns



10.3.6 DMA Function

SYMBOL	ITEM	MIN.	MAX.	UNIT
t_{WRL}	Time from $\overline{WR}$ fall to $\overline{RD}$ fall	100		ns
$t_{DR(Z)}$	Delay time from $\overline{RD}$ fall to Hi-Z		300	ns
t_{RWL}	Time from $\overline{RD}$ rise to $\overline{WR}$ rise	100		ns
$t_{DW(O)}$	Time from $\overline{WR}$ rise to Output state		300	ns
t_{DS}	Data setup time	1		μs
t_{DH}	Data Hold time	0		μs



10.4 Characteristics of analog part

(1) Microphone amplifier (Unless otherwise specified, $V_{SS1}=V_{SS2}=0V$, $V_{DD}=5.0V$, $Ta=25°C$, $f_{in}=1kHz$)

ITEM	APPLIED PIN	SYMBOL	TEST CONDITION	STANDARD VALUE			UNIT
				MIN.	TYP.	MAX.	
Pass band voltage gain	MICAMP1	V_{IN1}	$V_{IN}=6mVp-p$ $f_{in}=100Hz \sim 10kHz$ Output load 100kΩ 30pF	-	26	-	dB
	MICAMP2	V_{IN2}		-	20	-	
Total harmonic distortion	MICAMP1	V_{G1}	$V_{in}=6mVp-p$	-	2	-	%
	MICAMP2	V_{G2}		-	2	-	
Max. allowable input voltage	MICAMP1	V_{IN1}	-	-	-	200	mVp-p
	MICAMP2	V_{IN2}		-	-	400	
Input impedance	MICAMP1	R_{IN1}	-	-	30	-	kΩ
	MICAMP2	R_{IN2}		-	30	-	

(2) Band-pass filter (Unless otherwise specified, $V_{SS1}=V_{SS2}=0V$, $V_{DD}=5.0V$, $Ta=25°C$ $f_{in}=1kHz$)

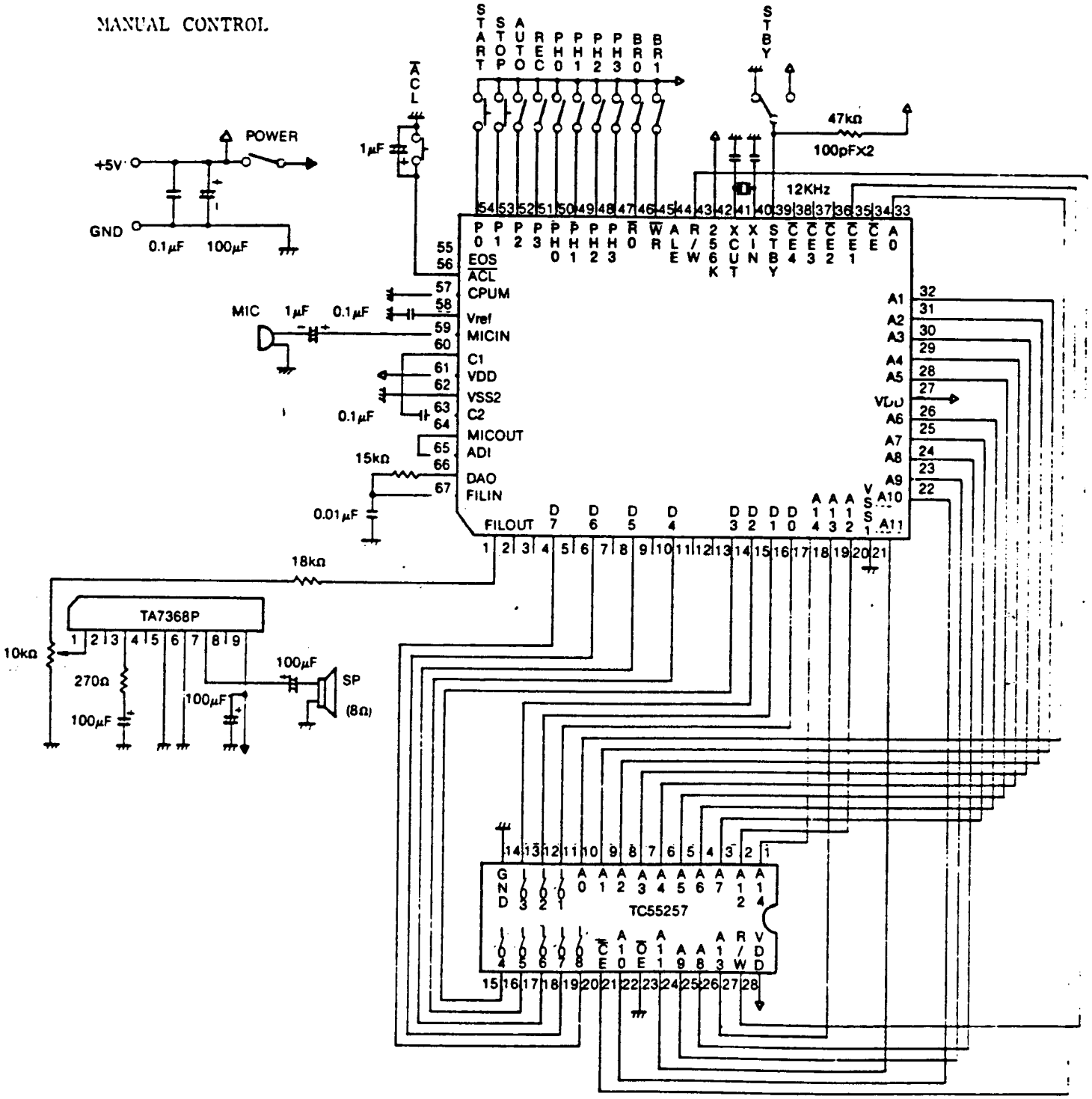
ITEM	SYMBOL	TEST CONDITION	STANDARD VALUE			UNIT
			MIN.	TYP.	MAX.	
Pass band voltage gain	V_G	$V_{IN}=1.0Vp-p$ Ouptut load 100kΩ 30pF	-	0	-	dB
Total harmonic distortion	THD	$V_{IN}=1.0Vp-p$	-	4	-	%
Max. allowable input voltage	V_{IN}		-	4.0	-	Vp-p
Output impedance	R_{OUT}		-	1	-	kΩ

(3) ADM analysis synthesize circuit (Unless otherwise specified, $V_{SS1}=V_{SS2}=0V$, $V_{DD}=5.0V$, $Ta=25°C$, $f_{in}=1kHz$)

ITEM	SYMBOL	TEST CONDITION	STANDARD VALUE			UNIT
			MIN.	TYP.	MAX.	
Max. allowable input voltage	V_{IN}	-	-	-	3.8	Vp-p

[11] EXAMPLE OF APPLICATION CIRCUIT

MANUAL CONTROL



* 0.1μF capacitor must be connected between V_{DD} and GND in S-RAM.

* On TC8830F, pins which are not connected must be opened.