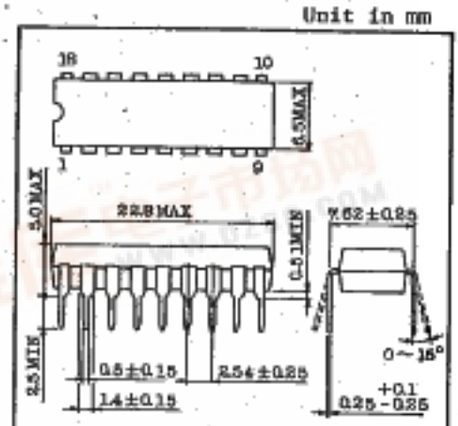
TENTATIVE

TC9106BP CB TRANSCEIVER PLL FREQUENCY SYNTHESIZER

- TC9106BP (C-MOS LSI) may be used a 40 channels CB transceiver frequency synthesizer.
- Included high speed programmable counter, operated direct division of VCO, can be used a simplified external circuit high quality PLL synthesizer in two-way.
- Outline is a 18 pin DIP.

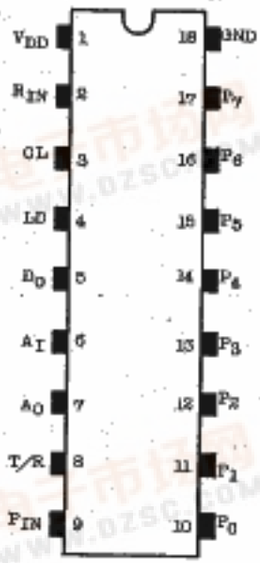
Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.18 leads.

JEDEC	—
TOSHIBA	5D18A-P

PIN CONNECTION



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +10	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V
Operation Temperature	Topr	-30 ~ 70	°C
Storage Temperature	Tstg	-55 ~ 125	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified V_{DD}=8V, R_{IN}=10.24MHz, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{DD}			7.5	8.0	8.5	V
Operating Supply Current	I_{DD}		V_{DD}=8V, f_{IN}=16MHz	-	18	25	mA
PROGRAMMABLE COUNTER							
Max. Operating Frequency	f_{MAX}		V_{DD}=7.5V	20	-	-	MHz
Min. Operating Input Voltage	$V_{IN(MIN)}$		f_{IN}=20MHz	2	-	-	Vp-p
REFERENCE FREQUENCY DIVIDER							
Max. Operating Frequency	f_{MAX}		V_{DD}=7.5V	12	-	-	MHz
Min. Operating Input Voltage	$V_{IN(MIN)}$		f_{IN}=12MHz	1	-	-	Vp-p
"H" LEVEL OUTPUT CURRENT							
D_O Output	I_{OH} D_O		V_{OH}=7V	-	0.3	-	mA
A_O Output	I_{OH} A_O						
CL Output	I_{OH} CL						
LD Output	I_{OH} LD						
"L" LEVEL OUTPUT CURRENT							
D_O Output	I_{OL} D_O		V_{OL}=1V	-	0.3	-	mA
A_O Output	I_{OL} A_O						
CL Output	I_{OL} CL		V_{OL}=8V	-	20	-	μA
LD Output	I_{OL} LD		V_{OL}=1V	-	0.3	-	mA
D_O TRI-STATE LEAKAGE							
Leakage Current "H" Level	I_{TLH} D_O			-	0.1	-	nA
Leakage Current "L" Level	I_{TLL} D_O						
AMPLIFIER							
Voltage Gain	G_V		f=5kHz	-	25	-	dB
Input Leakage Current "H" Level	I_{IH} A_I		V_{IH}=8V	-	0.1	-	nA
Input Leakage Current "L" Level	I_{IL} A_I		V_{IL}=0V				
P0 ∿ P7, T/R							
Pull Up/Down Resistance	R_{IN}			20	50	80	kΩ
High Level Input Voltage	V_{IH}			6	-	V_{DD}+0.3	V
Low Level Input Voltage	V_{IL}			-0.3	-	2.0	V

FEATURE

- Single X-tal (10.24MHz), All 40 channels CB transceiver.
- Direct division of VCO oscillation frequency due to high speed programmable counter, not necessary mixing down.
  The following Fig. 1 and Fig. 2 show the external circuit difference between present single X-tal type and TC9106BP (Toshiba new single X-tal). TC9106BP can simplify external circuit.

Fig. 1 PRESENT SINGLE X-TAL METHOD

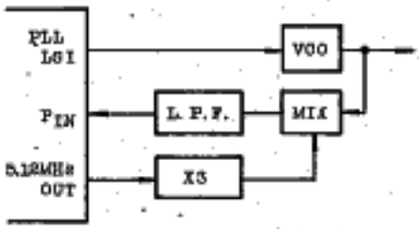
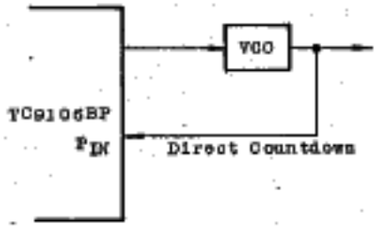


Fig. 2 TC9106BP DIRECT DIVISION METHOD



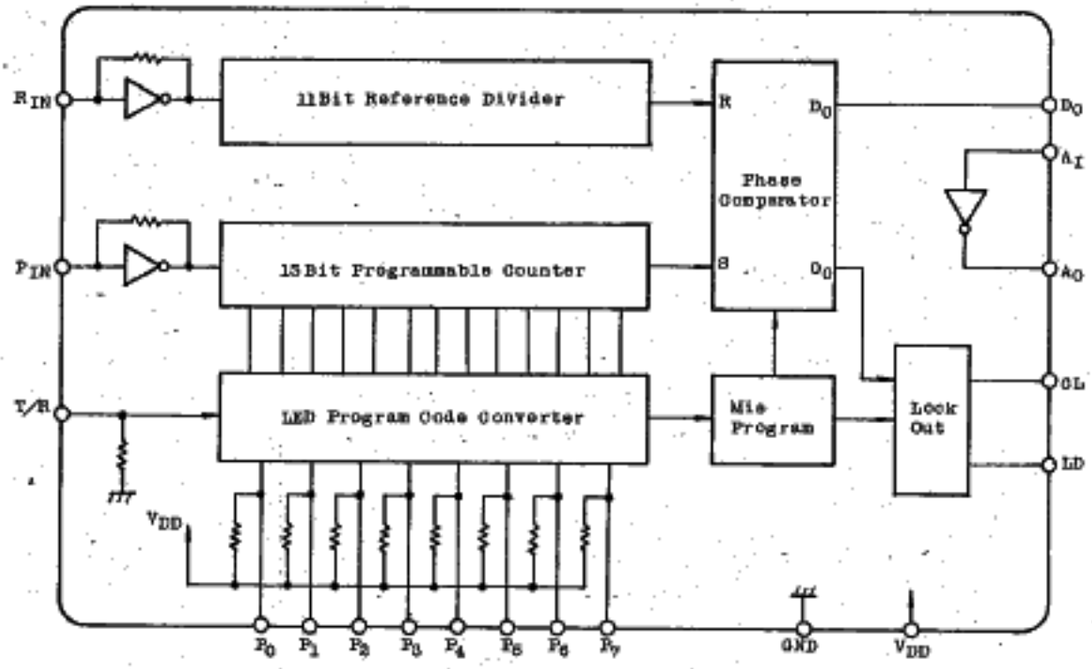
- Programmable counter has frequency devide shift function so that VCO oscillation frequency may shift 455kHz, equivalent to 2nd IF frequency, automatically be external switch.

- Can be programmed by 2 digit, 7 segment type LED drive code because of included code converter in internal channel selection program circuit. Therefore convenient to rotary switch/LED channel indicator type, and also can use conventional rotary switch.

- Included a detector of misprogram.
  Detected wrong program and can be stopped PLL function at the moment.

- Included a detector of lockout.
  When switched transmitting/receiving or channel, can detect instant lockout state, and make transmitting power hold for a short time. This hold time may by determinded by value of external capacitor. This function is effective as a audio muting against shock noise in channel change.

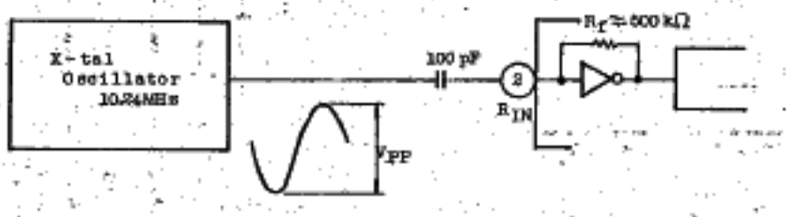
BLOCK DIAGRAM



BRIEF EXPLANATION OF EACH BLOCK PERFORMANCE

1. STANDARD FREQUENCY DIVIDER (11 BIT REFERENCE DIVIDER)

- Standard frequency divider generate 5kHz, PLL standard frequency by 11-stage binary counter (supplied 10.24MHz signal from R_{IN} terminal).
- R_{IN} input circuit has self-biased amplifier, input signal through a coupling capacitor is enough about 1 Vp-p sinesoidal wave.



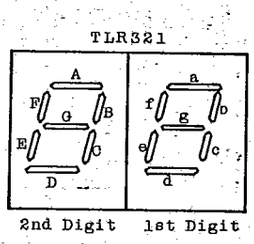
TC9106BP

2. PROGRAMMABLE COUNTER (13 BIT PROGRAMMABLE COUNTER)

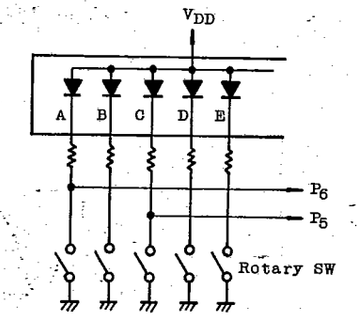
- Programmable counter is a 13 bit variable divider. Divided by indicated divide ratio from code converter binary code which is mentioned in following.
- TC9106BP has special high speed programmable counter, maximum operation frequency is higher than 20 MHz at V_{DD}=8V. Therefore can be divided directly by programmable counter without VCO oscillation frequency mixingdown in two ways.
- Divide range of programmable counter is 3345 ∿ 3433 division (in transmitting) and 3254 ∿ 3342 division (in receiving).
- Pin input has a self biased amplifier as like as R_{IN} input circuit. Therefore low input signal like higher than 2 Vp-p (16MHz) sinesoidal wave through a coupling capacitor is sufficient to operate it.

3. CODE CONVERTER

- P_0 ∿ P_7 channel selection are programmed by 2 digit, 7 segment LED indication code. Code converter include read only memory (ROM) to convert P_0 ∿ P_7 input code to 13 bit binary code.
- This code converter include control terminal (T/R) to shift 2139 from the standard programmable counter division number in two ways. Obtained 10.695 MHz in case standard frequency is 5 kHz for example. When T/R is L or open, it is receive-state, when T/R is H, it is transmit-state.
- P_0 ∿ P_7 input terminals include pull-up resistor respectively, read H level in case of open, lead connection between P_0 ∿ P_7 and LED is as follows.



P_0	f
P_1	a
P_2	g
P_3	e
P_4	d
P_5	C
P_6	A
P_7	F



4. MISPROGRAM DETECTOR

- Detect any wrong code except normal 1 ∿ 40 channels from input. When wrong code is detected, controlled lockout detector. This circuit changes LD output level to be L-level and makes phase converter performance stop simultaneously.
- Protect perfectly performance against any external interference, for instance cause by rotary switch wrong contact.

5. PHASE COMPARATER

- Phase comparater generates proper VCO control voltage, compared frequency and phase between 5 kHz, standard frequency, and programmable counter divided output signal.
- S and R input signal rise-phases are compared. When S input signal phase advances D_O output become to be H level, when delays D_O output become L level. Otherwise D_O output is held to be high impedance state.
- D_O terminal output signal controls VCO by converting DC level through low pass filter which has proper time constant.
  Performance waveforms in phase comparater are shown below.

FIG. 3 PHASE COMPARATER WAVEFORM

(Note) L_O output is supplied to detector.

6. LOCKOUT DETECTOR

- Detects lockout state and supplys L level signal to LD terminal when abnormal phenomena occur in external circuit, for example PLL lockout caused at channel. selection or on/off of press talk switch.
- LD terminal turns to L level in case that misprogram detector circuit operate like as lockout state.
- After lockout (L level), LD terminal is held for determinded period, then returns H level. The constant time period can be choosed by capacitor value between CL terminal and ground.
- To prevent wrong performance from external noise or vibration, designed to operate at the condition more than 10 sec., pulse width of L_O signal L level. (equivalent to that lockout detector operates at more than about $\pm 20°$, phase difference between S and R input phase.
- Fig. 4 shows logic diagram of lockout detector, Fig. 5 shows waveform.

FIG. 4 LOGIC DIAGRAM

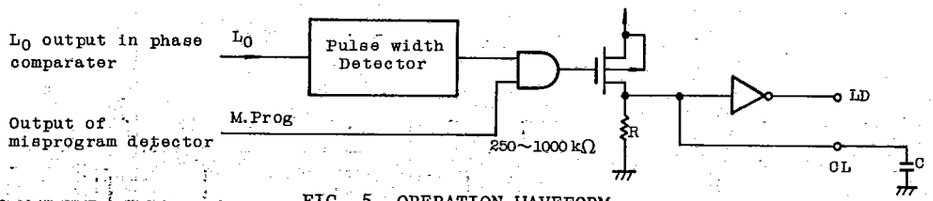
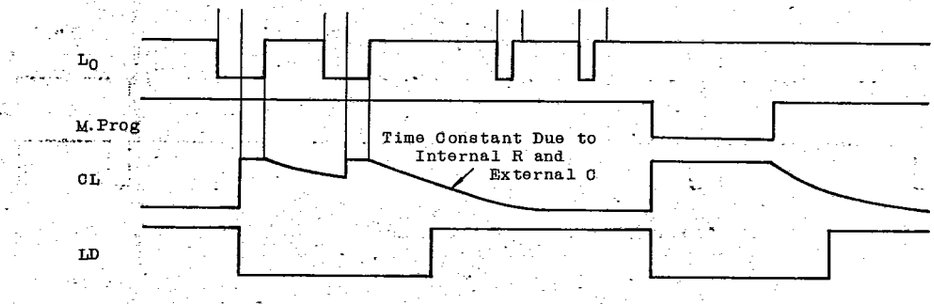


FIG. 5 OPERATION WAVEFORM



TC9106BP

T-50-17

PROGRAM CODE TABLE (Note) o show "H" level $f_{VCO}=N\times0.005$ (MHz)

CHANNEL NUMBER	PROGRAM CODE								R/T=L (RECEIVE)		R/T=H (TRANSMIT)	
	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	N	f_{VCO}	N	f_{VCO}
1	o	o	o	o	o	o	o	o	3254	16.27	3345	16.725
2	o					o	o	o	3256	16.28	3347	16.735
3	o			o		o	o	o	3258	16.29	3349	16.745
4		o		o	o	o	o	o	3262	16.31	3353	16.765
5				o		o	o	o	3264	16.32	3355	16.775
6		o				o	o	o	3266	16.33	3357	16.785
7	o		o	o	o	o	o	o	3268	16.34	3359	16.795
8						o	o	o	3272	16.36	3363	16.815
9				o	o	o	o	o	3274	16.37	3365	16.825
10			o				o	o	3276	16.38	3367	16.835
11	o	o	o	o	o		o	o	3278	16.39	3369	16.845
12	o						o	o	3282	16.41	3373	16.865
13	o			o			o	o	3284	16.42	3375	16.875
14		o		o	o		o	o	3286	16.43	3377	16.885
15				o			o	o	3288	16.44	3379	16.895
16		o					o	o	3292	16.46	3383	16.915
17	o		o	o	o		o	o	3294	16.47	3385	16.925
18							o	o	3296	16.48	3387	16.935
19				o	o		o	o	3298	16.49	3389	16.945
20			o			o		o	3302	16.51	3393	16.965
21	o	o	o	o	o	o		o	3304	16.52	3395	16.975
22	o					o		o	3306	16.53	3397	16.985
23	o			o		o		o	3312	16.56	3403	17.015
24		o		o	o	o		o	3308	16.54	3399	16.995
25				o		o		o	3310	16.55	3401	17.005
26		o				o		o	3314	16.57	3405	17.025
27	o		o	o	o	o		o	3316	16.58	3407	17.035
28						o		o	3318	16.59	3409	17.045
29				o	o	o		o	3320	16.60	3411	17.055
30			o					o	3322	16.61	3413	17.065
31	o	o	o	o	o			o	3324	16.62	3415	17.075
32	o							o	3326	16.63	3417	17.085
33	o			o				o	3328	16.64	3419	17.095
34		o		o	o			o	3330	16.65	3421	17.105
35				o				o	3332	16.66	3423	17.115
36		o						o	3334	16.67	3425	17.125
37	o		o	o	o			o	3336	16.68	3427	17.135
38								o	3338	16.69	3429	17.145
39				o	o			o	3340	16.70	3431	17.155
40			o				o		3342	16.71	3433	17.165

(Note) Rotary switch $P_0 \sim P_7$: None-mark is "ON", o-mark is "OPEN"

TC9106BP

T-50-17

PERFORMANCE AGAINST WRONG-PROGRAM

o TC9106BP include a program data code ROM, respectively only 40 channel, regulated by FCC rules.
Any external channel selection program can determine the data out of the programmable counter in the IC directly, and cannot generate the any other frequency except only formal 40 channel frequencies.

o TC9106BP include eight program input terminals because of LED drive code. SO these are 256 combinations due to eight inputs theoretically, however, this IC is designed to detect only formal 40 channel combinations. At the other combinations, this IC detects wrong code combinations or mis-programs, then make a phase comparator performance in the IC stop and transmitting output of two way radio is cut off by generated lockout signal at the moment.

o As the above mentioned, TC9106BP is designed to prevent any abnormal performances and interferences perfectly due to channel selection failure, illegal modification, or any other malfunctions.

Following are an explanation on circuit performance.
When the 8 bit channel data is put into ROM-1, if the channel data is one of normal 1 ∿ 40 channel, output of ROM-1 is sent to ROM-2 and the output of NOR gate is L-level
When the input channel data is the wrong except normal 1 ∿ 40 channel, the NOR output changes H-level.
At the same time, this circuit changes LD output level to be L-level and make phase comparator performance stop.

TC9106BP

T-50-17

PROGRAM CODE DETECTOR BLOCK DIAGRAM