

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC9223P, TC9223F

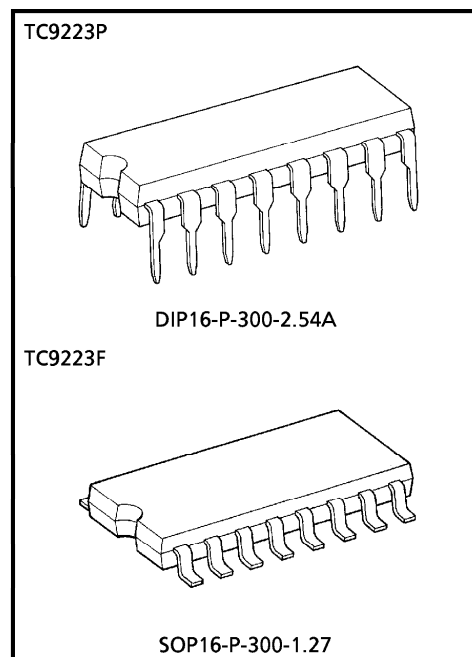
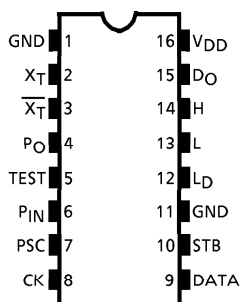
## PLL FREQUENCY SYNTHESIZER LSI FOR COMMUNICATION USE

TC9223P, TC9223F are developed as PLL frequency synthesizer LSI for communication use and has the following features.

### FEATURES

- Can be used as PLL LSI in many communication equipment, e.g., personal radio, mobile radio telephone, CB radio and so on because of its system design for wide applications.
- With a built-in 14bit reference frequency divider, capable of frequency division ranging from 5 to 16,383 divisions.
- Built-in 7bit and 11bit programmable dividers of pulse swallow type.
- Provided with 2 systems of phase comparator outputs.
- Provided with one general purpose output port.
- PSC (Prescaler Control) output can be switched according to input signal rising or falling timing by program.
- DIP16pin and SOP16pin packages.

### PIN CONNECTION

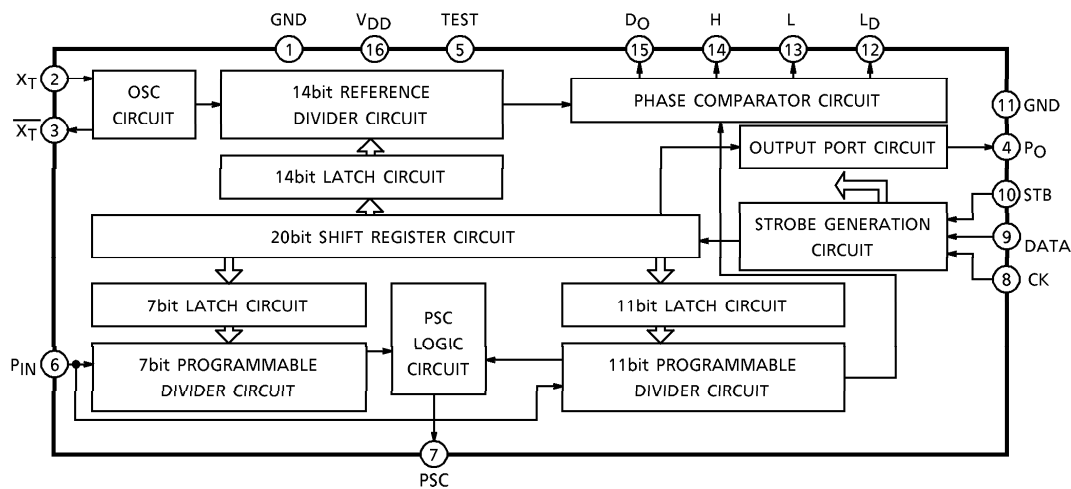


Weight  
 DIP16-P-300-2.54A : 1.00g (Typ.)  
 SOP16-P-300-1.27 : 0.16g (Typ.)

980910EBA2

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BLOCK DIAGRAM



PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1	GND	Ground-1	Logic ground terminal.	—
2	$X_T$	Crystal oscillator terminal	Reference frequency crystal oscillator input and output.	Feedback resistor built in
3	$\overline{X_T}$			
4	$P_O$	General purpose output port	General purpose output port externally controllable by serial data.	CMOS output
5	TEST	Test terminal	Used normally at "L" level or Open state. Test mode operation at "H" level.	Pull-down resistor built in
6	PIN	Programmable counter input	Programmable counter input terminal. Input an external prescaler output through a coupling capacitor.	Built in amps
7	PSC	Prescaler control	2 modulus prescaler frequency division control signal output. "H" level : P, "L" level : P + 1	CMOS output
8	CK	Serial data input	Serial data input terminals to control this LSI externally.	Built in schmitt trigger circuit
9	DATA			
10	STB		Schmitt trigger input.	
11	GND	Ground-2	Ground terminal of phase comparator charge pump.	—
12	$L_D$	Lock detector	Outputs "H" level pulse when phase difference is detected by the phase comparator. Can be set compulsorily by data given externally.	CMOS output
13	L	Phase comparator output	Phase comparator output terminals to connect external high voltage charge pump.	CMOS output N-ch open drain output
14	H			
15	$D_O$	Phase comparator charge pump output	$D_O$ is tri-state output.	—
16	$V_{DD}$	Power supply	+5V power supply terminal.	—

**OPERATION**

1. Serial data input

Serial data can control 4 group functions separately. Data is always input from LSB and final 2 bits data selects the group.

- Group 1 — Reference divider frequency division ratio
- Group 2 — Programmable counter frequency division ratio
- Group 3 — PSC control  
Phase comparator S, R inputs replace
- Group 4 — General purpose output ports  
Lock detector compulsory set

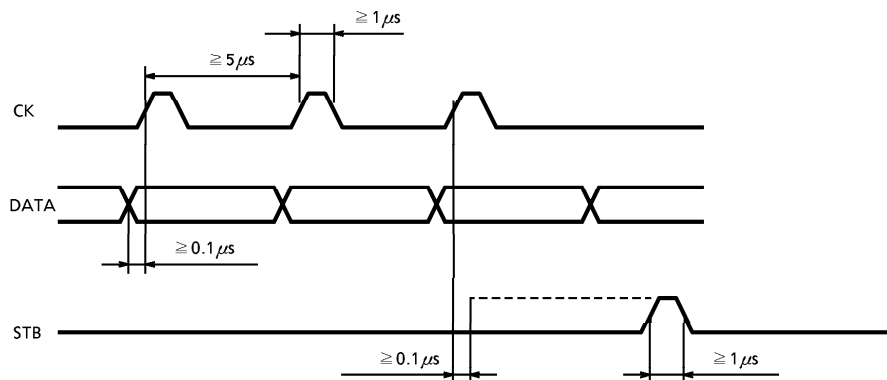
The serial data input circuit is composed of 3 lines of DATA, CK and STB. Data is taken in order into the internal shift register at the leading edge of CK.

By setting STB at "H" level after all data are input, data are transferred to the latch selected by the group code and this LSI is controlled.

Each of 3 serial data input terminals has a built-in Schmitt trigger circuit that prevent data error by noise, etc.

For details of data construction of each group, refer to the explanations of respective blocks.

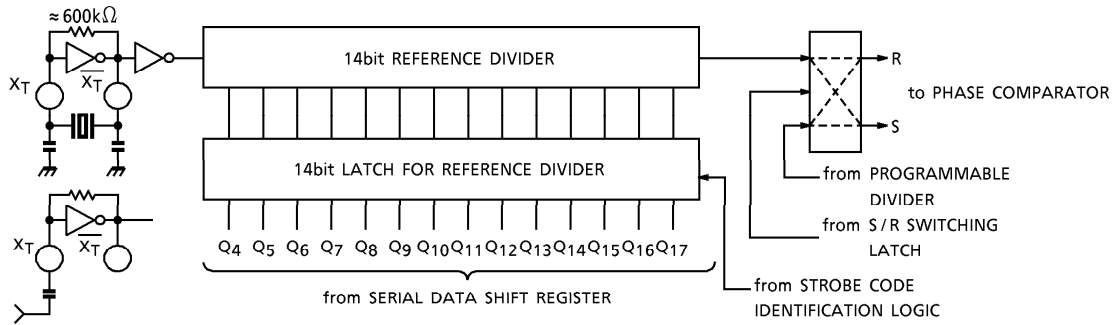
- Serial data transfer timing



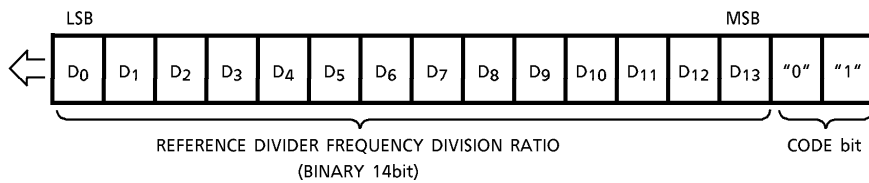
(\*) Set a time from the last CK rising to STB rising at  $0.1 \mu s$  or above.

2. Reference divider

This block generates PLL reference frequency and is composed of an amplifier for a crystal oscillator and 14bit programmable divider.



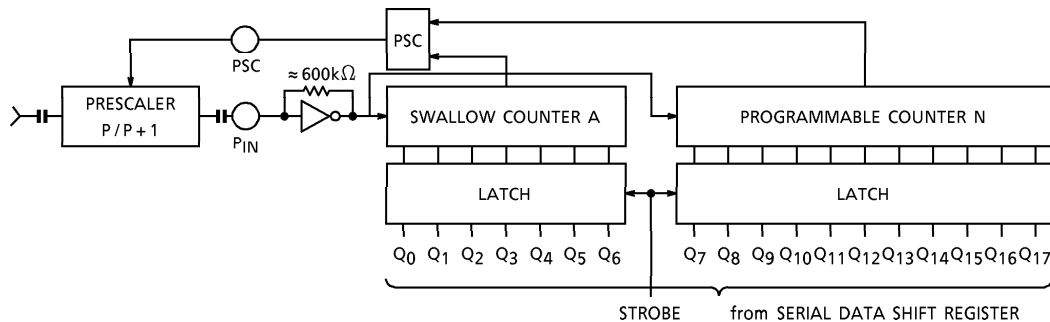
- The programmable divider is composed of binary 14 bits and is capable frequency division from 5 to 16,383 divisions by serial data given externally. Therefore, a crystal needed to generate reference frequency is freely selectable and common use of the crystal for other purpose is also possible.
- Serial data to control reference divider block is of 16 bits as following construction.



(\*)  $D_0 \sim D_{13}$  is binary code N of frequency division ratio intended.  
 $5 \leq N \leq 16,383$

3. Programmable counter

Programmable counter circuit adopts swallow system to generate high frequency and is composed of 7 bits swallow counter, 11 bits programmable counter and prescaler control logic to switch frequency division ratio of 2 modulus prescaler connected externally.



- Total frequency division ratio is defined as below.

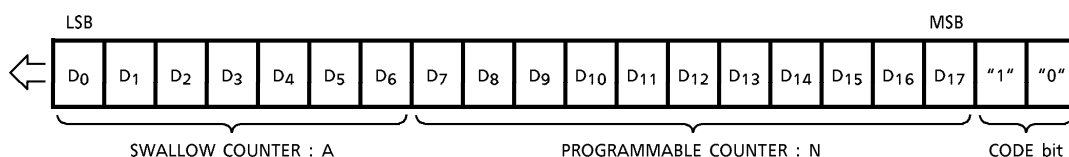
$$\begin{aligned} \text{Frequency division ratio} &= (P + 1) \cdot A + P \cdot (N - A) \\ &= P \cdot N + A \end{aligned} \quad (\text{Note}) \quad N > A$$

- Frequency division ratio of the external prescaler should be "P + 1" when PSC is "L" level and "P" when PSC is "H" level.

- Serial data

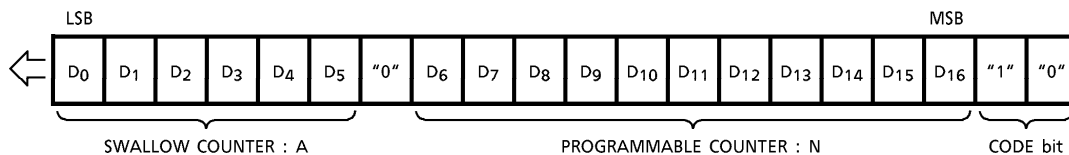
Serial data which defines frequency division ratio of programmable counter is composed of 20bits but changes according to "P" of external prescaler.

- (1) When used with an external prescaler of P = 128



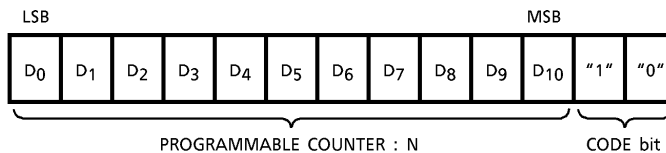
(\*) D<sub>0</sub>~D<sub>17</sub> is binary code D of frequency division ratio intended.  
Generally 16,384 ≤ D ≤ 262,143

- (2) When used with an external prescaler of P = 64



(\*) D<sub>0</sub>~D<sub>16</sub> is binary code D of frequency division ratio intended.  
The 7th bit should be fixed at "L".  
Generally 4,096 ≤ D ≤ 131,071

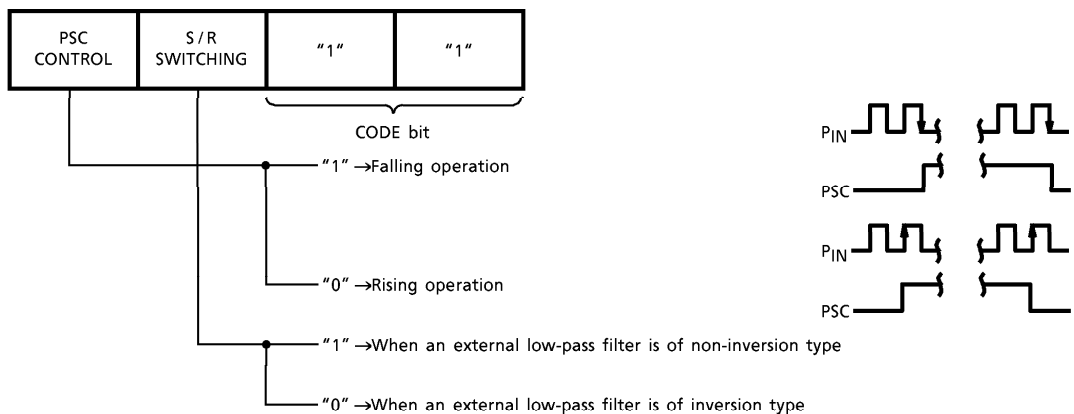
- (3) When used as a normal programmable counter



(\*) D<sub>0</sub>~D<sub>10</sub> is binary code D of frequency division ratio intended.  
5 ≤ D ≤ 2,047

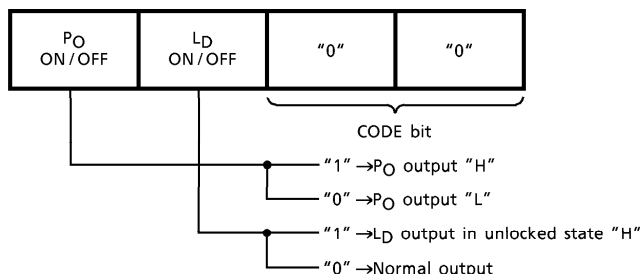
4. Inversion of S/R input to PSC control / phase comparator

- PSC control  
 "PSC" (prescaler) output is capable of switching operation according to rising or falling timing of "P<sub>IN</sub>" input signal.
- Inversion of S/R inputs to phase comparator  
 S/R switching bit is a control latch for mutual replacement of reference divider output and programmable divider output when they are led to the phase comparator.
- Serial data



5. General purpose output port/lock detector

- General purpose output port  
 "P<sub>O</sub>" output port is available for many functions, e.g., transmitter/receiver switching signal, band switching signal, sensitivity switching and frequency band switching according to serial data.
- Lock detector  
 The lock detector output pulse signal for a phase difference time detected by the phase detector circuit.  
 In addition, this lock detector output can be fixed in the unlocked state by force by serial data given externally.  
 By fixing the lock detector in the unlocked state immediately before channel changing to stop transmission output and releasing the detector from the unlocked state at a definite time after the channel change, troubles at channel changing, e.g., by overshoot can be prevented.
- Serial data



**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	-0.3~7.0	V
Input Voltage	V <sub>IN</sub>	-0.3~V <sub>DD</sub> +0.3	V
Power Dissipation	P <sub>D</sub>	300	mW
Operating Temperature	T <sub>opr</sub>	-40~85	°C
Storage Temperature	T <sub>stg</sub>	-65~150	°C

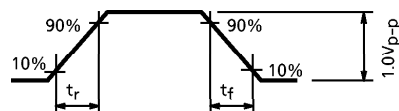
**ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V<sub>DD</sub> = 5V)**

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V <sub>DD</sub>	—	f <sub>X<sub>T</sub></sub> = 30MHz, 0.5V <sub>p-p</sub> f <sub>p IN</sub> = 30MHz, 1.0V <sub>p-p</sub> (*)	4.5	5.0	5.5	V
Operating Supply Current	I <sub>DD</sub>	—	f <sub>X<sub>T</sub></sub> = 30MHz, 0.5V <sub>p-p</sub> f <sub>p IN</sub> = 30MHz, 1.0V <sub>p-p</sub> (*)	—	15.0	20.0	mA
Operating Input Frequency	f <sub>X<sub>T</sub>1</sub>	—	V <sub>DD</sub> = 4.5~5.5V, V <sub>IN</sub> = 0.5V <sub>p-p</sub> (Note 1)	1.0	—	30.0	MHz
	f <sub>X<sub>T</sub>2</sub>	—	V <sub>DD</sub> = 3.0V, V <sub>IN</sub> = 0.5V <sub>p-p</sub> (Note 1)	1.0	—	10.0	
	f <sub>p IN1</sub>	—	V <sub>DD</sub> = 4.5~5.5V, V <sub>IN</sub> = 1.0V <sub>p-p</sub> (Note 2)	0.1	—	30.0	
	f <sub>p IN2</sub>	—	V <sub>DD</sub> = 3.0V, V <sub>IN</sub> = 1.0V <sub>p-p</sub> (Note 2)	0.1	—	10.0	
X'tal Oscillation Frequency	f <sub>OSC</sub>	—	V <sub>DD</sub> = 4.5~5.5V (Note 3)	1.0	—	30.0	MHz
Operating Input Voltage	V <sub>X<sub>T</sub></sub>	—	V <sub>DD</sub> = 4.5~5.5V	0.5	—	V <sub>DD</sub>	V <sub>p-p</sub>
	V <sub>p IN</sub>	—	V <sub>DD</sub> = 4.5~5.5V	1.0	—	V <sub>DD</sub>	
Input Voltage	"H" Level	V <sub>IH</sub>	CK, DATA, STB	3.8	—	5.0	V
	"L" Level	V <sub>IL</sub>		0.0	—	1.2	
Input Current	"H" Level	I <sub>IH</sub>	CK, DATA, STB	V <sub>IH</sub> = 5V		1.0	μA
	"L" Level	I <sub>IL</sub>		V <sub>IL</sub> = 0V		-1.0	
Breakdown Voltage	V <sub>OH</sub>	—	I <sub>OH</sub> ≤ 0.1μA	—	—	12.0	V
Tri-State Off-Leak Current	I <sub>OZ</sub>	—	D <sub>O</sub> V <sub>OH</sub> = 5V, V <sub>OL</sub> = 5V	-0.1	—	0.1	μA
Output Current	"H" Level	I <sub>OH1</sub>	D <sub>O</sub> , L V <sub>OH</sub> = 4V	—	-1.0	-0.5	mA
	"L" Level	I <sub>OL1</sub>	D <sub>O</sub> , H, L V <sub>OL</sub> = 1V	0.5	1.0	—	
	"H" Level	I <sub>OH2</sub>	L <sub>D</sub> , P <sub>SC</sub> , P <sub>O</sub> V <sub>OH</sub> = 4V	—	-1.5	-1.0	
	"L" Level	I <sub>OL2</sub>	L <sub>D</sub> , P <sub>SC</sub> , P <sub>O</sub> V <sub>OL</sub> = 1V	1.0	1.5	—	
Input Frequency	f <sub>CK</sub>	—	CK	—	—	200	kHz

(\*) Ta = -40~85°C

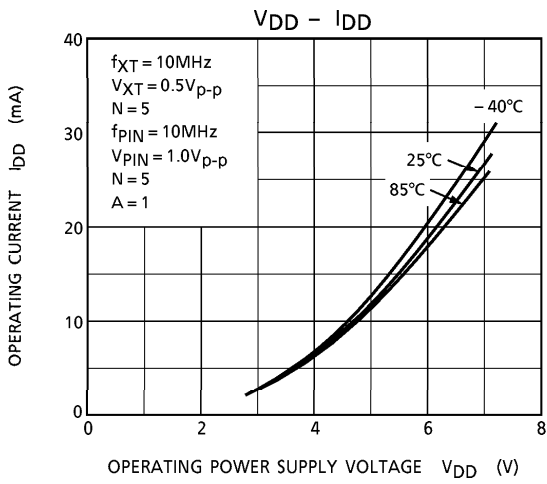
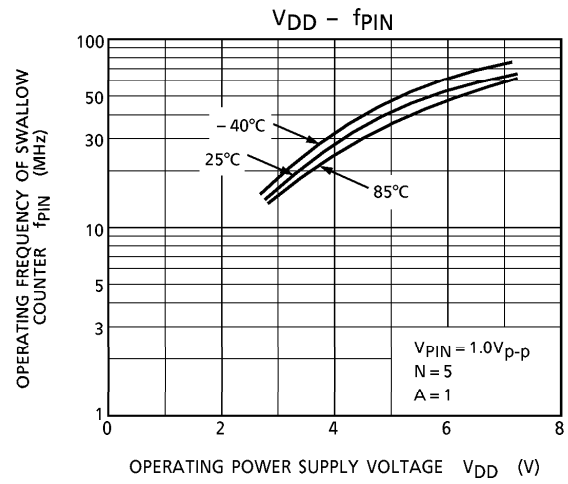
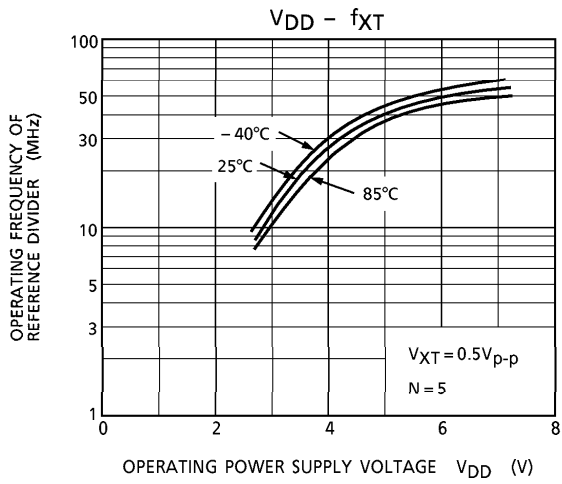
(Note 1) X<sub>T</sub> is SIN wave input.

(Note 2) P<sub>IN</sub> is SQ wave input. Rising and falling slopes of input waveform are specified as follows.



(\*) tr = tf < 200ns

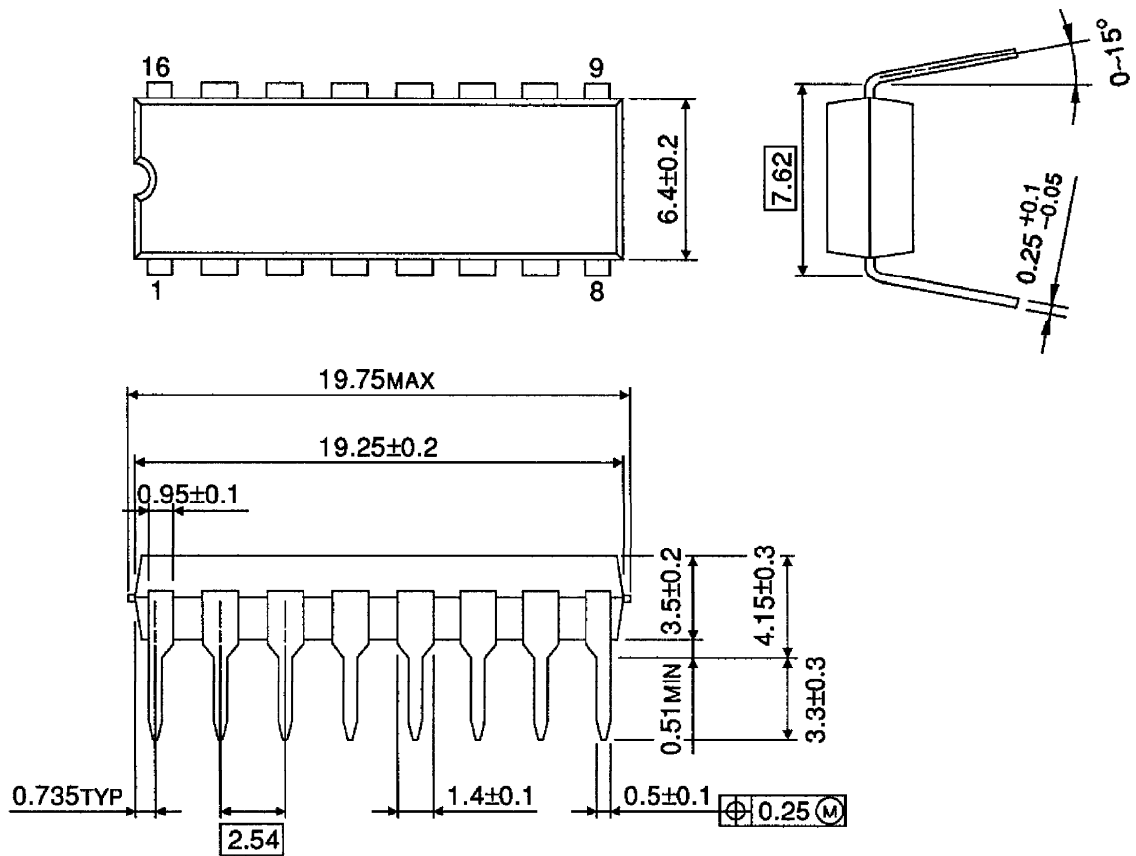
(Note 3) Use a crystal oscillator that has a low CI value and a good starting characteristic.





**OUTLINE DRAWING**  
DIP16-P-300-2.54A

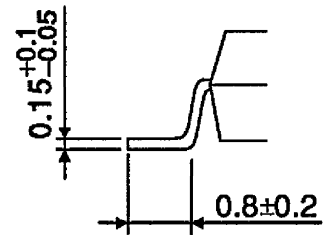
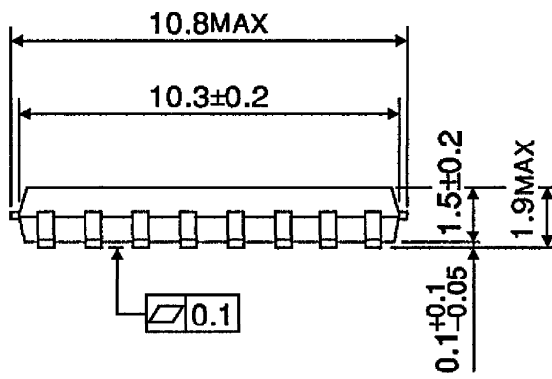
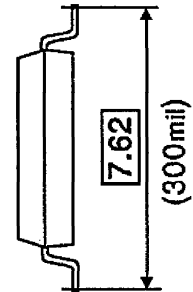
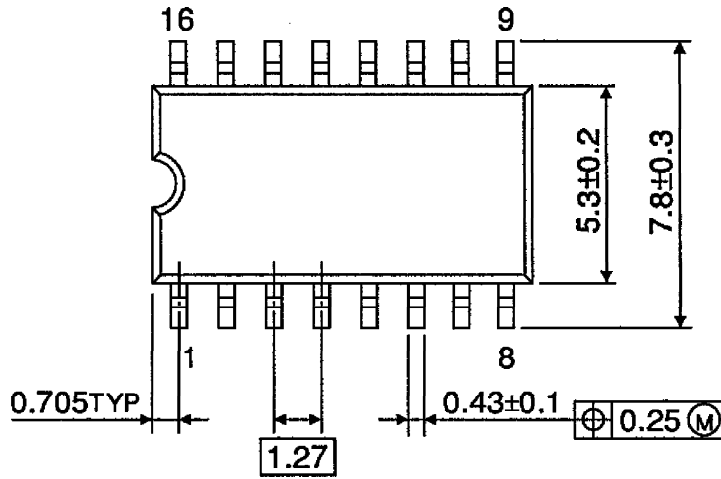
Unit : mm



Weight : 1.00g (Typ.)

**OUTLINE DRAWING**  
SOP16-P-300-1.27

Unit : mm



Weight : 0.16g (Typ.)

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