

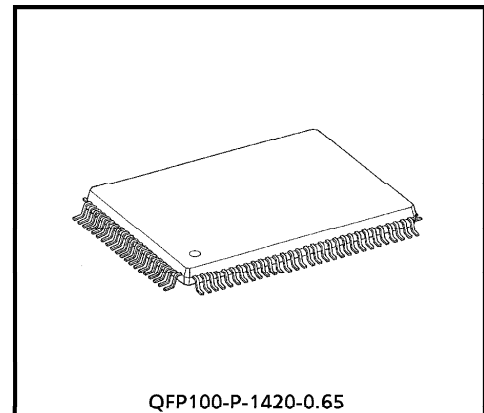
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9296AF

DIGITAL SERVO SINGLE CHIP PROCESSOR BUILT IN 1 BIT DA CONVERTER

The TC9296AF is a single chip processor which incorporates the following function : synchronous separation protection and interpolation, EFM demodulation, Error correction, microcontroller interface, digital equalizer for use in servo LSI and servo control circuit.

In addition, the TC9296AF incorporates a 1 bit DA converter. In combination with the head amplifier TA2066F for digital servo, the TC9296AF allows simplified, adjustment-free structuring of CD player system.



QFP100-P-1420-0.65

Weight : 1.6g (Typ.)

FEATURES

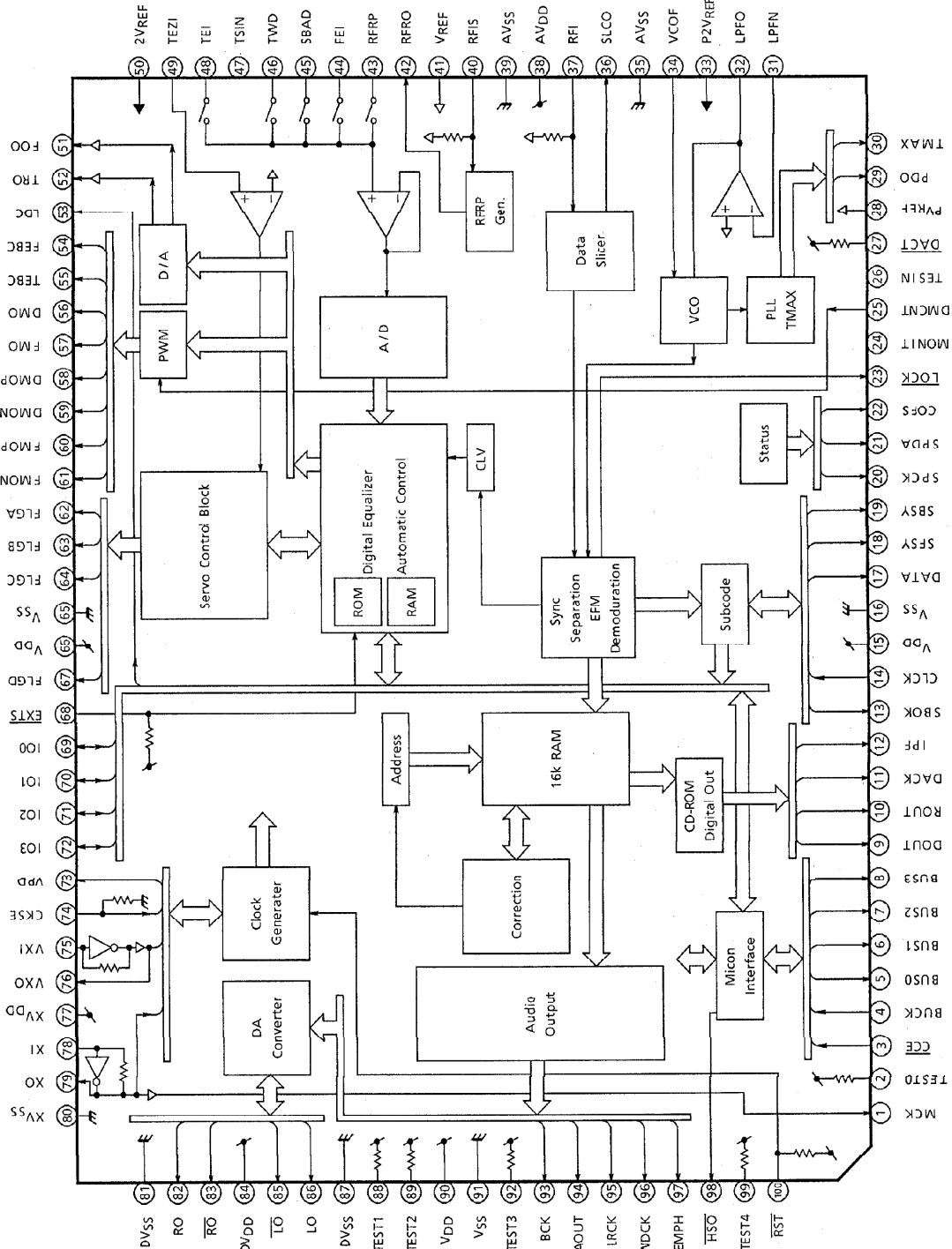
- Sync pattern detection, sync signal protection and synchronization can be made correctly.
- Built in EFM demodulation circuit, subcode demodulation circuit.
- Capable of correcting dual C1 correction and triple C2 correction using the CIRC correction theoretical format.
- Jitter absorbing capacity of ± 6 frames.
- Built in 16K RAM.
- Built in digital out circuit.
- Built in variable pitch control circuit.
- Built in digital peak meter circuit.
- Built in L/R independent digital attenuator.
- Audio output responds to bilingual function.
- Reed timing free subcode Q data and capable of synchronous output with audio data.
- Built in data slicer and analog PLL (free-adjustment VCO).
- Capable of automatic adjustment function of focus servo and tracking servo, offset, loop gain and balance.

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- Built in digital equalizer for phase compensation.
- Built in RAM for digital equalizer coefficient and capable of variable pickup.
- Built in focus, tracking servo control circuit.
- Search control corresponds to every mode and can realize high speed and stable search.
- Built in AFC circuit and APC circuit for CLV servo of disc motor.
- Built in defect and shock-free circuit.
- Built in 8 times oversampling digital filter and 1 bit DA converter.
- Soft mute function.
- Capable of double speed operation.
- Built in microcontroller interface circuit.
- CMOS silicon structure and high speed, low power consumption.
- 100 pin flat package.

BLOCK DIAGRAM (TOP VIEW)



PIN FUNCTION

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
1	MCK	O	Internal master clock output terminal.	
2	TEST0	I	Test terminal. Normally set either to "H" or open.	With pull-up resistor
3	\overline{CCE}	I	Chip enable for microcontroller interface. The bus line becomes active at "L".	Schmitt input
4	BUCK	I	Data sending/receiving clock input terminal.	
5	BUS0	I/O	Data input/output terminal for microcontroller interface.	Schmitt input Open drain output With pull-up resistor
6	BUS1			
7	BUS2			
8	BUS3			
9	DOUT	O	Digital output terminal.	
10	ROUT	O	CD-ROM data output terminal.	
11	DACK	O	CD-ROM data reading clock output terminal. This can be select 2.8/5.6MHz by command.	
12	IPF	O	Correction flag output terminal. It turns to "H" when AOUT output is unable to correct C ₂ correction.	
13	SBOK	O	Output terminal of CRCC judgment result of subcode Q data. It turns "H" when CRCC judgment is OK.	
14	CLCK	I	Input terminal for subcode P-W data reading clock.	
15	V _{DD}	—	Digital supply voltage terminal. (+ 5V)	
16	V _{SS}	—	Digital ground terminal.	
17	DATA	O	Output terminal subcode P-W data.	
18	SFSY	O	Regenerated frame sync signal output.	
19	SBSY	O	Subcode block sync signal output.	
20	SPCK	O	Processor status signal reading clock output terminal. (176.4kHz)	
21	SPDA	O	Processor status signal output terminal.	
22	COFS	O	Correction frame clock output terminal. (7.35kHz)	
23	\overline{LOCK}	O	Lock status output terminal. It turns to "H" when sync pattern of 17ms during EFM signal are not detected consecutively.	
24	MONIT	O	LSI internal signal monitor terminal.	
25	DMCNT	I	DMOP, DMON terminal mode setting terminal. This outputs AFC and APC errors at "L".	With pull-up resistor
26	TESIN	I	Test input terminal.	
27	\overline{DACT}	I	Test input terminal. Normally set either to "H" or open.	With pull-up resistor

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS								
28	PVREF	—	PLL reference supply voltage terminal. (V_{REF})									
29	PDO	O	Phase difference signal output terminal of EFM signal and PLCK signal.	3-state output ($2V_{REF}$, V_{REF} , AV_{SS})								
30	TMAX	O	TMAX detection output terminal.	3-state output ($2V_{REF}$, V_{REF} , AV_{SS})								
			<table border="1"> <thead> <tr> <th>DETECTION RESULT</th> <th>TMAX OUTPUT</th> </tr> </thead> <tbody> <tr> <td>Longer than</td> <td>"AV_{SS}"</td> </tr> <tr> <td>Shorter than fixed freq.</td> <td>"$2V_{REF}$"</td> </tr> <tr> <td>Within the fixed freq.</td> <td>"V_{REF}"</td> </tr> </tbody> </table>		DETECTION RESULT	TMAX OUTPUT	Longer than	" AV_{SS} "	Shorter than fixed freq.	" $2V_{REF}$ "	Within the fixed freq.	" V_{REF} "
			DETECTION RESULT		TMAX OUTPUT							
			Longer than		" AV_{SS} "							
Shorter than fixed freq.	" $2V_{REF}$ "											
Within the fixed freq.	" V_{REF} "											
31	LPFN	I	Inversion input terminal of LPF amplifier.	Analog input								
32	LPFO	O	Inversion output terminal of LPF amplifier.	Analog output								
33	P2VREF	—	PLL reference supply voltage terminal. ($2V_{REF}$)									
34	VCOF	O	VCO filter terminal.									
35	AV_{SS}	—	Analog ground terminal.									
36	SLCO	O	Data slice level output terminal.	Analog output								
37	RFI	I	RF signal input terminal.	Analog input								
38	AV_{DD}	—	Analog supply voltage terminal. (+5V)									
39	AV_{SS}	—	Analog ground terminal.									
40	RFIS	I	RFRP detection input terminal.	Analog input								
41	V_{REF}	—	Analog reference supply voltage terminal.									
42	RFRO	O	RFRP detection output terminal.	Analog output								
43	RFRP	I	RF ripple signal input terminal.	Analog input								
44	FEI	I	Focus error signal input terminal.	Analog input								
45	SBAD	I	Sub beam adder signal input terminal.	Analog input								
46	TWD	I	Window comparator input terminal.	Analog input								
47	TSIN	I	Test input terminal. Normally set either to "H" or open.	With pull-up resistor								
48	TEI	I	Tracking error signal input terminal.	Analog input								
49	TEZI	I	Tracking error zero input terminal.	Analog input								
50	$2V_{REF}$	—	Analog reference supply voltage terminal.									
51	FOO	O	Focus servo equalizer output terminal.	Analog output								
52	TRO	O	Tracking servo equalizer output terminal.	Analog output								
53	LDC	O	ALPC circuit ON/OFF signal output terminal. It outputs "H" when laser ON.									
54	FEBC	O	Focus balance control signal output terminal. It outputs PWM signal of 3-state. (PWM carrier : 88.2kHz)	3-state output ($2V_{REF}$, V_{REF} , AV_{SS})								

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
55	TEBC	O	Tracking balance control signal output terminal. It outputs PWM signal of 3-state. (PWM carrier : 88.2kHz)	3-state output (2V _{REF} , V _{REF} , AV _{SS})
56	DMO	O	Disc motor equalizer output terminal. It outputs PWM signal of 3-state. (PWM carrier : 88.2kHz)	3-state output (2V _{REF} , V _{REF} , AV _{SS})
57	FMO	O	Feed moter equalizer output terminal. It outputs PWM signal of 3-state. (PWM carrier : 88.2kHz)	3-state output (2V _{REF} , V _{REF} , AV _{SS})
58	DMOP	O	Disc motor equalizer output terminal. It outputs PWM signal when + polarity. (PWM carrier : 88.2kHz)	2-state output (V _{DD} , V _{SS})
59	DMON	O	Disc motor equalizer output terminal. It outputs PWM signal when - polarity. (PWM carrier : 88.2kHz)	2-state output (V _{DD} , V _{SS})
60	FMOP	O	Feed motor equalizer output terminal. It outputs PWM signal when + polarity. (PWM carrier : 88.2kHz)	2-state output (V _{DD} , V _{SS})
61	FMON	O	Feed motor equalizer output terminal. It outputs PWM signal when - polarity. (PWM carrier : 88.2kHz)	2-state output (V _{DD} , V _{SS})
62	FLGA	O	External flag terminal for internal signal.	
63	FLGB			
64	FLGC			
65	V _{SS}	—	Digital ground terminal.	
66	V _{DD}	—	Digital power supply voltage terminal. (+5V)	
67	FLGD	O	External flag terminal for internal signal.	
68	$\overline{\text{EXTS}}$	I	External shock signal input terminal. It makes tracking equalizer gain up mode when at "L".	With pull-up resistor
69	IO0	I/O	General I/O port.	
70	IO1			
71	IO2			
72	IO3			
73	VPD	O	Phase comparator output terminal of variable pitch control.	3-state output (V _{DD} , HiZ, V _{SS})
74	CKSE	I	X'tal selection terminal. It is "L" at 16.9344MHz and "H" at 33.8688MHz.	
75	VXI	I	Clock input terminal for variable pitch VCO.	Analog input
76	VXO	O	VXI terminal input buffer output terminal.	

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
77	XVDD	—	X'tal oscillation circuit power supply voltage terminal. (+5V)	
78	XI	I	X'tal oscillation circuit input terminal.	
79	XO	O	X'tal oscillation circuit output terminal.	
80	XVSS	—	X'tal oscillation circuit ground terminal.	
81	DVSS	—	Analog ground terminal for DA converter R channel.	
82	RO	O	R channel data output terminal.	
83	\overline{RO}	O	R channel data inversion output terminal.	
84	DVDD	—	DA converter supply voltage terminal. (+5V)	
85	\overline{LO}	O	L channel data inversion output terminal.	
86	LO	O	L channel data output terminal.	
87	DVSS	—	Analog ground terminal for DA converter L channel.	
88	TEST1	I	Test terminal. Normally set either "H" or open.	With pull-up resistor
89	TEST2	I	Test terminal. Normally set either "H" or open.	With pull-up resistor
90	VDD	—	Digital supply voltage terminal. (+5V)	
91	VSS	—	Digital ground terminal.	
92	TEST3	I	Test terminal. Normally set either "H" or open.	With pull-up resistor
93	BCK	O	Bit clock output terminal. (1.4122MHz)	
94	AOUT	O	Audio data output terminal.	
95	LRCK	O	Channel clock output terminal. It outputs "L" when L channel and "H" when R channel. The output polarity can be invertible by command.	
96	WDCK	O	Word clock output terminal. (88.2kHz)	
97	EMPH	O	Subcode Q data emphasis flag output terminal. It turns to "H" when emphasis ON and "L" when OFF. The output polarity can be invertible by command.	
98	\overline{HSO}	O	Double speed mode output terminal. It outputs "H" when normal speed and "L" when double speed.	
99	TEST4	I	Test terminal. Normally set either "H" or open.	With pull-up resistor
100	\overline{RST}	I	Reset signal input terminal. It turns to "L" when resetting.	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V _{DD}	-0.3~5.5	V
Input Voltage	V _{IN}	-0.3~V _{DD} +0.3	V
Power Dissipation	P _D	1250	mW
Operating Temperature	T _{opr}	-25~75	°C
Storage Temperature	T _{stg}	-55~150	°C

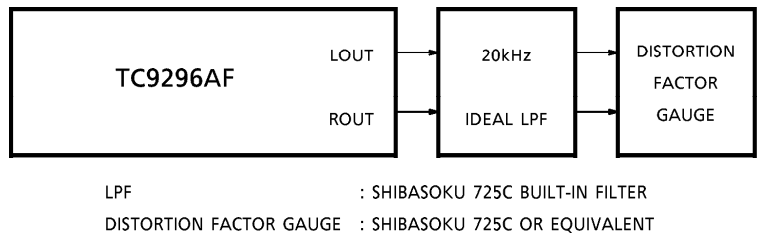
DC CHARACTERISTICS (Unless otherwise specified, V_{DD} = 5V, 2V_{REF} = 4.2V, V_{REF} = 2.1V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Operating Supply Voltage	V _{DD}	—		4.75	5.0	5.25	V	
Operating Supply Current	I _{DD}	—	XI = 16.9344MHz, In normal mode	—	55	90	mA	
Input Voltage	"H" Level	V _{IH}	—	CMOS input terminals except analog input terminal	3.5	—	—	V
	"L" Level	V _{IL}						
Input Current	"H" Level	I _{IH}	—	V _{IH} = 5V V _{IL} = 0V	—	—	1.0	μA
	"L" Level	I _{IL}						
Try State Leak Current	"H" Level	I _{TLH}	—	V _{IH} = 5V V _{IL} = 0V	④ Terminal	—	—	1.0
	"L" Level	I _{TLL}						
Output Current	"H" Level	I _{OH}	—	V _{OH} = 4.6V	① Terminal	—	—	-1.0
	"L" Level	I _{OL}	—	V _{OL} = 0.4V		2.0	—	—
	"H" Level	I _{OH}	—	V _{OH} = 4.6V	② Terminal	—	—	-1.0
	"L" Level	I _{OL}	—	V _{OL} = 0.4V		2.0	—	—
	"H" Level	I _{OH}	—	V _{OH} = 3.8V	③ Terminal	—	—	-1.0
	"L" Level	I _{OL}	—	V _{OL} = 0.4V		1.0	—	—
V _{REF} Output ON Resistance	R _{ON}	—		—	—	500	Ω	
Pull-Up Resistance	R _{UP} (1)	—	⑤ Terminal	25.0	50.0	75.0	kΩ	
	R _{UP} (2)	—	BUS3~BUS0	8.0	20.0	32.0		
Pull-Down Resistance	R _{DW}	—	CKSE	25.0	50.0	75.0	kΩ	
Osc.Amp.Feedback Resistance	R _N	—	XI XO between	2.0	4.0	6.0	MΩ	

	TERMINAL NAME	CONDITION
① Terminal	MCK, BUS0, BUS1, BUS2, BUS3, DOUT, ROUT, DACK, TMAX, FMOP, FMON, DMOP*, DMON*, FLGA, FLGB, FLGC, FLCD, VPD, BCK, AOUT, LRCK, WDCK	V _{DD} = 5.0V, V _{force} = 4.6 / 0.4V (*) DMOP, DMON (DMCNT = "H")
② Terminal	IPF, SBOK, DATA, SFSY, SBSY, SPCK, SPDA, COFS, LOCK, MONIT, LDC, IO0, IO1, IO2, IO3, EMPH, HSO	
③ Terminal	FEBC, TEBC, FMO, DMO, DMOP*, DMON*	2V _{REF} = 4.0V, V _{force} = 3.8 / 0.4V (*) DMOP, DMON (DMCNT = "L")
④ Terminal	TMAX, IO0, IO1, IO2, IO3, VPD	V _{DD} = 5.0V, V _{force} = 4.6 / 0.4V
⑤ Terminal	DMCNT, DACT, EXTS, RST, TEST0~TEST4	

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Total Harmonic Distortion + Noise	THD + N	1	1kHz sine wave Full-scale input	—	- 85	- 80	dB
S / N Ratio	S / N	1		90	98	—	dB
Dynamic Range	DR	1	1kHz sine wave - 60dB input conversion	90	95	—	dB
Cross-talk	CT	1	1kHz sine wave Full-scale input	—	- 95	- 85	dB

TEST CIRCUIT 1 : Application circuit example-2 is used.



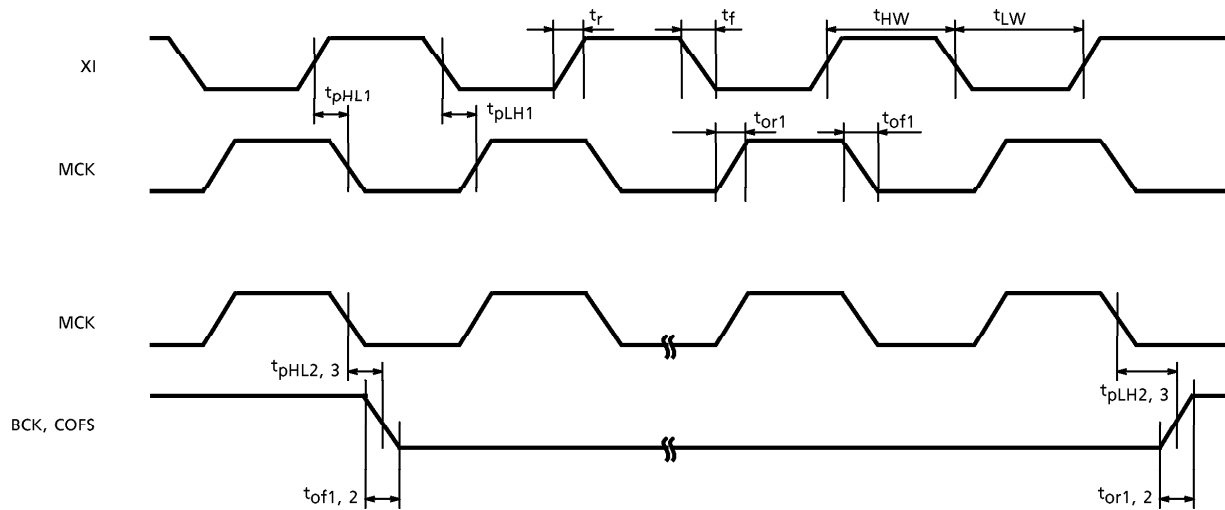
MEASURING ITEM	DISTORTION FACTOR GAUGE FILTER SETTING A WEIGHT
THD + N, CT	OFF
S / N, DR	ON

A WEIGHT : IEC-A OR EQUIVALENT

AC CHARACTERISTICS

Clock system timing

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Clock Width	"H" Level	t_{HW}	—	XI input	18	—	—	ns		
	"L" Level	t_{LW}			18	—	—			
Input Rising Time		t_r			—	—	—		10	ns
Input Falling Time		t_f			—	—	—		10	
Transfer Time (1)	"H" Level	t_{pHL1}	—	XI→MCK	—	—	60	ns		
	"L" Level	t_{pLH1}			—	—	60			
Transfer Time (2)	"H" Level	t_{pHL2}	—	MCK→BCK	—	—	60			
	"L" Level	t_{pLH2}			—	—	60			
Transfer Time (3)	"H" Level	t_{pHL3}	—	MCK→COFS	—	—	100			
	"L" Level	t_{pLH3}			—	—	100			
Output Rising Time (1)		t_{or1}	—	MCK, BCK	—	—	15	ns		
Output Falling Time (1)		t_{of1}			—	—	—		15	
Output Rising Time (2)		t_{or2}	—	COFS	—	—	40	ns		
Output Falling Time (2)		t_{of2}			—	—	—		40	

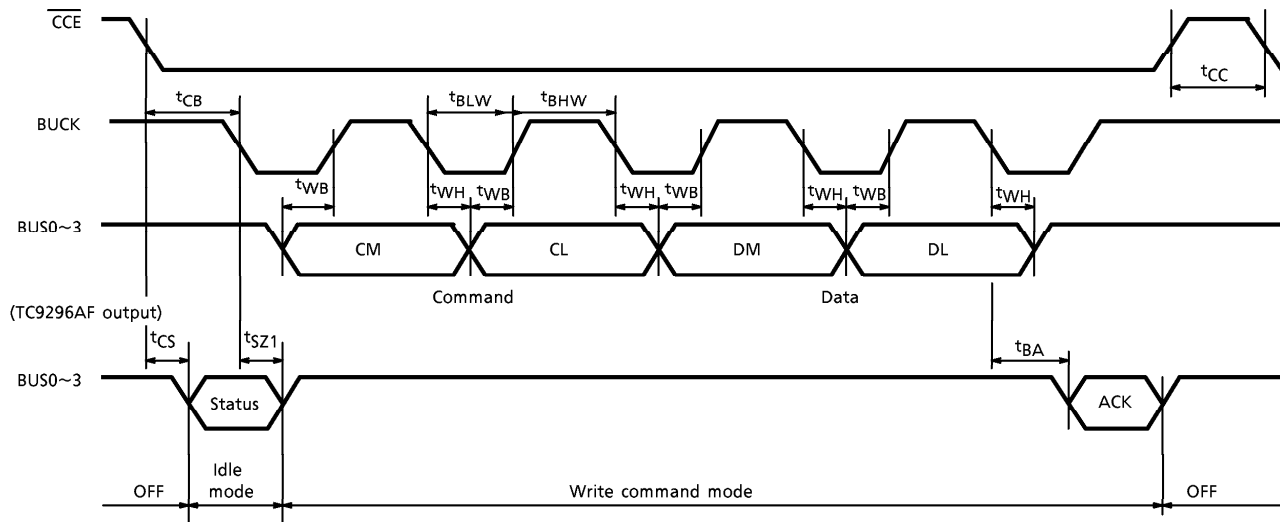


MICROCONTROLLER INTERFACE

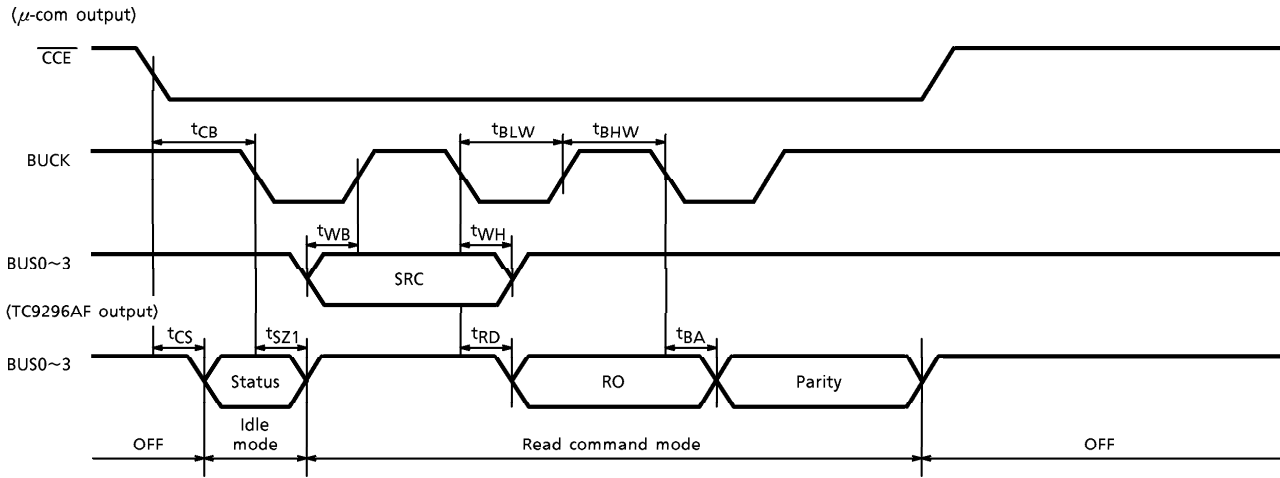
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
BUCK Clock Width	"H" Level	t _{BHW}	—	WRITE, SRC mode	1.0	—	—	μs
			—	QDRC mode (× 1)	6.0	—	—	
	—		QDRC mode (× 2)	3.0	—	—		
	"L" Level	t _{BLW}	—		1.0	—	—	
CCE "H" Clock Pulse Width		t _{CC}	—	CCE falling reference	1.0	—	—	
CCE, BUCK Delay Time		t _{CB}	—	CCE rising reference	0	—	—	
CCE Status Data Access Time		t _{CS}	—	CCE falling reference	—	—	0.1	
Write Data Setup Time		t _{WB}	—	BUCK rising reference	0	—	—	
Write Data Hold Time		t _{WH}	—	BUCK falling reference	0.5	—	—	
Read Data Access Time		t _{RD}	—	BUCK falling reference	0.4	—	0.5	
ACK Data Access Time		t _{BA}	—	BUCK falling reference	0.4	—	0.5	
Status Data Disable Time		t _{SZ1}	—	CCE falling Reference	0.4	—	0.5	
Data Disable Time		t _{SZ2}	—	→Status output	—	—	0.1	

(a) Write command mode

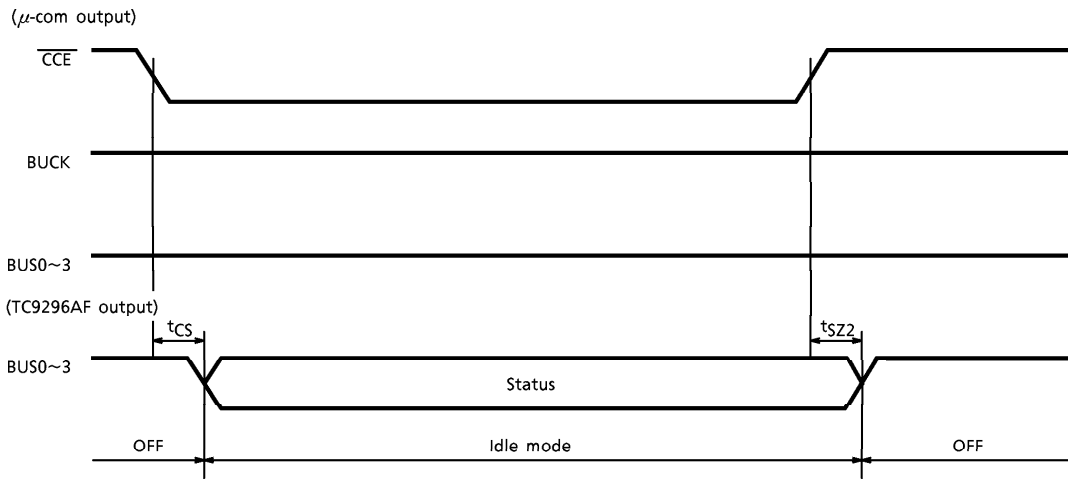
(μ-com output)



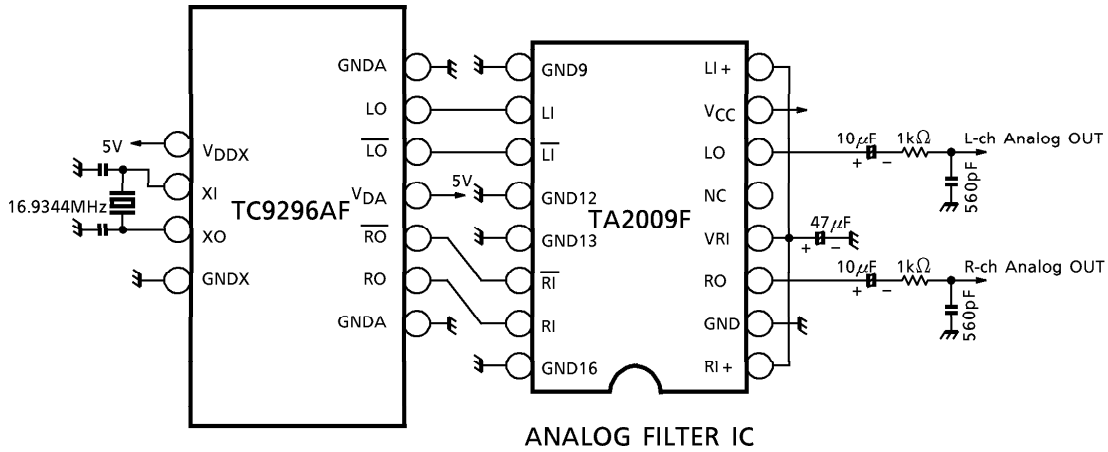
(b) Read command mode



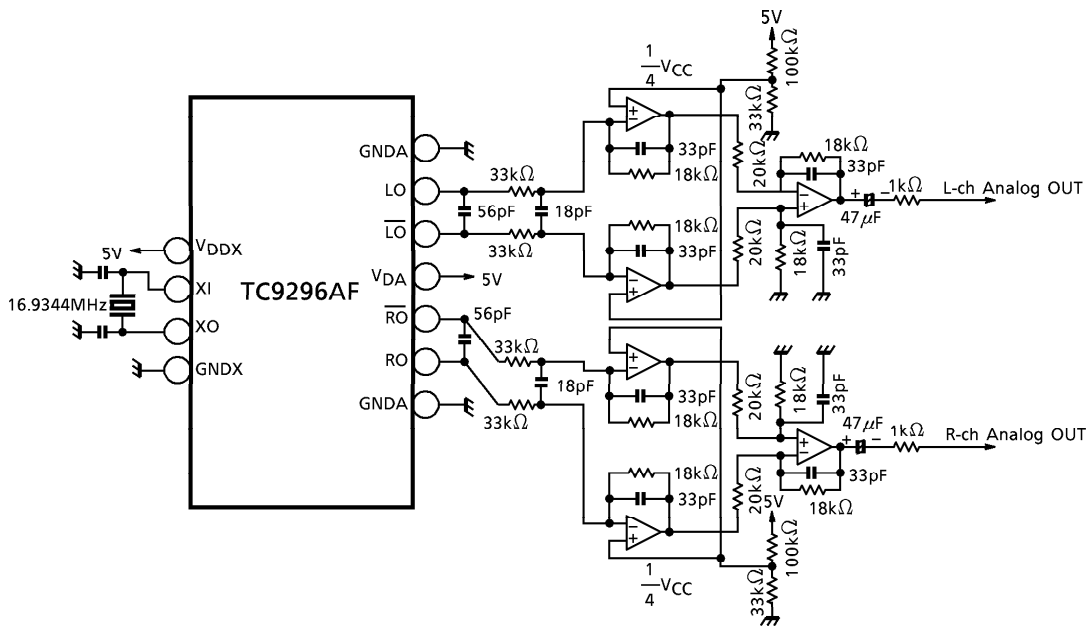
(c) Idle mode



APPLICATION CIRCUIT EXAMPLE-1 (+ 5V single power supply used)



APPLICATION CIRCUIT EXAMPLE-2 ($\pm 5V$ two power supply used)



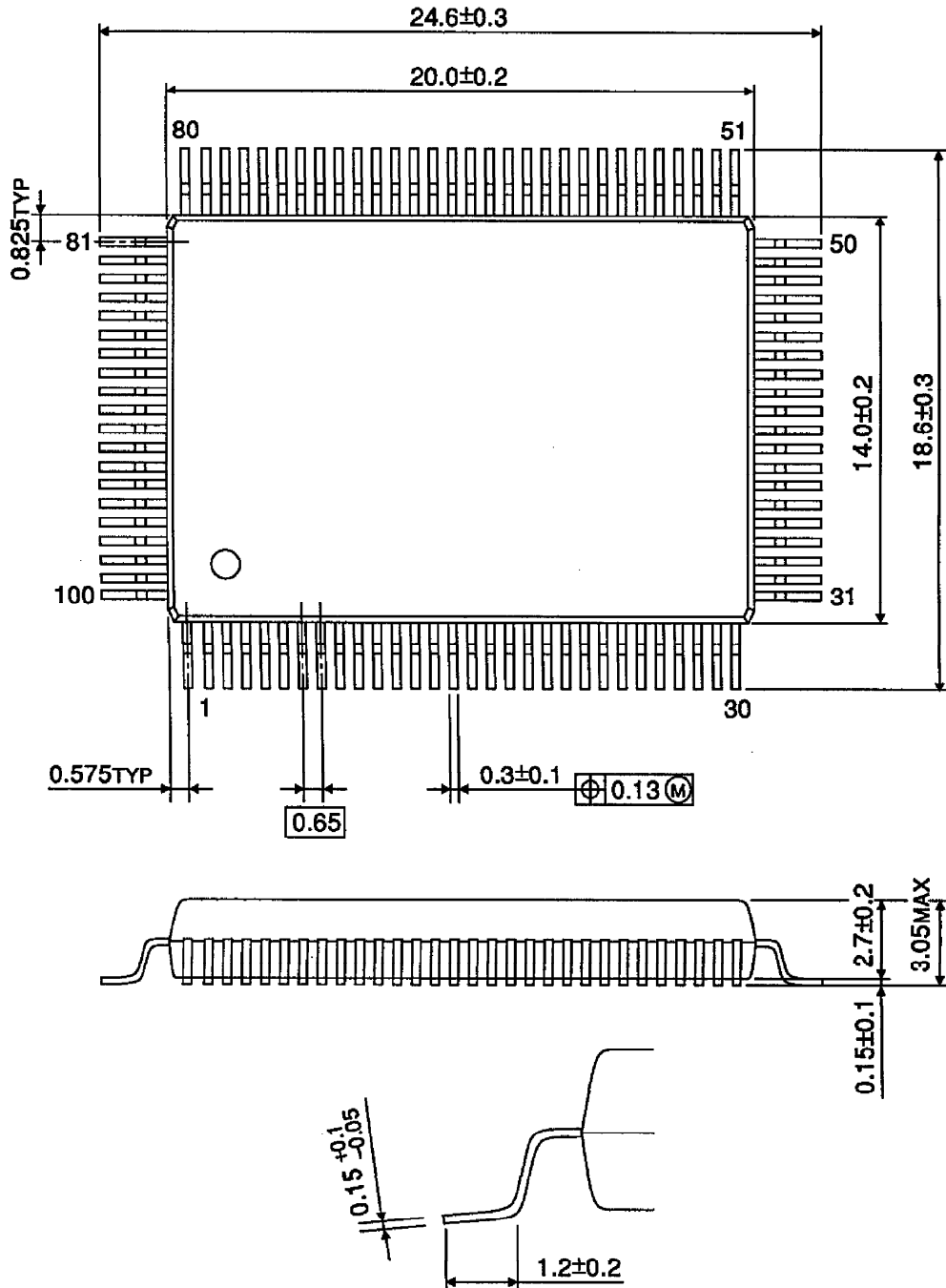
(Cautions)

- Quality of crystal oscillation wave form largely affect S/N ratio and noise distortion. Further, this is also true then system clock is input externally through the XI terminal.
- The wiring between the TC9296AF output and the TA2009F input must be made the shortest.
- The condenser between V_{DD} and GND shall be connected as close to the pin as possible.

OUTLINE DRAWING

QFP100-P-1420-0.65

Unit : mm



Weight : 1.6g (Typ.)

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