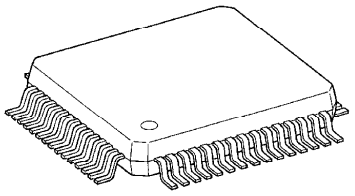
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9411F

CD GRAPHICS DECODER

TC9411F is a CMOS LSI which integrates on a single chip signal processing necessary for playing back CD graphics. TC9411F loads subcode data output from CD player processor TC9236AF or TC9284BF, de-interleaves, corrects errors, decides instructions, performs graphic processing, and outputs composite video signals.



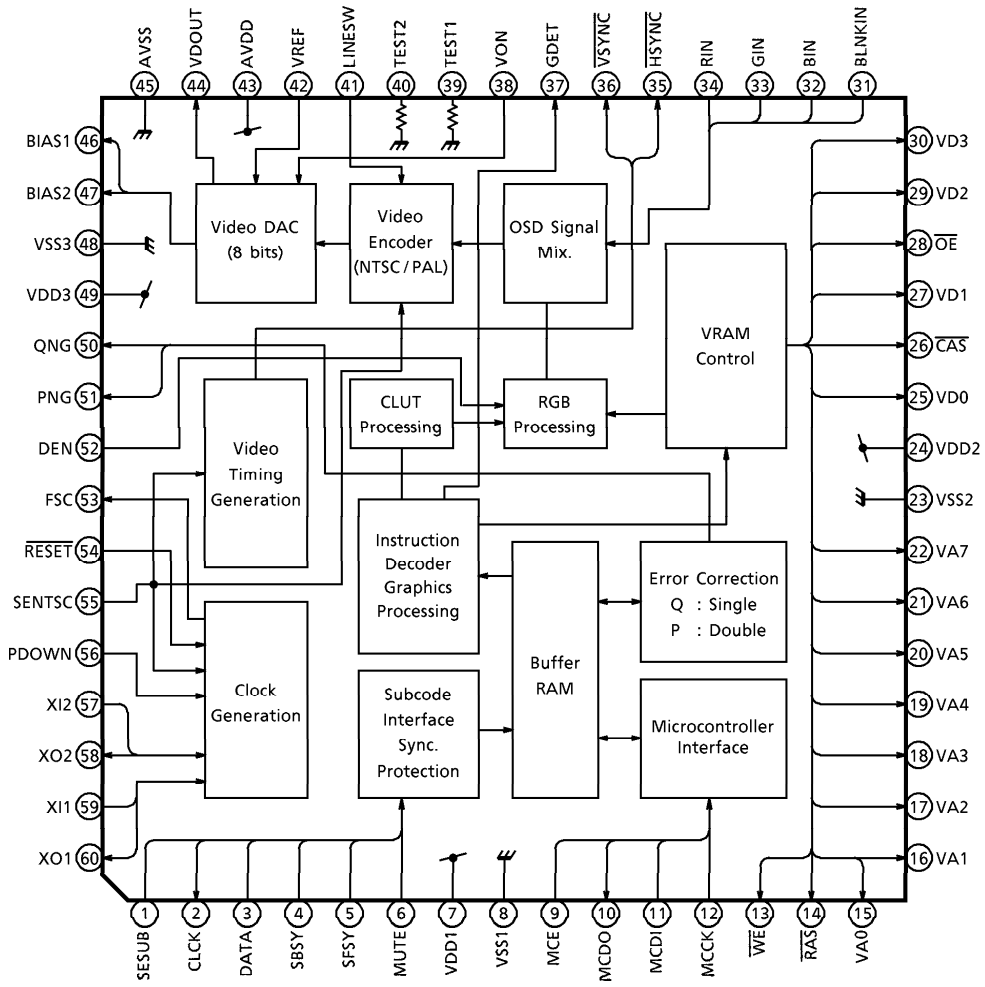
QFP60-P-1414-0.80D

Weight : 1.08g (Typ.)

FEATURES

- Configures a CD graphics decoder in two chips with external DRAM (64K words × 4 bits).
- Supports crystal oscillation function switchable between two standards, NTSC and PAL.
- Subcode interface function conforms to EIAJ. Performs, for the loaded subcode data, block sync protection, insertion, de-interleave, error detection and error correction.
- Performs instruction processing and graphic processing for TV graphics and line graphics to control display images.
- Using built-in 8 bits video signal DAC, outputs analog signals for composite video.
- Using video DAC stop mode, reduces power consumption during no graphics processing.
- Using serial-type microcontroller interface, fine adjustment of display position and setting of background color are possible.
- Basic operation possible without microcontroller.
- 60 pin flat package.

BLOCK DIAGRAM



PIN FUNCTIONS

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
1	SESUB	I	Subcode I/F select terminal. ("L" = EIAJ1, "H" = EIAJ2)	
2	CLCK	O	Subcode data transfer clock output terminal.	
3	DATA	I	Playback subcode data (R~W) input terminal.	
4	SBSY	I	Playback subcode block signal input terminal.	
5	SFSY	I	Playback subcode frame signal input terminal.	
6	MUTE	I	Playback subcode data invalid status input terminal.	
7	VDD1	—	Digital supply voltage terminal.	
8	VSS1	—	Digital ground terminal.	
9	MCE	I	Serial input (MCSI) and serial output (MCDO) operation enable switch terminal.	
10	MCDO	O	Serial data output terminal.	
11	MCDI	I	Serial data input terminal.	
12	MCCK	I	Serial input (MCSI) and serial output (MCDO) data transfer clock input terminal.	
13	$\overline{WE}$	O	External DRAM control terminal.	
14	$\overline{RAS}$	O	External DRAM control terminal.	
15	VA0	O	External DRAM address output terminal.	
16	VA1	O	External DRAM address output terminal.	
17	VA2	O	External DRAM address output terminal.	
18	VA3	O	External DRAM address output terminal.	
19	VA4	O	External DRAM address output terminal.	
20	VA5	O	External DRAM address output terminal.	
21	VA6	O	External DRAM address output terminal.	
22	VA7	O	External DRAM address output terminal.	
23	VSS2	—	Digital ground terminal.	
24	VDD2	—	Digital supply voltage terminal.	
25	VD0	I/O	External DRAM data I/O terminal.	
26	$\overline{CAS}$	O	External DRAM control terminal.	
27	VD1	I/O	External DRAM data I/O terminal.	
28	$\overline{OE}$	O	External DRAM control terminal.	
29	VD2	I/O	External DRAM data I/O terminal.	
30	VD3	I/O	External DRAM data I/O terminal.	
31	BLNKIN	I	OSD blanking control terminal. ("H" = OSD)	
32	BIN	I	OSD color B control terminal. ("H" = OSD)	
33	GIN	I	OSD color G control terminal. ("H" = OSD)	
34	RIN	I	OSD color R control terminal. ("H" = OSD)	
35	$\overline{HSYNC}$	O	Composite sync. signal output terminal.	
36	$\overline{VSYNC}$	O	Vertical sync. signal output terminal.	

PIN No.	SYMBOL	I / O	FUNCTIONAL DESCRIPTION	REMARKS
37	GDET	O	CDG data detect flag output terminal. ("L" = not detected, "H" = CDG detected)	
38	VON	I	DAC operation stop select terminal. ("L" = DAC stop, "H" = DAC output)	
39	TEST1	I	Test terminal. Normally, keep at "L" level or open.	With pull-down resistor
40	TEST2			
41	LINESW	I	Number of lines select terminal. NTSC mode : "L" = 262 lines, "H" = 263 lines PAL mode : "L" = 312 lines, "H" = 314 lines	
42	VREF	I	DAC output amplitude control voltage apply terminal. (amplitude = VDD – VREF)	
43	AVDD	—	Analog supply voltage terminal. (for DAC)	
44	VDOUT	O	Composite video output terminal. (8 bits DAC output)	
45	AVSS	—	Analog ground terminal. (for DAC)	
46	BIAS1	O	DAC bias output terminal. (Connect capacitor for rejection ripple.)	
47	BIAS2	O	DAC bias output terminal. (Connect capacitor for rejection ripple.)	
48	VSS3	—	Digital ground terminal.	
49	VDD3	—	Digital supply voltage terminal.	
50	QNG	O	Q row correction error status output terminal. ("L" = OK, "H" = error)	
51	PNG	O	P row correction error status output terminal. ("L" = OK, "H" = error)	
52	DEN	I	CDG display select terminal. ("L" = CD graphics, "H" = BGC)	
53	FSC	O	Color sub-carrier wave clock output terminal.	
54	$\overline{\text{RESET}}$	I	Reset terminal.	
55	SENTSC	I	NTSC mode / PAL mode select terminal. ("L" = PAL, "H" = NTSC)	
56	PDOWN	I	Standby mode select terminal. ("H" = clock stop)	
57	XI2	I	Crystal oscillator connecting terminal. (for PAL : 17.734476MHz)	With feedback resistor
58	XO2	O		
59	XI1	I	Crystal oscillator connecting terminal. (for NTSC : 14.31818MHz)	With feedback resistor
60	XO1	O		

OUTLINE DRAWING

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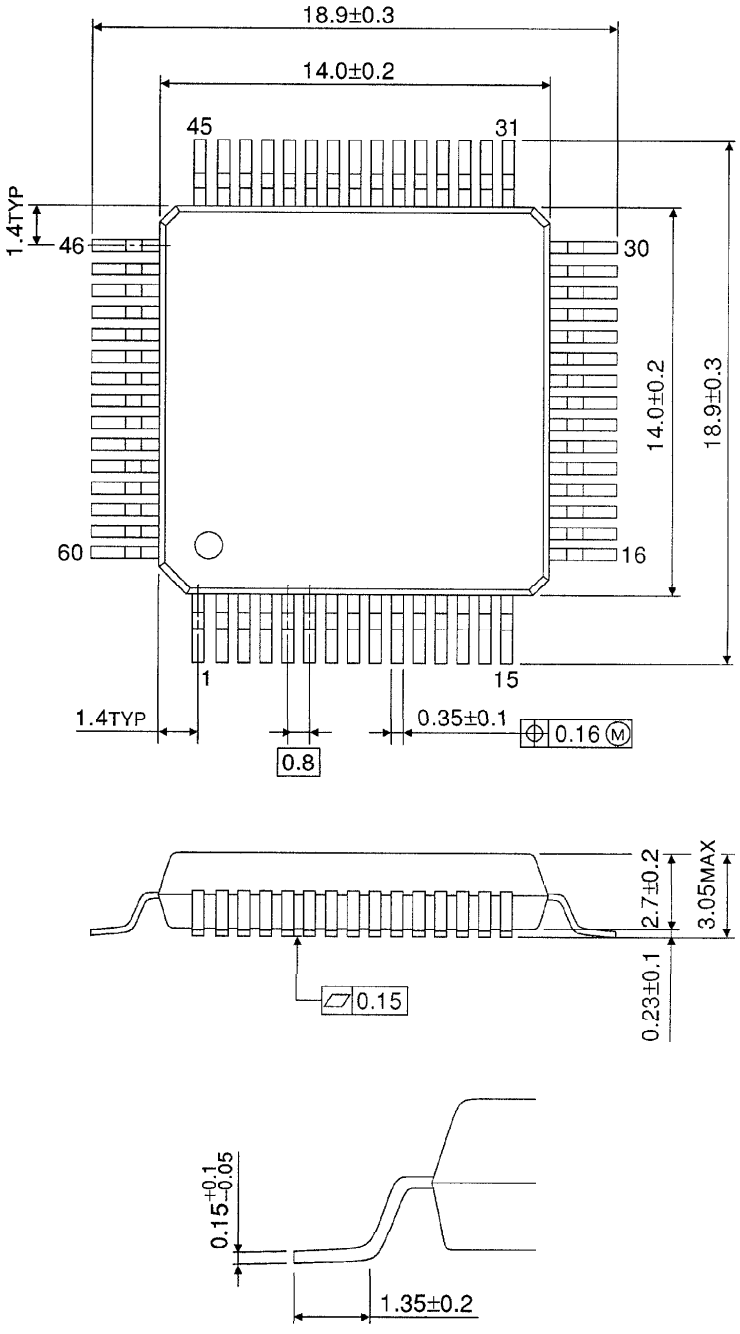
Unit : mm



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