TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

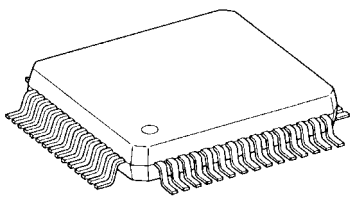
TC9444F

Single-Chip karaoke IC II

The TC9444F is a karaoke chip for such applications as equipment for CD/LD players, mini component stereo sets, radio-cassette players, and VTRs.

With its internal AD/DA converter system, the TC9444F can offer such karaoke functions as echo, vocal canceling, and key control on a single chip in addition to such digital signal processing (DSP) features as sound field control and bass/treble control.

Because the program and coefficients are stored on internal ROM, the IC can be controlled by simple settings.



QFP60-P-1414-0.80D

Weight: 1.08 g (typ.)

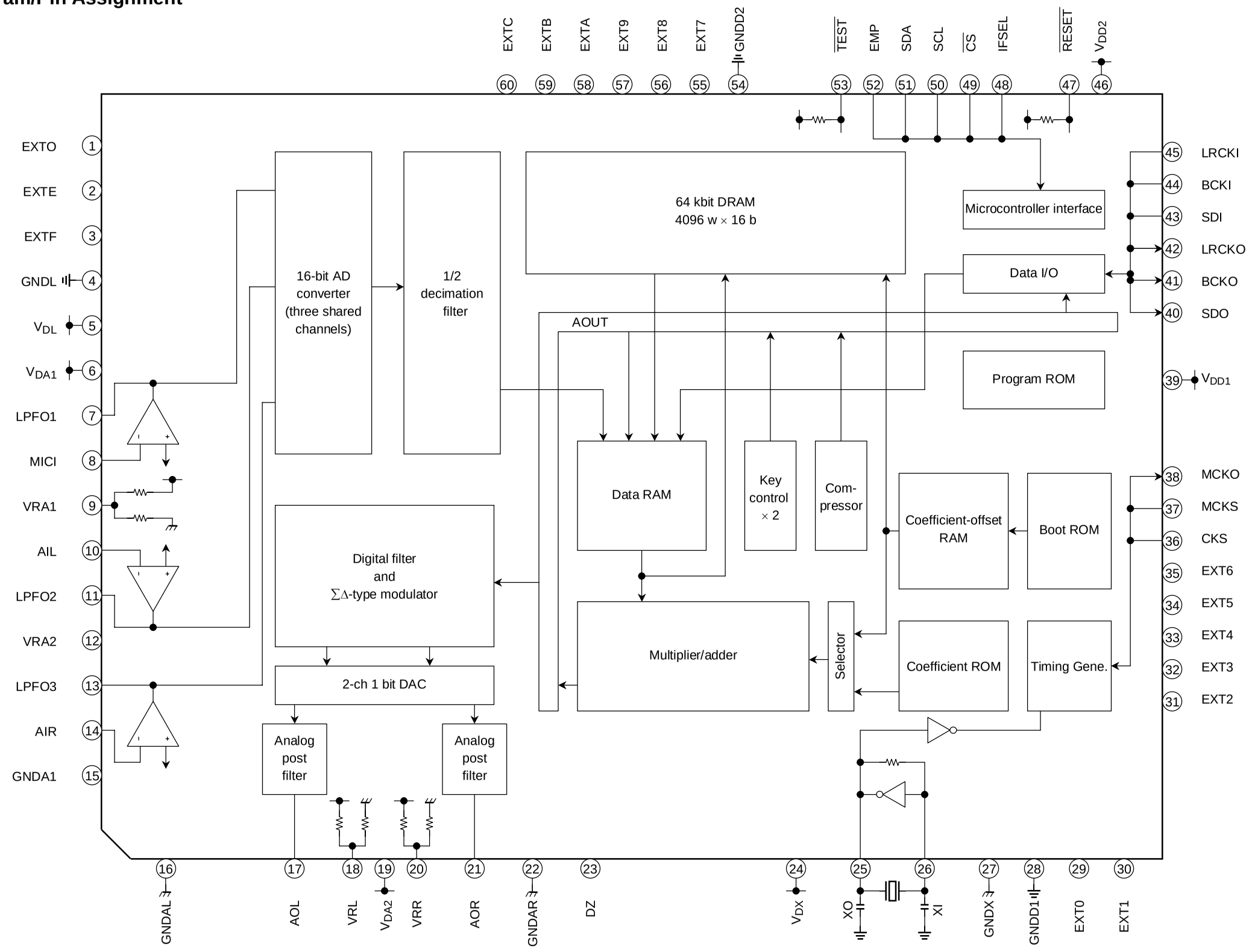
Features

- Incorporates an AD converter (three channels) with 2 times oversampling.
  THD: −65dB S/N ratio: 80dB (typ.)
  built-in pre-filter op-amp
- Incorporates a 1-bit ΣΔ-type DA converter (two channels).
  THD: −86dB S/N ratio: 93dB (typ.)
  built-in tertiary analog post filter
- Supports one port for digital input and one for digital output.
- Incorporates 64 Kbits of delay RAM
- Microcontroller interface: I^2C bus mode as well as Toshiba's original three-lead mode
- Built-in boot ROM initializes coefficients at reset or via a boot command.

[Compatible Software]

- Microphone echo: Variable delay time/level
- Vocal cancellation: Attenuates only vocals from standard source
- Vocal change: Vocals fade in/out depending on whether there is input from microphone
- Vocal key control: For chorus and duet functions
- Supports multi-sound sources: Various modes
- Pseudo stereo: Monaural sources enhanced by sense of spaciousness
- Key control: 14-step (max ±1 octave) stereo key control
- Compressor or bass boost: Compression ratio selectable in range 6 to 36dB.
  Compression effect (amount of boost) can be varied smoothly.
- Sound field control: Uses delay RAM to simulate such acoustic environments as churches, halls, sports stadiums, and discos.
- Equalizer: Characteristics switchable by coefficient or I/F bit settings
- 3D sound field: Offers 3-D sound.

Block Diagram/Pin Assignment



Pin Descriptions

Pin No.	Pin Name	I/O	Function	Remarks
1	EXTO	O	Extended output port D	
2	EXTE	O	Extended output port E	
3	EXTF	O	Extended output port F	
4	GNDL	—	DRAM ground	
5	V_{DL}	—	DRAM power supply	
6	V_{DA1}	—	ADC power supply	
7	LPFO1	O	Op-amp output for microphone input	
8	MICI	I	Op-amp input for microphone input	
9	VRA1	—	ADC reference voltage 1	
10	AIL	I	Op-amp input for line L-channel	
11	LPFO2	O	Op-amp output for line L-channel	
12	VRA2	—	ADC reference voltage 2	
13	LPFO3	O	Op-amp output for line R-channel	
14	AIR	I	Op-amp input for line R-channel	
15	GNDA1	—	ADC ground	
16	GNDAL	—	DAC L-channel ground	
17	AOL	O	DAC L-channel output	
18	VRL	—	DAC reference voltage	
19	V_{DA2}	—	DAC power supply	
20	VRR	—	DAC reference voltage	
21	AOR	O	DAC R-channel output	
22	GNDAR	—	DAC R-channel ground	
23	DZ	O	Digital zero input detection (“H” = zero detection)	
24	V_{DX}	—	Oscillator block power supply	
25	XO	O	Oscillator connection	
26	XI	I	Oscillator connection or clock input	
27	GNDX	—	Oscillator block ground	
28	GNDD1	—	Digital ground 1	
29	EXT0	O	Extended output port 0	
30	EXT1	O	Extended output port 1	
31	EXT2	O	Extended output port 2	
32	EXT3	O	Extended output port 3	
33	EXT4	O	Extended output port 4	
34	EXT5	O	Extended output port 5	
35	EXT6	O	Extended output port 6	
36	CKS	I	System clock selection (“H” = 512 fs, “L” = 384 fs)	Schmitt input
37	MCKS	I	MCKO output clock selection (“H” = 1/1, “L” = 1/2 divider)	Schmitt input
38	MCKO	O	System clock output	
39	V_{DD1}	—	Digital power supply 1	
40	SDO	O	Digital audio data output	
41	BCKO	O	Bit clock output	
42	LRCKO	O	Channel clock output	
43	SDI	I	Digital audio data input	Schmitt input

Pin No.	Pin Name	I/O	Function	Remarks
44	BCKI	I	Bit clock input	Schmitt input
45	LRCKI	I	Channel clock input	Schmitt input
46	V_{DD2}	—	Digital power supply 2	
47	$\overline{RESET}$	I (U)	Reset (“L” = reset)	With pull-up resistor Schmitt input
48	IFSEL	I	Microcontroller interface selection (“H” = three-lead mode, “L” = I^2C mode)	Schmitt input
49	$\overline{CS}$	I	Three-lead mode: Command send start signal I^2C: chip select	Schmitt input
50	SCL	I	Microcontroller interface serial clock	Schmitt input
51	SDA	O	Microcontroller interface serial data	Schmitt input
52	EMP	—	De-emphasis setting (“H” = ON)	Schmitt input
53	$\overline{TEST}$	I (U)	Test mode setting (“H” = fixed)	With pull-up resistor Schmitt input
54	GNDD2	I	Digital ground 2	
55	EXT7	O	Extended output port 7	
56	EXT8	O	Extended output port 8	
57	EXT9	O	Extended output port 9	
58	EXTA	O	Extended output port A	
59	EXTB	O	Extended output port B	
60	EXTC	O	Extended output port C	

Block Operations

1. Operating Clocks

The master clock can be selected between 512 or 384 fs using the CKS pin. The master clock uses oscillator or external clock input, through the XI pin.

Regardless of a master clock, the number of digital signal processing steps are predetermined. However, the DA converter's operating clock varies according to the master clock mode.

The MCKS pin sets the MCKO output, selecting 1/1 or 1/2 divider of the XI pin.

Table 1.1 Operating Clock Selection and DA Converter Oversampling Rate

CKS Pin	MCKS Pin	XI Input	MCKO Output	DAC Oversampling Rate
L	L	384 fs	192 fs	192 fs
	H		384 fs	
H	L	512 fs	256 fs	256 fs
	H		512 fs	

2. Digital Audio Data Input/Output

2.1 Sync Mode

The data input/output bit clock and internal sync (master) mode or external sync (slave) mode are set using microcontroller interface bits SYNM1 and SYNM2. Initialization by reset sets master mode.

Table 2.1 Sync Mode and Input/Output Bit Clock Settings

SYNM2	SYNM1	SYNC Mode	BCKI	BCKO
0	0	Master	(Note 1)	64 fs (Note 2)
0	1	Slave	32 fs	BCKI
1	0	Slave	48 fs	BCKI
1	1	Slave	64 fs	BCKI

Note 1: See Table 2.2.

Note 2: XI input divider clock

2.2 Data Input Formats

Table 2.2 and Figure 2.1 show the data input formats. Microcontroller interface bits IBIT1, IBIT2, and IBIT3 select the format.

In master mode, the BCKI clock rate varies through the range shown in 2.2.

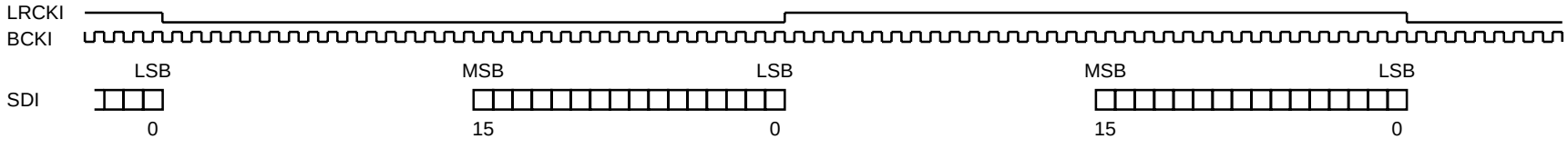
In slave mode, the BCKI input clock is directly output through the IC internal buffer as the data output bit clock (BCKO). Therefore, when using the digital data output, input the clock shown in Table 2.2.

The IIS-compatible format can accept up to 24 bits of data. When inputting data shorter than 24 bits, fix the lower bits to 0.

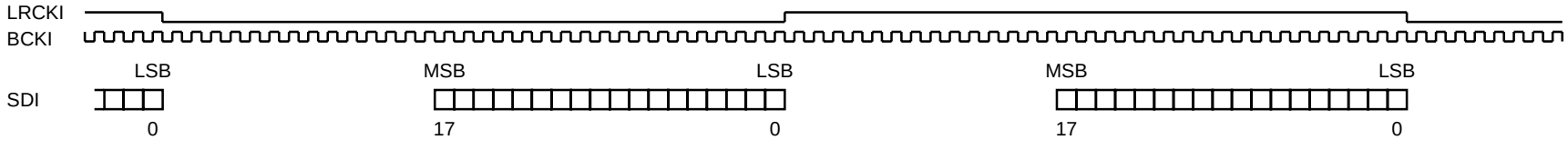
Table 2.2 Data Input Formats

SYNM2	SYNM1	IBIT3	IBIT2	IBIT1		Format	BCKI
0	0	0	0	0	Master mode	MSB first, Right-Justified mode, 16-bit data	32 fs to 128 fs
0	0	0	0	1		MSB first, Right-Justified mode, 18-bit data	36 fs to 128 fs
0	0	0	1	0		MSB first, Right-Justified mode, 20-bit data	40 fs to 128 fs
0	0	0	1	1		MSB first, Right-Justified mode, 24-bit data	48 fs to 128 fs
0	0	1	0	0		IIS-compatible, 24 bits	64 fs
0	1	0	0	0	Slave mode	MSB first, Right-Justified mode, 16-bit data	32 fs
0	1	0	0	1		Prohibited	32 fs
0	1	0	1	0		Prohibited	32 fs
0	1	0	1	1		Prohibited	32 fs
0	1	1	0	0		IIS-compatible, 16 bits	32 fs
1	0	0	0	0		MSB first, Right-Justified mode, 16-bit data	48 fs
1	0	0	0	1		MSB first, Right-Justified mode, 18-bit data	48 fs
1	0	0	1	0		MSB first, Right-Justified mode, 20-bit data	48 fs
1	0	0	1	1		MSB first, Right-Justified mode, 24-bit data	48 fs
1	0	1	0	0		IIS-compatible, 24 bits	48 fs
1	1	0	0	0		MSB first, Right-Justified mode, 16-bit data	64 fs
1	1	0	0	1		MSB first, Right-Justified mode, 18-bit data	64 fs
1	1	0	1	0		MSB first, Right-Justified mode, 20-bit data	64 fs
1	1	0	1	1		MSB first, Right-Justified mode, 24-bit data	64 fs
1	1	1	0	0		IIS-compatible, 24 bits	64 fs

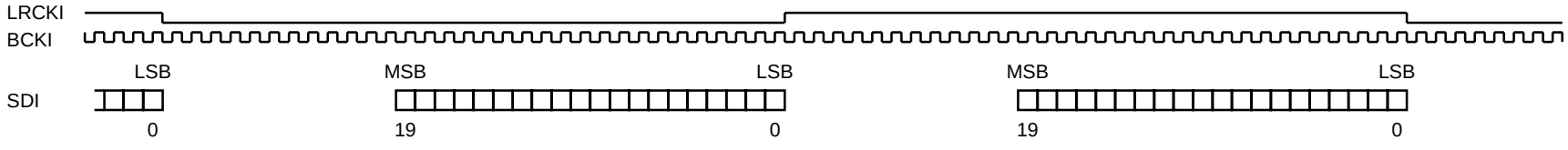
a) (IBIT3, IBIT2, IBIT1) = (0, 0, 0): MSB first, Right-Justified mode, 16-bit data



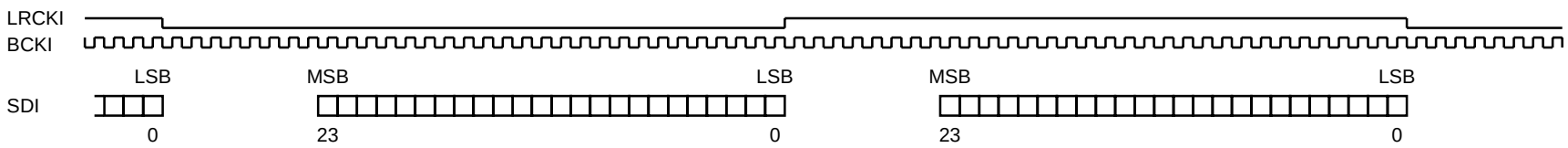
b) (IBIT3, IBIT2, IBIT1) = (0, 0, 1): MSB first, Right-Justified mode, 18-bit data



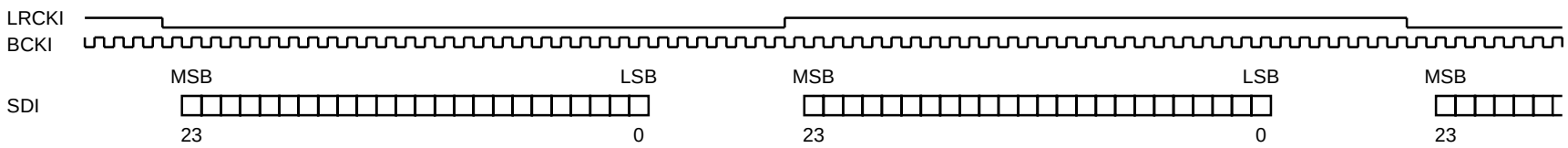
c) (IBIT3, IBIT2, IBIT1) = (0, 1, 0): MSB first, Right-Justified mode, 20-bit data



d) (IBIT3, IBIT2, IBIT1) = (0, 1, 1): MSB first, Right-Justified mode, 24-bit data



e) (IBIT3, IBIT2, IBIT1) = (1, 0, 0): IIS-compatible, 24 bits max



Note 3: In either mode, sections where “SDI” is omitted are don’t care (no internal data loading).

Figure 2.1 Data Input Formats (BCK = 64 fs)

The microcontroller interface RLS bit controls the polarity of the input/output channel clock (LRCKI, LRCKO).

Table 2.3 Channel Clock Polarity

RLS	Operation
0	L-channel data input/output when LRCKI and LRCKO = “H”
1	L-channel data input/output when LRCKI and LRCKO = “L”

2.3 Zero Data Detection Function Common to L/R

The TC9444F incorporates a function to output a zero detection flag from the DZ pin when input data contain a string of digital zeros. This is used to forcibly mute the analog output.

Table 2.4 shows the time that elapses until data are detected as zero data. If digital zeros continue to be output during this period, a zero detection flag is set.

Moreover, setting the DZINH bit in the microcontroller interface mode command to "H" halts zero detection, fixing the DZ pin to "L" and disabling the zero detection function (see the microcontroller interface section below).

Table 2.4 Digital Zero Data Detection Time

fs	32 kHz	44.1 kHz	48 kHz
Detection Time	1024 ms	743 ms	683 ms

A reset sets the DZ signal to "H".

2.4 Data Output Formats

Table 2.5 and Figure 2.2 show the data output formats. Microcontroller interface bits OBIT1 and OBIT2 select the format.

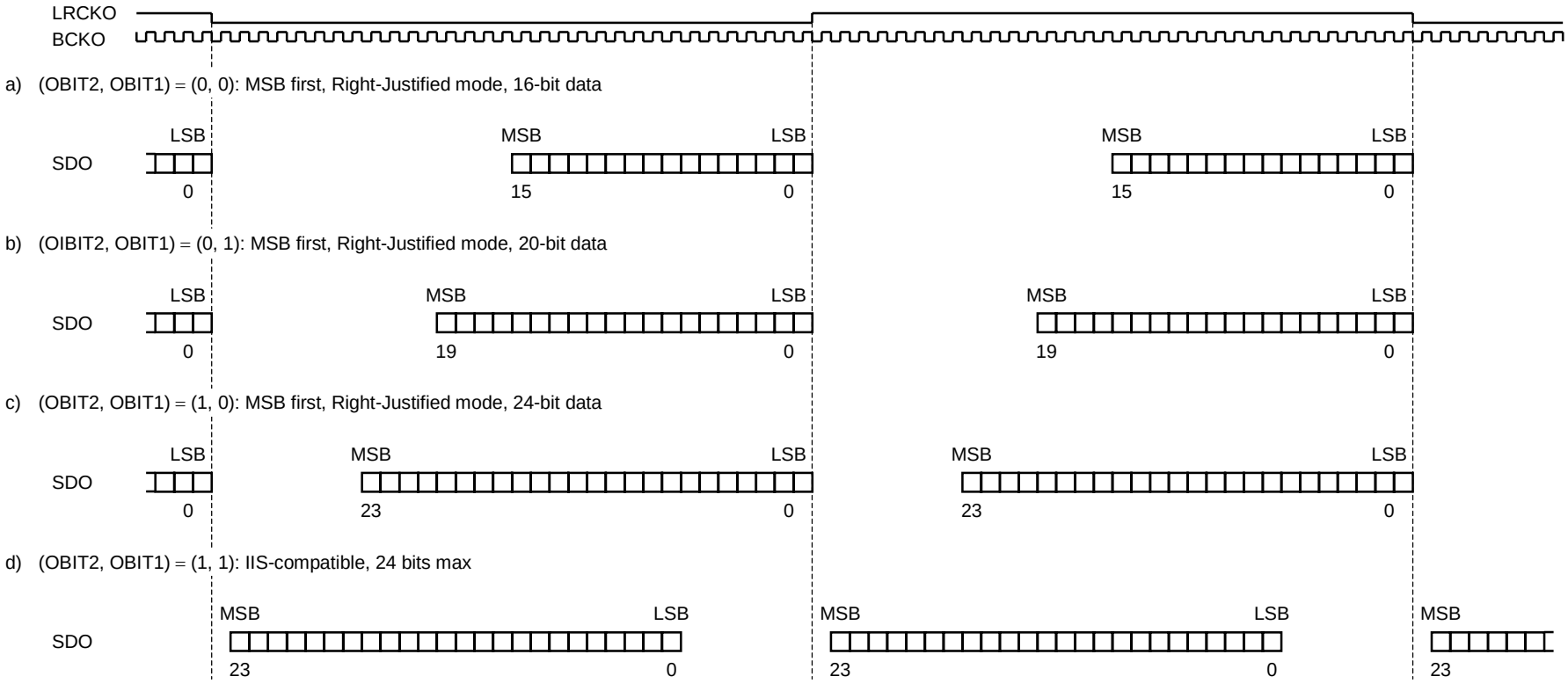
In master mode, the BCKI clock rate varies through the range shown in Table 2.2. Note, however, that BCKO is fixed to 64 fs.

In slave mode, the BCKI input clock is directly output as the data output bit clock (BCKO) through the IC internal buffer (see section 2.2).

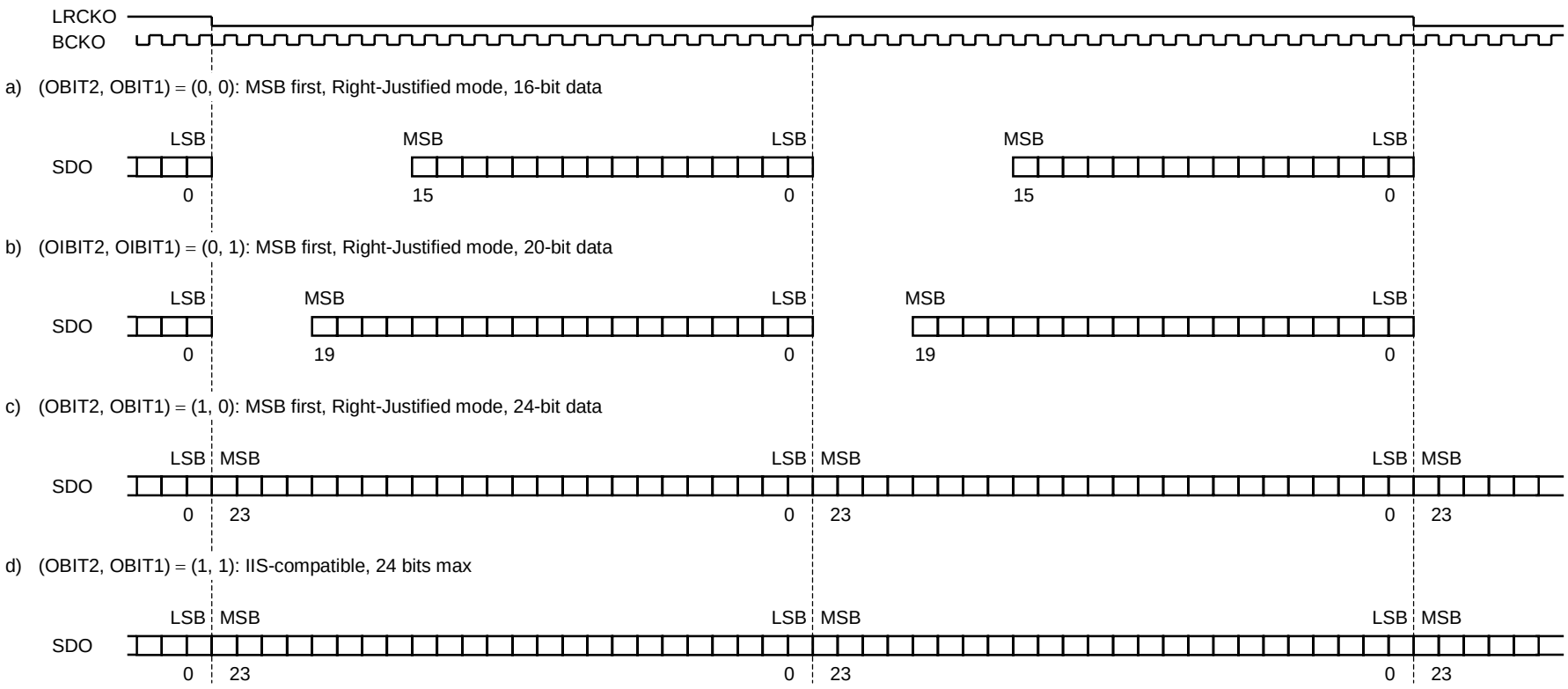
Table 2.5 Data Output Formats

SYNM2	SYNM1	IBIT2	IBIT1		Format	BCKI
0	0	0	0	Master mode	MSB first, Right-Justified mode, 16-bit data	64 fs
0	0	0	1		MSB first, Right-Justified mode, 20-bit data	64 fs
0	0	1	0		MSB first, Right-Justified mode, 24-bit data	64 fs
0	0	1	1		IIS-compatible, 24 bits	64 fs
0	1	0	0	Slave mode	MSB first, Right-Justified mode, 16-bit data	32 fs (= BCKI)
0	1	0	1		Prohibited	32 fs (= BCKI)
0	1	1	0		Prohibited	32 fs (= BCKI)
0	1	1	1		IIS-compatible, 16 bits	32 fs (= BCKI)
1	0	0	0		MSB first, Right-Justified mode, 16-bit data	48 fs (= BCKI)
1	0	0	1		MSB first, Right-Justified mode, 20-bit data	48 fs (= BCKI)
1	0	1	0		MSB first, Right-Justified mode, 24-bit data	48 fs (= BCKI)
1	0	1	1		IIS-compatible, 24 bits	48 fs (= BCKI)
1	1	0	0		MSB first, Right-Justified mode, 16-bit data	64 fs (= BCKI)
1	1	0	1		MSB first, Right-Justified mode, 20-bit data	64 fs (= BCKI)
1	1	1	0		MSB first, Right-Justified mode, 24-bit data	64 fs (= BCKI)
1	1	1	1		IIS-compatible, 24 bits	64 fs (= BCKI)

(SYNM2, 1) = (0, 0) or (1, 1) BCKO = 64 fs



(SYNM2, 1) = (1, 0) BCKO = 48 fs



(SYNM2, 1) = (0, 1) BCKO = 32 fs

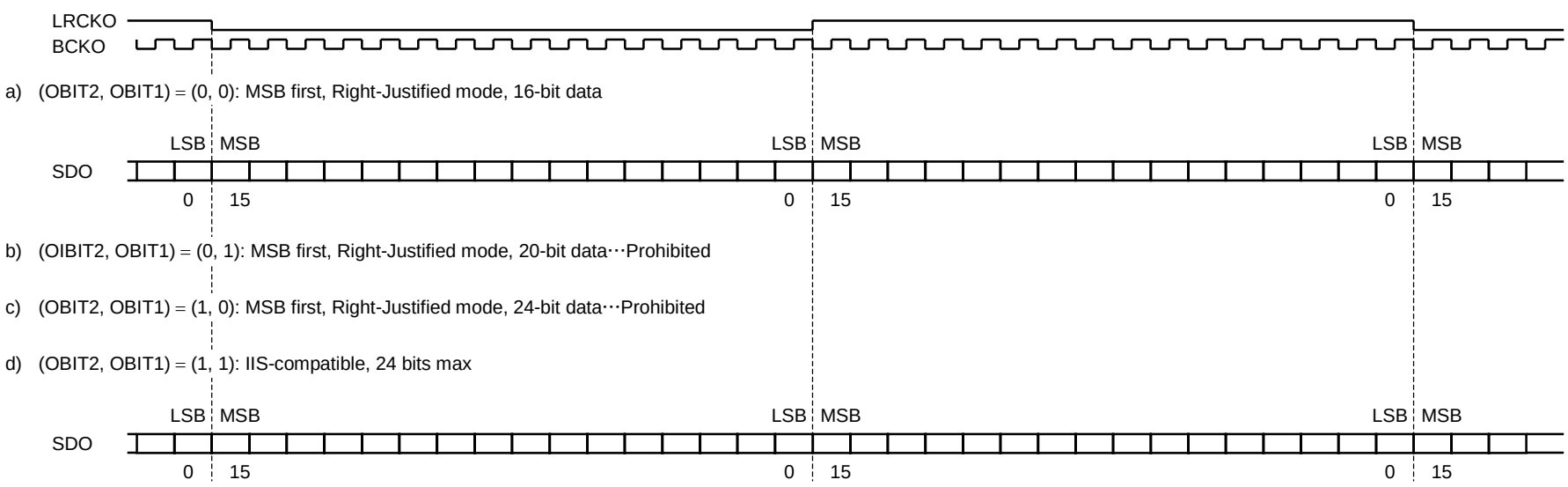


Figure 2.2 Data Output Formats

3. Microcontroller Interface

Consisting of commands and data, the microcontroller interface block is designed as a simple and easy-to-use interface. This interface has two modes: I^2C bus mode and three-lead mode. I^2C bus mode can be switched by a DC setting via a pin.

3.1 Commands

One-byte (8-bit) commands are used to perform a range of settings. Some commands are followed by one to three bytes of data.

An initial reset sets the microcontroller interface block to master mode. Boot ROM data can be used to output a sound at reset (analog through mode).

After power-on, reset at least once by setting the $\overline{\text{RESET}}$ pin to low level.

Table 3.1 List of Commands

Command	CH	CL	Data	Setting Contents
BOOT	0	0	—	Initializes coefficient RAM.
MUTE	1	0 to 3	—	Turns soft mute and RAMCLR on/off.
KEYCON	2	0 to F	—	Key control; amount of key shift
VC	3	0 to F	—	16-page bank vocal cancel/change, multi-sound source
BKSA	4	0 to 3	—	4-page bank function reserve
BKSB	5	0, 1	—	2-page bank function reserve
EMP	6	0 to F	—	De-emphasis
DECI	7	0 to 3	—	Delay RAM decimation rate
ATIME	8	0 to 3	—	Level detection attack time
RTIME	9	0 to 6	—	Level detection release time
COMP	A	0 to F	—	Compressor function
ATTA	B	0	2-byte	Digital attenuator level A
ATTB	B	1	2-byte	Digital attenuator level B
KEYCON2	B	2	2-byte	Controls an independent key or sets vibrato.
EXTO	B	3	2-byte	Extended output port data
CRAM	C	0, 1	3-byte	Writes coefficient RAM.
MODE	D	0 to 3	1-byte	Sets IC operating mode.

Note 4: The functions of some commands vary according to the internal program.

Also, some programs contain commands that need not be set.

Refer to the separate software datasheet.

The commands are described below. The values in the table marked by an asterisk are the initial values at a reset.

Setting $\overline{\text{RESET}}$ to "L" also mutes the DA converter output (op-amp feed-back causes the DA converter to output VREF). Accordingly, to completely mute the analog output during operation, digitally mute the output using the MUTE command, then set $\overline{\text{RESET}}$ to "L".

3.2 BOOT Command

One-byte command to initialize coefficient RAM.

Initializes coefficient RAM values to the internal BOOT ROM values, retaining the other command interface settings.

After the BOOT command is received, initialization completes in a 1-fs cycle. Boot release is not required.

When reset is made by setting the $\overline{\text{RESET}}$ pin to "L", boot is still executed.

3.3 MUTE Command

One-byte command to clear data RAM and delay RAM, and to execute a soft mute using the digital attenuator.

Table 3.2 MUTE Command

CH	CL			
	3	2	1	0
1	0	0	RAMCLR	MUTE

Note 5: At a reset, the initial value is CL = 0H.

MUTE: MUTE = "H" sets soft mute.

RAMCLR: RAMCLR = "H" clears data RAM and delay RAM.

At a soft mute, the time constant is determined by the operation sampling frequency and the time constant selection bit set by the ATTA command. After the soft mute is released, the digital attenuator is restored to the set level.

In data RAM, sequentially writing all-zero data (fixing the input data to 000000H) while RAMCLR = "H" clears data RAM. Therefore, the number of fs cycles required to completely clear data RAM depends on the program. Normally, several cycles are required.

For a program which is written to in one place only, a 128-word update takes no more than 3 ms.

In delay RAM, after RAMCLR = H, 0000H is sequentially written to delay RAM at subsequent write operations (INIT operation).

When using delay RAM to significantly change the effect of the SFC processing, to clear the data in RAM, take the following steps. First set the MUTE bit. Then, after waiting only the length of the digital attenuator time constant, set RAMCLR to "H" to clear the data in RAM. Then set the RAMCLR and MUTE bits to "L". This will enable you to change the signal processing content without any switching noise.

3.4 KEYCON Command

One-byte command to control the amount of key shift. The CL value indicates the amount of key shift.

The difference between the 20H command and the 28H command is the point at which key control processing completely stops. Using the 20H command to turn key control off disables the use of internal delay RAM in the key control processing, thus allowing delay RAM to be allocated to other processing.

The amount of key shift set by the KEYCON command applies to both L and R stereo key control and to monaural key control. The key shift is set in semitone steps.

As delay RAM is used in key control processing, when switching the key shift setting between 0 and a value other than 0, the signal is intermittent. The soft mute automatically comes on to avoid switching noise at this time. After the command is issued, the following steps are performed automatically.

Mute → Internal settings switched → Mute released

This series of processing operations takes around 46 ms to execute.

Table 3.3 Setting Key Shift Amount

CH	CL	Setting Content
2	0	Key shift 0 (key control off)
2	1	+1200 cent
2	2	+600 cent
2	3	+500 cent
2	4	+400 cent
2	5	+300 cent
2	6	+200 cent
2	7	+100 cent
*2	8	Key shift 0
2	9	−100 cent
2	A	−200 cent
2	B	−300 cent
2	C	−400 cent
2	D	−500 cent
2	E	−600 cent
2	F	−1200 cent

3.5 VC Command

One-byte command to set through, vocal cancel, and vocal change for each input source.
Refer to the separate software datasheet.

3.6 BKSA Command

One-byte command to set four-page bank switching.

3.7 BKSB Command

One-byte command to set two-page bank switching.

3.8 EMPH Command

This command selects an internal de-emphasis digital filter.

The filter is either a digital filter selected, via software, by switching a DSP coefficient bank, or an internal DA converter digital filter selected via hardware.

The filter is set through the microcontroller interface. The filter is on only when the EMP pin goes high. This command sets the filter on/off directly from the CD processor EMP flag without passing through the microcontroller.

As well as a de-emphasis filter, the DSP block filter can also be used as a high-pass filter for canceling DC offset. (the CROM data determines the filter's function.)

Table 3.4 EMPH Command

CH	CL			
	3	2	1	0
6	ESB2	ESB1	ESA2	ESA1

Note 6: At a reset, the initial value is CL = 5H.

Table 3.5 Settings with EMPH Command

CH	CL				Setting Block	Filter Characteristics
	ESB2	ESB1	ESA2	ESA1		
6	—	—	0	0	DSP block	Bank 0 (fs = 44.1 kHz)
*6	—	—	0	1	DSP block	Bank 1 (off)
6	—	—	1	0	DSP block	Bank 2 (fs = 48 kHz)
6	—	—	1	1	DSP block	Bank 3 (fs = 32 kHz)
6	0	0	—	—	Output DAC block	fs = 44.1 kHz
*6	0	1	—	—	Output DAC block	Off (through)
6	1	0	—	—	Output DAC block	fs = 48 kHz
6	1	1	—	—	Output DAC block	fs = 32 kHz

3.9 DECI Command

One-byte command to select the decimation filter for delay processing in delay RAM.

At a reset, the initial value is 1/3 decimation (CL = 2).

This command determines only the decimation filter band. The decimation rate in delay RAM is determined by the OFRAM command value.

Table 3.6 DECI Command

CH	CL	Setting Content
7	0	1/1 decimation
7	1	1/2 decimation
*7	2	1/3 decimation
7	3	1/4 decimation

3.10 ATIME Command

One-byte command to set the compressor block attack time.

Table 3.7 ATIME Command

CH	CL	ATK1	ATK0	Attack Time [ms]			
				CB2, 1 = 0, 0	CB2, 1 = 0, 1	CB2, 1 = 1, 0	CB2, 1 = 1, 1
8	0	L	L	4	3	2	1
8	1	L	H	8	6	4	2
*8	2	H	L	16	12	8	4
8	3	H	H	32	24	16	8

3.11 RTIME Command

One-byte command to set the compressor block release time.

Table 3.8 RTIME Command [s]

CH	CL	REL1	REL1	REL0	Release Time			
					CB2, 1 = 0, 0	CB2, 1 = 0, 1	CB2, 1 = 1, 0	CB2, 1 = 1, 1
9	0	L	L	L	1.1	0.5	0.3	0.1
*9	1	L	L	H	1.6	1.0	0.7	0.3
9	2	H	L	L	2.6	2.0	1.3	0.6
9	3	L	H	H	4.6	4.1	2.6	1.1
9	4	H	L	L	8.7	8.2	5.2	2.2
9	5	H	L	H	16.9	16.3	10.4	4.5
9	6	H	H	L	33.3	32.6	20.8	9.0

3.12 COMP Command

One-byte command to select the compressor function.

Table 3.9 COMP Command

CH	CL			
	3	2	1	0
A	VCHG	CBS	CB2	CB1

Note 7: At a reset, the initial value is CL = 8H.

VCHG: VCHG = “H” selects (turns on) the vocal change function.

CBS: Selects the compression ratio. CBS = “L” selects a ratio of 24dB; CBS = “H” selects 36dB (refer to the table)

CB2, 1: Used for precise selection of the compression ratio.

Table 3.10 Compression Ratio Settings

CBS	CB2	CB1	Compression Ratio
0	0	0	24dB
0	0	1	18dB
0	1	0	12dB
0	1	1	6dB
1	0	0	36dB
1	0	1	27dB
1	1	0	18dB
1	1	1	9dB

Noise can result when CB2, 1 are used to switch the compression ratio.
To switch the ratio without clunking, refer to the software datasheet.

3.13 ATTA Command

Command to set the digital attenuator level by adding two-byte data.

When the lower 14 bits of the data are set to 2000H, the attenuator level is 0dB.

The upper two bits are the attenuator time constant selection bits. These bits select the soft mute time constants.

When switching using the MUTE or KEYCON command, the value set by ATTA is also valid for the automatic mute function.

Table 3.11 ATTA Command

CH	CL	D1								D0		
B	0	DSA2	DSA1	ALA13	ALA12	ALA11	ALA10	ALA09	ALA08	ALA07	~	ALA00

Note 8: At a reset, the initial values are DSA = 0H (23 ms) and ALA [13:00] = 2000H (0dB).

The following formula determines the data ALA [13:00] depending on the level (LEVEL [dB]) to be set.

ALA [13:00] = 2000H*10^ (LEVEL/20).

Table 3.12 Attenuator Setting Level

ALA [13:00]	Output Level
3FFFH	+6.020dB
……	……
3000H	+3.523dB
……	……
2000H	−0.000dB
1FFFH	−0.001dB
1FFEH	−0.002dB
……	……
16A7H	−3.000dB
……	……
1000H	−6.021dB
……	……
0002H	−72.247dB
0001H	−78.268dB
0000H	−∞dB

Table 3.13 Attenuator Time Constants

DSA2	DSA1	Time Constant		
		fs = 32 kHz	fs = 44.1 kHz	fs = 48 kHz
L	L	32 ms	23 ms	21 ms
L	H	128 ms	92 ms	86 ms
H	L	256 ms	186 ms	171 ms
H	H	512 ms	372 ms	341 ms

Time required for change from 0dB to −∞dB.

3.14 ATTB Command

Command to set the cross fade level for the vibrato function on/off by adding two-byte data.

When the lower 14 bits of the data are set to 2000H, the attenuator level is 0dB. The upper two bits are the attenuator time constant selection bits. These bits select the soft mute time constants.

Table 3.14 ATTB Command

CH	CL	D1								D0		
B	1	DSB2	DSB1	ALB13	ALB12	ALB11	ALB10	ALB09	ALB08	ALB07	~	ALB00

Note 9: At a reset, the initial values are DSB = 0H (23 ms) and ALB [13:00] = 2000H (0dB).

The values are set in the same way as the settings for the ATTA command.

3.15 KEYCON2 Command

Command to set the independent key control right channel or to set the vibrato function by adding two-byte data.

Because the initial reset sets ENA to “L”, L/R common key control by KEYCON is enabled at an initial reset.

Table 3.15 KEYCON2 Command

CH	CL	D1								D0		
B	2	0	0	ENA	VIB	K2R11	K2R10	K2R09	K2R08	K2R07	~	K2R00

Note 10: At a reset, the initial values are D1 = D2 = 0H.

ENA: Set to “H” when using independent key control or vibrato.

VIB: Set to “H” when using the vibrato function.

K2R [11:00]: When KEYCON2 is used for independent key control, these bits set the key control rate. When KEYCON2 is used to select the vibrato function, these bits set the step value that determines the vibrato cycle.

Table 3.16 Key Control Set by KEYCON2 (ENA = “H”, VIB = “L”)

Amount of Key Shift	K2R [11:00]	D1	D0
+1200 cent	400	24	00
+600 cent	1A8	21	A8
+500 cent	157	21	57
+400 cent	10A	21	0A
+300 cent	0C2	20	C2
+200 cent	07D	20	7D
+100 cent	03D	20	3D
.....			
+50 cent	01E	20	1E
+40 cent	018	20	18
+30 cent	012	20	12
+20 cent	00C	20	0C
+10 cent	006	20	06
−10 cent	FFA	2F	FA
−20 cent	FF4	2F	F4
−30 cent	FEE	2F	EE
−40 cent	FE9	2F	E9
−50 cent	FE3	2F	E3
.....			
−100 cent	EC7	2F	C7
−200 cent	F90	2F	90
−300 cent	F50	2F	50
−400 cent	F2D	2F	2D
−500 cent	EFF	2E	FF
−600 cent	ED4	2E	D4
−1200 cent	E00	2E	00

K2R [11:00] = (2^ (N/1200 [cent]) − 1.0) *400H

Table 3.17 Vibrato Cycle Set by KEYCON2 (ENA = “H”, VIB = “H”)

Cycle [Hz]	K2R [11:00]	D1	D0
.....			
2	05D	30	5D
.....			
4	0BA	30	BA
.....			
8	175	31	75
.....			

K2R [11:00] = N/22500 [Hz] *100000H

3.16 EXTO Command

Command to set the output data of the extended output port by adding two-byte data.
The two-byte data are output in parallel directly from the EXT0 to EXTF pins.
The command is used to control the LEDs which display the key control on/off status and the amount of key shift.

Table 3.18 EXTO Command

CH	CL	D1								D0		
B	3	EXTF	EXTE	EXTD	EXTC	EXTB	EXTA	EXT9	EXT8	EXT7	~	EXT0

Note 11: At a reset, the initial values are D1 = D0 = 0H.

3.17 CRAM Command

Command to write coefficient RAM data by adding three-byte data.
As in the following table, the value of the MSB of the address is assigned to the LSB of the CL bits.

Table 3.19 CRAM Command

CH	CL				D2								D1
C	0	0	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	AD17	AD16	

D2	D1			D0		
	DT15	~	DT08	DT07	~	DT00

Note 12: A reset or a boot command sets the coefficient RAM value to its initial value.

The R/W offset addresses of coefficient RAM and delay RAM are written as 18 bits of data. An address consists of three memory allocation bits, three decimation rate bits, and 12 offset address bits. Because the content of these settings depends on the internal program, refer to the separate software datasheet.

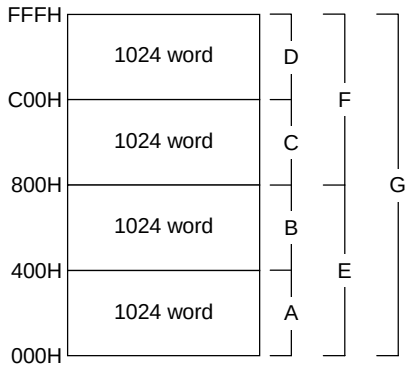
Table 3.20 OFRAM Command

CH	CL				D2								D1
C	0	0	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	MAL2	MAL1	

D2	D1							D0		
	MAL0	DECI2	DECI1	DECI0	DTI1	~	DT08	DT07	~	DT00

Note 13: A reset or a boot command sets the offset RAM value to its initial value.

In addition Delay RAM is properly used by MAL [2:0] as RAM of 1024, 2048, and 4096 word, as shown in the following figure.



Note 14: Since C block is assigned to Keycontrol R-ch, and D block is assingned to Keycontrol L-ch, it is neseccary to be set to KEY = 0H when using it here.

Figure 3.1 Block Division of Delay RAM

Table 3.21 Block Assignment and Address Range of Delay RAM

MAL2	MAL1	MAL0	Block	Address Range
0	0	0	A	3FFh to 000h
0	0	1	B	7FFh to 400h
0	1	0	C	BFFh to 800h
0	1	1	D	FFFh to C00h
1	0	0	E	7FFh to 000h
1	0	1	F	FFFh to C00h
1	1	—	G	FFFh to 000h

Table 3.22 Setting of Decimation Ratio

DECI2	DECI1	DECI0	Decimation Ratio
0	0	0	1/1
0	0	1	1/2
0	1	0	1/3
0	1	1	1/4

The same or overlapping block cannot be accessed by different decimation ratio.

Moreover, decimation ratio set up here and decimation ratio set up by DECI command need to be fundamentally made in agreement.

DECI bit set up with an offset address determines decimation ratio of memory access, and a setup to DECI command determines the band of a decimation filter.

3.18 MODE Command

Command to set the IC operating mode by adding one-byte data.
This command bundles parameters so that they need be set once only at power-on.
The CL bits are also used to make settings.

Table 3.23 MODE Command

CH	CL				D0							
	3	2	1	0	7	6	5	4	3	2	1	0
D	0	SYMM2	SYMM1	RLS	OBIT2	OBIT1	IBIT3	IBIT2	IBIT1	MCKINH	DZINH	ADPD

Note 15: At a reset, the initial values are SYNM2 = SYNM1 = 0, RLS = 1, D0 = 00H.

(master mode, 16-bit input/output)

SYNM1, 2: Select sync mode

RLS: Selects the channel clock polarity (when RLS = “H” and LRCK = “L” or when RLS = “L” and LRCK = “H”, L-channel data selected).

OBIT1, 2: Select the digital audio output format.

IBIT1, 2, 3: Select the digital audio input format.

MCKINH: When “H”, disables the MCKO pin output (MCK pin is fixed to low).

DZINH: When “H”, disables the digital zero detection output (DZ pin is fixed to low).

ADPD: When “H”, the AD converter power save and output are masked by setting them to digital zeros.

The MCKINH bit is used to halt the XI input clock (or the halved input clock) output from the MCKO pin. The MCKO pin uses a large output buffer for high-speed clock output. However, to suppress unnecessary output without using this pin, set MCKINH to High.

A function is supported to forcibly mute the DAC output by checking whether digital data input from the SDI pin are all zeroes and by setting the DZ pin high if all-zero input continues for a specified detection time (Table 2.4).

When digital input and analog input are switched, digital input zero detection becomes active, setting the DZ pin to High. The DZINH bit is used to inhibit the DZ pin from going High.

Setting the ADPD bit to High halts the AD converter internal circuits and masks the AD converter output by setting to digital zeros. As some circuitry is halted at this time, the power dissipation drops slightly.

4. AD Converter

The TC9444F incorporates a successive approximation 16-bit AD converter with a two times oversampling rate. The AD converter performs three-channel interleave processing for the line input L/R-channels and the microphone input.

The microphone input is designed to internally generate an echo effect. The microphone main signal and the microphone echo signal are combined outside the IC. The microphone main signal and the microphone echo component can also be added internally using a microphone through-path in the IC.

When not using an AD converter, connect jumpers between the MICI-LPFO1, AIL-LPFO2, and AIR-LPFO3 pins.

5. DA Converter

Incorporates a ΣΔ-type modulation 1-bit DA converter and a tertiary analog post filter.

6. Reset Timing

After turning on the power supply, always perform a reset by setting the /RESET pin to Low.
Figure 6.1 shows the reset and boot timing.
When performing a power-on reset, note the timing shown in Figure 6.2.

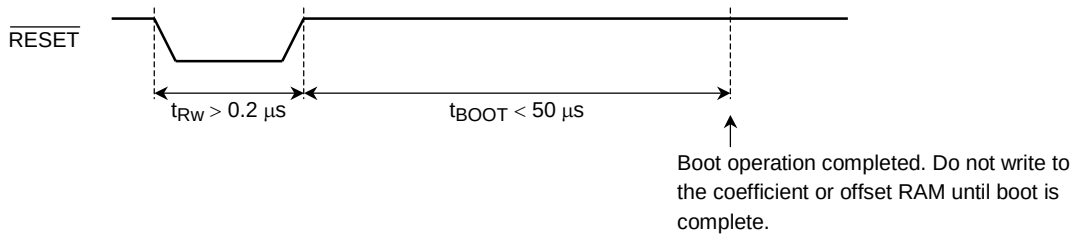


Figure 6.1 Reset and Boot

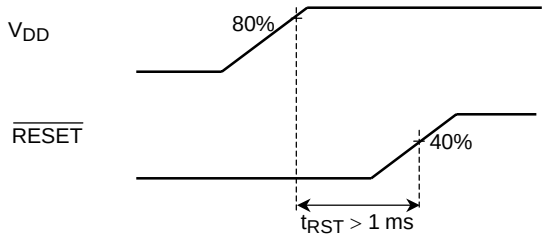


Figure 6.2 Power-On Reset Timing

7. Microcontroller Interface Signal Timing

Microcontroller interface signal timing supports three-lead mode and I^2C bus mode.

7.1 Three-Lead Bus Mode

Setting IFSEL = "H" sets the microcontroller interface to three-lead bus mode.
Setting the $\overline{CS}$ signal = "L" enables control from the microcontroller.
Figure 7.1 shows the interface timing when three-lead mode is selected.
When transmitting two or more commands, be sure to set $\overline{CS}$ to H between each command.
When writing to coefficient or offset RAM, be sure to write the data word by word in 1 fs per word. As coefficient or offset RAM cannot be updated in multiple-word batches, take particular care when updating filter coefficients.

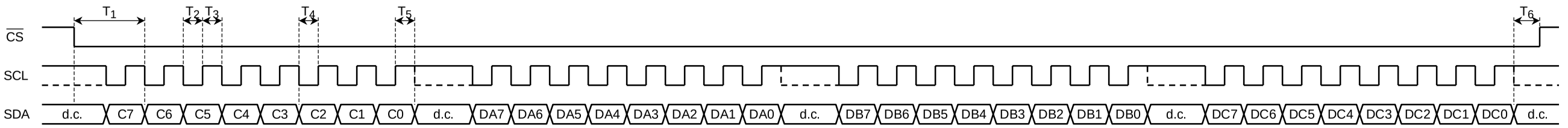
7.2 I^2C Bus Mode

Setting IFSEL = "L" sets the microcontroller interface to I^2C bus mode.
In I^2C bus mode, the $\overline{CS}$ pin can be fixed to "L". Note that the $\overline{CS}$ pin signal can also be used as the chip select signal.
The I^2C slave address is:

```
MSB          LSB
 1101       1000
 ^^^^^^^^^^^^^^
```

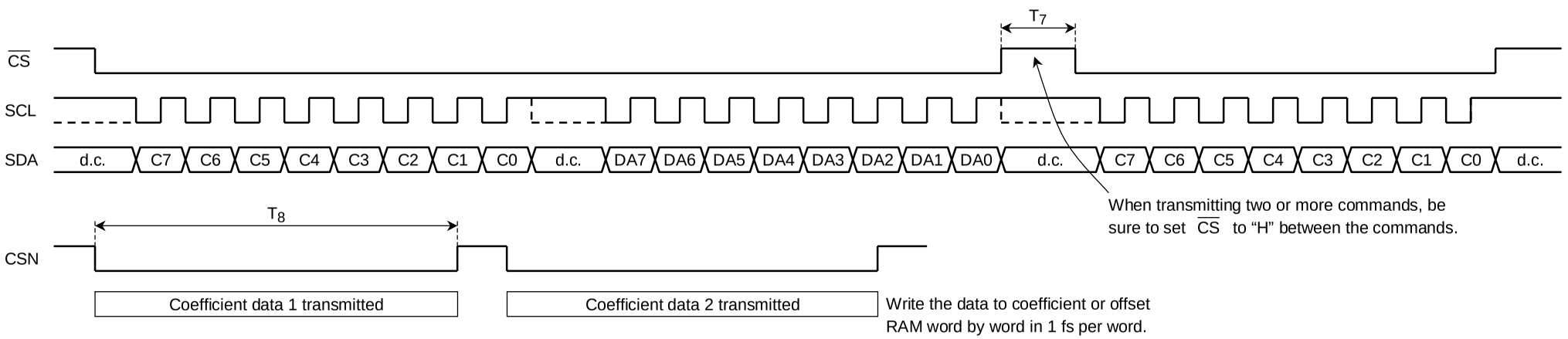
Data can only be written to this address. Therefore, fix the LSB of read/write mode bits to 0.
As I^2C bus mode does not permit continuous writing, insert an END condition after each command, then a START condition to start writing data again.

- **Four-Byte Commands**



d.c.: don't care

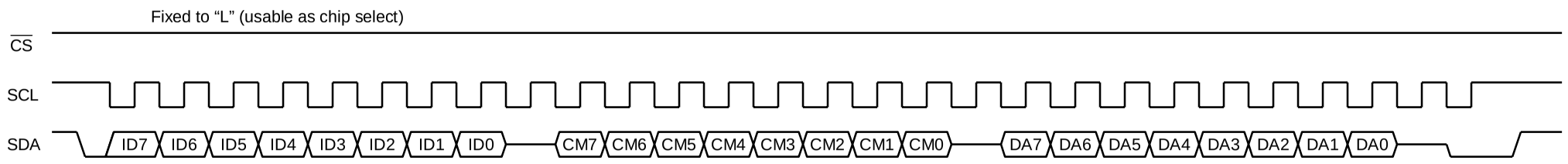
- **When consecutively transmitting two or more commands:**



T_1 > 0.2 μs: Interface setup time
T_2 > 0.2 μs: Shift clock "L" time
T_3 > 0.2 μs: Shift clock "H" time
T_4 > 0.2 μs: Data setup time
T_5 > 0.2 μs: Data hold time
T_6 > 0.2 μs: Interface hold time
T_7 > 0.2 μs: $\overline{CS}$ signal "H" duration
T_8 > 1/fs: Coefficient, offset RAM write cycle

Figure 7.1 Three-Lead Interface Timing (IFSEL = "H")

- **Two-Byte Commands**



- **When transmitting multiple commands**

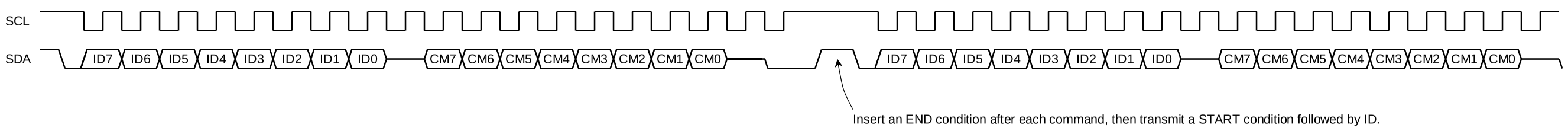
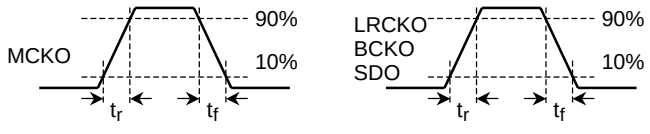


Figure 7.2 I^2C Interface Timing (IFSEL = "L")

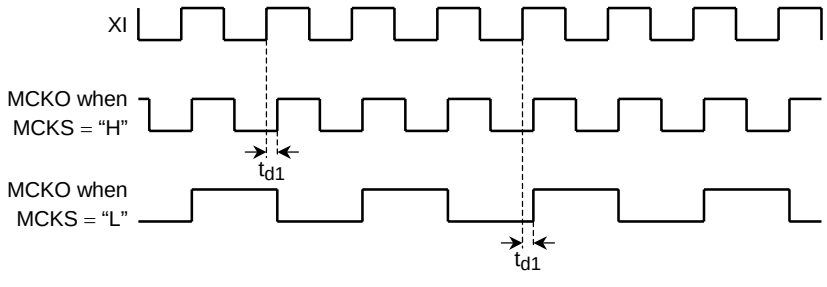
8. Digital Data Input/Output Timing

- **Rising Edge, Falling Edge**



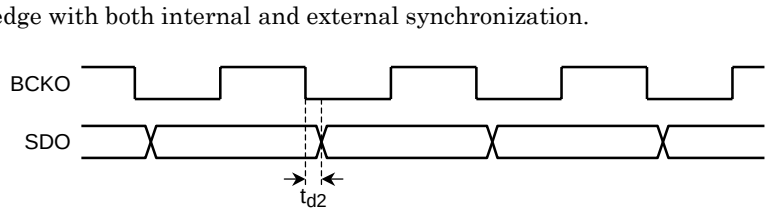
- **Master Clock**

The MCKO pin outputs the XI input clock or the XI input clock divided by two.



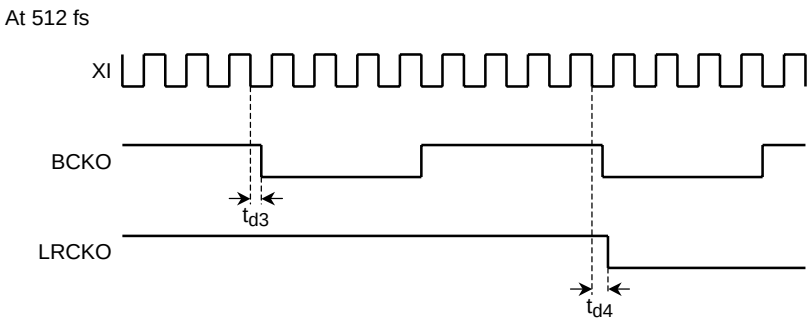
- **SDO Output**

SDO is output on the BCKO falling edge with both internal and external synchronization.

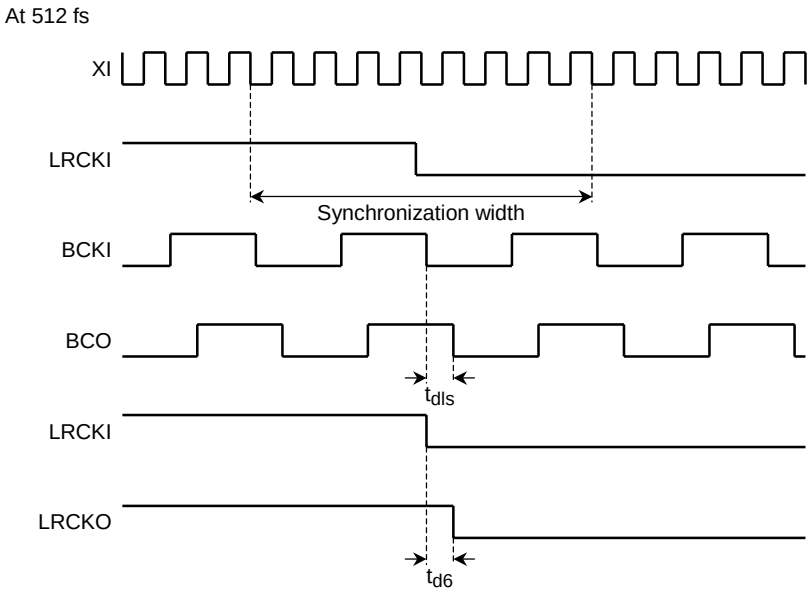


- **Master Mode**

BCKO and LRCKO are divided from the XI input clock.



- **Slave Mode**



- **Data Input**

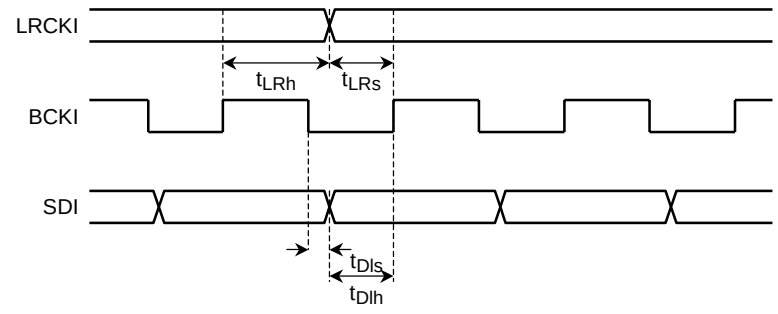


Figure 7.3 Digital Data Input/Output Timing

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 to 6.0	V
Input voltage	V_{in}	−0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	500	mW
Operating temperature	T_{opr}	−40 to 85	°C
Storage temperature	T_{stg}	−55 to 150	°C

Electrical Characteristics (unless otherwise specified, Ta = 25°C, V_{DD} = 5.0 V)

DC Characteristics

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating voltage		V_{DD}	—	Ta = −40 to 85°C	4.5	5.0	5.5	V
Current consumption		I_{DD}	—	XI = 16.9 MHz, 384 fs mode	—	57	80	mA
Input voltage	"H" level	V_{IH}	—	Digital input pins	V_{DD} × 0.8	—	—	V
	"L" level	V_{IL}			0	—	V_{DD} × 0.2	
Input current	"H" level	I_{IH}	—	Digital input pins	—	—	1.0	μA
	"L" level	I_{IL}			−1.0	—	—	
Output current 1	"H" level	I_{OH1}	—	When V_{OH} = 4.5 V	−2.0	—	—	mA
(Note 16)	"L" level	I_{OL1}		When V_{OH} = 0.5 V	—	—	2.0	
Output current 2	"H" level	I_{OH2}	—	When V_{OH} = 4.5 V	−4.0	—	—	mA
(Note 17)	"L" level	I_{OL2}		When V_{OH} = 0.5 V	—	—	4.0	
Pull-up resistors		R_{up}	—	$\overline{\text{RESET}}$, $\overline{\text{TEST}}$ pin	—	50	—	kΩ

Note 16: DZ, EXT0 to F, LRCKO, BCKO, SDO, SDA pins

In I^2C bus mode, the SDA pin is "L" output only (open drain).

Note 17: MCKO pin

AC Characteristics

AD Converter

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Maximum input level	Ain	1	V_{DD} = 5.0 V	—	1.15	1.20	V_{rms}
S/(N + D) ratio	S/N (AD)	1	−50dB, 1 kHz sine wave input	72	80	—	dB
THD + N	THD (AD)	1	−0dB, 1 kHz sine wave input	—	−65	−57	dB
Crosstalk	CT (AD)	1	—	—	−68	−60	dB

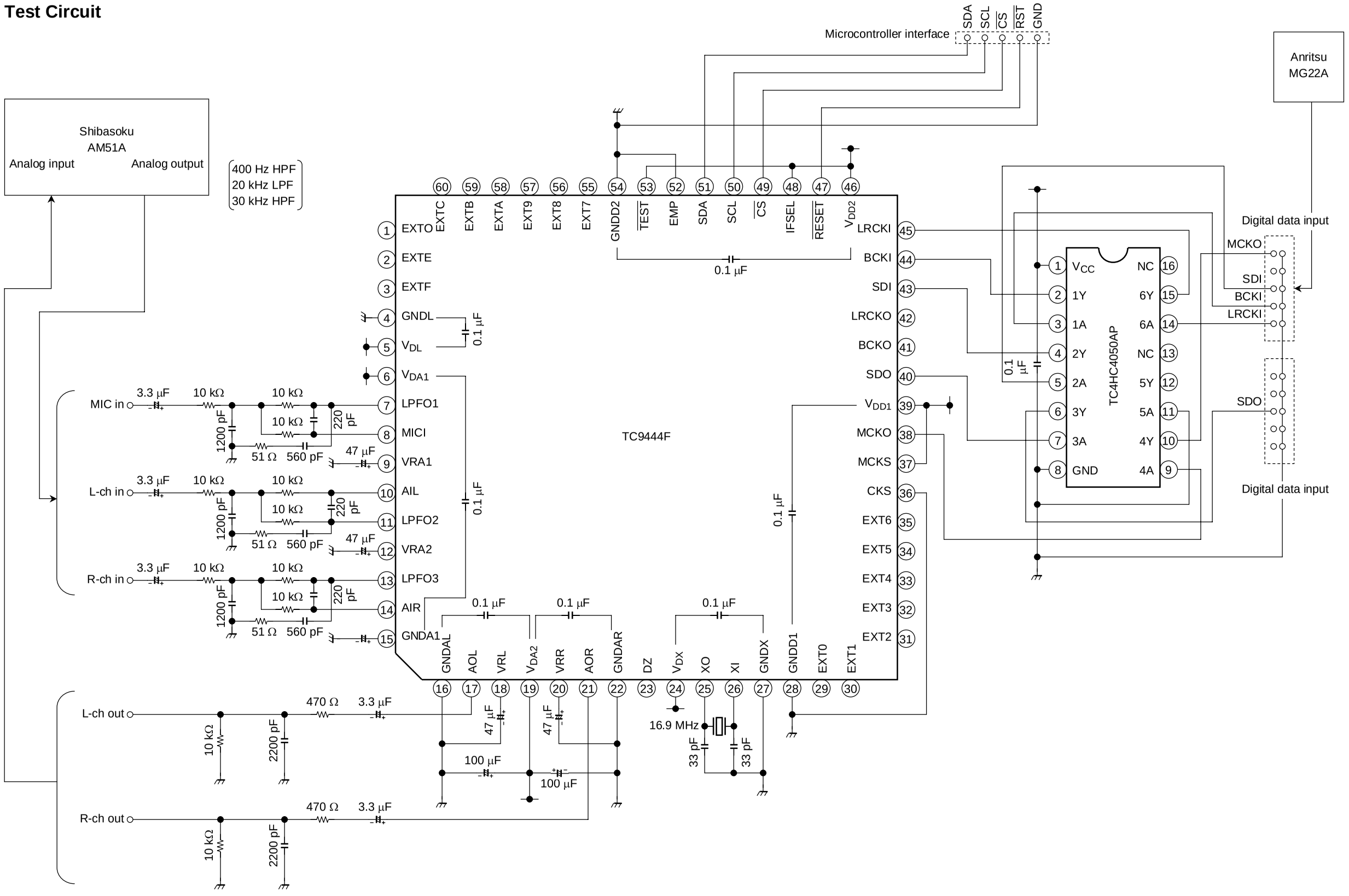
DA Converter

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output level	Aout	1	—	—	1.2	—	V_{rms}
S/N ratio	S/N (DA)	1	−30dB, 1 kHz sine wave input	84	93	—	dB
THD + N	THD (DA)	1	−0dB, 1 kHz sine wave input	—	−86	−78	dB
Crosstalk	THD (DA)	1	−0dB, 10 kHz sine wave input	—	−83	−75	dB
	CT (DA)	1	—	—	−90	−82	

Timings

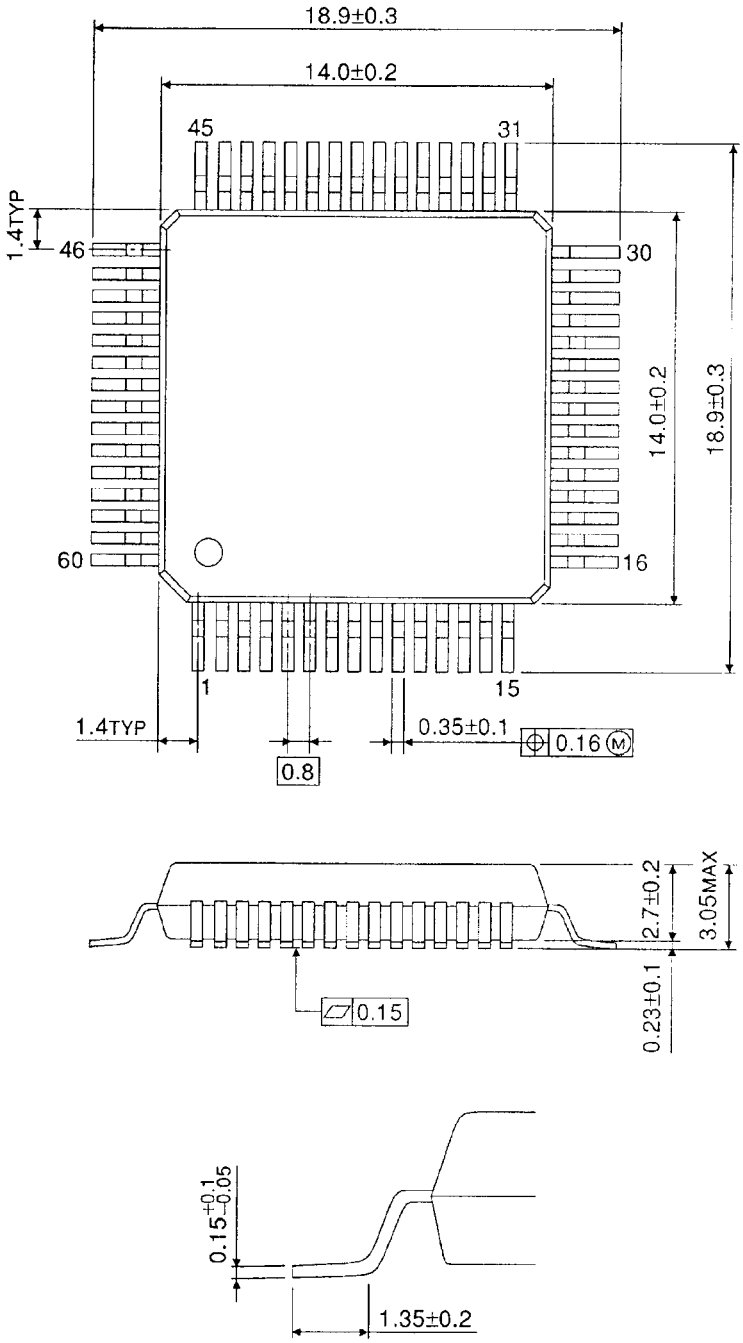
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Rise time		t_r	—	CL = 50 pF, LRCKO, BCKO, SDO	—	—	30	ns
				MCKO	—	—	20	
Fall time		t_f	—	CL = 50 pF, LRCKO, BCKO, SDO	—	—	30	ns
				MCKO	—	—	20	
Delay time	Common	t_{d1}	—	XI → MCKO	—	—	20	ns
		t_{d2}		BCKO → SDO	—	—	5	
	In master mode	t_{d3}		XI → BCKO	—	—	15	
		t_{d4}		XI → LRCKO	—	—	30	
	In slave mode	t_{d5}		BCKI → BCKO	—	—	30	
		t_{d6}		LRCKI → LRCKO	—	—	30	
SDI setup time		t_{DIs}	—	—	50	—	—	ns
SDI hold time		t_{DIh}	—	—	50	—	—	ns
LRCKI setup time		t_{LRs}	—	—	50	—	—	ns
LRCKI hold time		t_{LRh}	—	—	50	—	—	ns
Interface setup time		T_1	—	—	0.2	—	—	μs
Interface shift clock pulse width		T_2, T_3	—	—	0.2	—	—	μs
Interface data setup time		T_4	—	—	0.2	—	—	μs
Interface data hold time		T_5	—	—	0.2	—	—	μs
Interface hold time		T_6	—	—	0.2	—	—	μs
Interface $\overline{CS}$ signal “H” duration		T_7	—	—	0.2	—	—	μs
Coefficient and offset RAM write cycle		T_8	—	—	1/fs	—	—	s
Power-on reset time		t_{RST}	—	—	1	—	—	ms
Reset pulse width		t_{Rw}	—	—	0.2	—	—	μs
Boot time		t_{BOOT}	—	Time required for boot	—	—	50	μs

Test Circuit



Package Dimensions

QFP60-P-1414-0.80D Unit : mm



Weight: 1.08 g (typ.)

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000707EBA

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