

TOSHIBA

TCD2551D

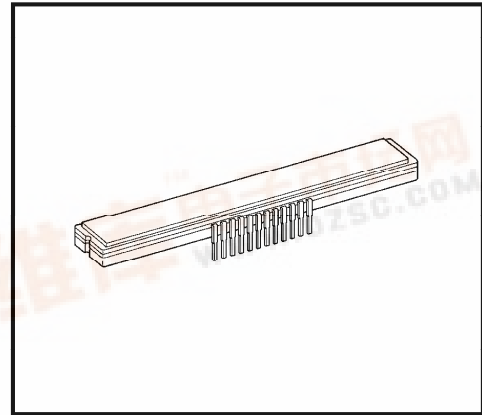
TENTATIVE TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

TCD2551D

The TCD2551D is a high sensitive and low dark current 5340 elements×3 line CCD color image sensor. The sensor is designed for color scanner. The device contains a row of 5340 elements×3 line photodiodes which provide a 24 lines/mm across a A4 size paper. The device is operated by 5V pulse, and 12V power supply.

FEATURES

- Number of Image Sensing Elements : 5340 elements×3 line
- Image Sensing Element Size : 8μm by 8μm on 8μm centers
- Photo Sensing Region : High sensitive pn photodiode
- Clock : 2 phase (5V)
- Distance Between Photodiode Array : 64μm (8 Lines)
- Internal Circuit : Sample and Hold circuit, Clamp circuit
- Package : 24 pin DIP
- Color Filter : Red, Green, Blue



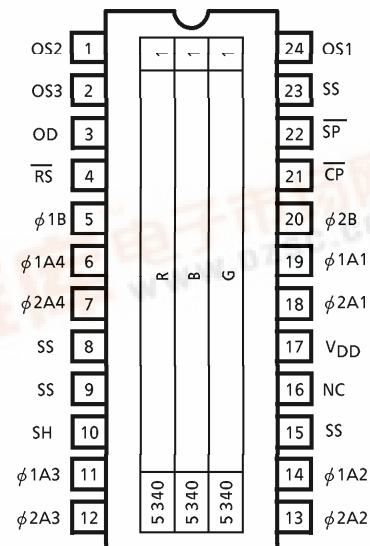
Weight : 6.5g (Typ.)

MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	V_{ϕ}	-0.3~8	V
Shift Pulse Voltage	V_{SH}		V
Reset Pulse Voltage	V_{RS}		V
Sample and Hold Pulse Voltage	V_{SP}		V
Clamp Pulse Voltage	V_{CP}		V
Power Supply Voltage	V_{OD} V_{DD}	-0.3~15	V
Operating Temperature	T_{opr}	0~60	°C
Storage Temperature	T_{stg}	-25~85	°C

(Note 1) All voltage are with respect to SS terminals (Ground).

PIN CONNECTIONS



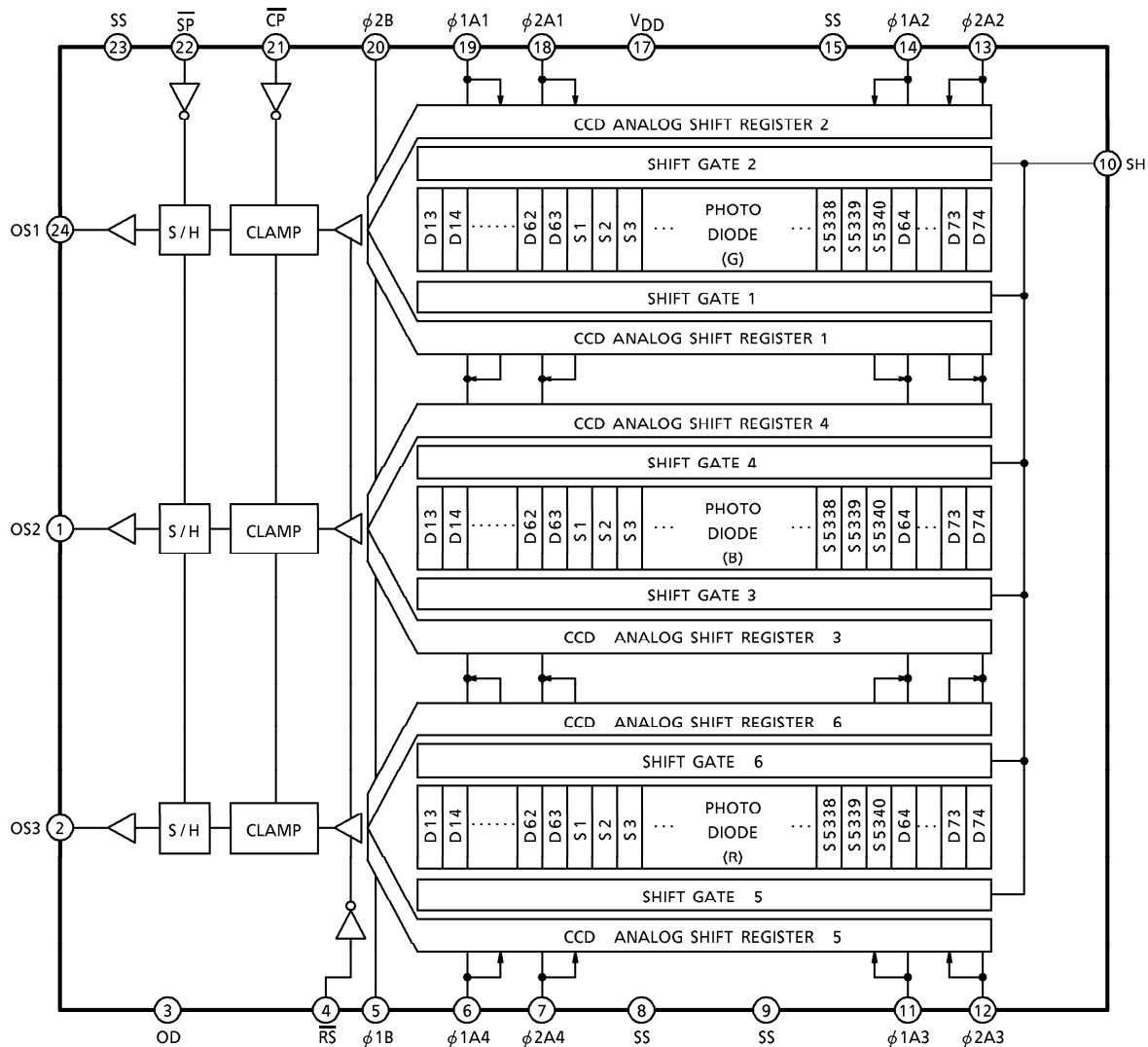
(TOP VIEW)

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CIRCUIT DIAGRAM



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PIN NAMES

PIN No.	SYMBOL	NAME	PIN No.	SYMBOL	NAME
1	OS2	Signal Output 2 (Blue)	13	ϕ 2A2	Clock 2 (Phase 2)
2	OS3	Signal Output 3 (Red)	14	ϕ 1A2	Clock 2 (Phase 1)
3	OD	Power (Analog)	15	SS	Ground
4	\overline{RS}	Reset Gate	16	NC	Non Connection
5	ϕ 1B	Final Stage Clock (phase 1)	17	V _{DD}	Power (Digital)
6	ϕ 1A4	Clock 4 (Phase 1)	18	ϕ 2A1	Clock 1 (Phase 2)
7	ϕ 2A4	Clock 4 (Phase 2)	19	ϕ 1A1	Clock 1 (Phase 1)
8	SS	Ground	20	ϕ 2B	Final Stage Clock (phase 2)
9	SS	Ground	21	\overline{CP}	Clamp Gate
10	SH	Shift Gate	22	\overline{SP}	Sample and Hold Gate
11	ϕ 1A3	Clock 3 (Phase 1)	23	SS	Ground
12	ϕ 2A3	Clock 3 (Phase 2)	24	OS1	Signal Output 1 (Green)

OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{OD} = 12V, V ϕ = V \overline{RS} = V_{SH} = V \overline{CP} = 5V (PULSE), f ϕ = 0.5MHz, f \overline{RS} = 1.0MHz,
 LOAD RESISTANCE = 100k Ω , t_{INT} (INTEGRATION TIME) = 10ms,
 LIGHT SOURCE = A LIGHT SOURCE + CM500S FILTER (t = 1.0mm))

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Responsivity	Red	R _R	3.7	5.3	6.9	V / lx·s	(Note 2)
	Green	R _G	5.3	7.7	10.0		
	Blue	R _B	2.0	2.9	3.8		
Photo Response Non Uniformity		PRNU (1)	—	10	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Register Imbalance		RI	—	—	3	%	(Note 5)
Saturation Output Voltage		V _{SAT}	2.0	2.5	—	V	(Note 6)
Saturation Exposure		SE	0.20	0.32	—	lx·s	(Note 7)
Dark Signal Voltage		V _{DRK}	—	3.0	9.0	mV	(Note 8)
Dark Signal Non Uniformity		DSNU	—	4.0	12.0	mV	(Note 9)
DC Power Dissipation		P _D	—	500	550	mW	
Total Transfer Efficiency		TTE	92	—	—	%	
Output Impedance		Z _O	—	0.3	1.0	k Ω	
DC Signal Output Voltage		V _{OS}	3.0	6.0	8.0	V	(Note 10)
Random Noise		N _{Dσ}	—	1.25	—	mV	(Note 11)

(Note 2) Responsivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

(Note 3) PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature. The amount of the incident light is 50% of SE (Typ.)

$$PRNU (1) = \frac{\Delta\bar{x}}{\bar{x}} \times 100 (\%)$$

Where \bar{x} is average of total signal outputs and $\Delta\bar{x}$ is the maximum deviation from \bar{x} .

(Note 4) PRNU (3) is defined as maximum voltage difference between two adjacent pixels, where measured at 5% of SE (Typ.).

(Note 5) RI is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$RI = \frac{\sum_{n=1}^{5339} |x_n - x_{n+1}|}{5339 \cdot \bar{x}} \times 100 (\%)$$

Where x_n and x_{n+1} are signal outputs of each pixel. \bar{x} is average of signal outputs of all effective pixels.

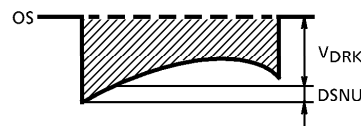
(Note 6) V_{SAT} is defined as minimum Saturation Output Voltage of all effective pixels.

(Note 7) Definition of SE

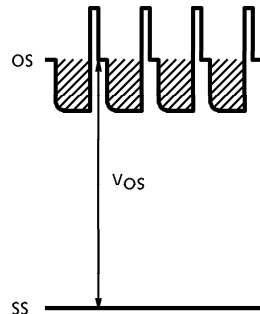
$$SE = \frac{V_{SAT}}{R_G} (lx \cdot s)$$

(Note 8) V_{DRK} is defined as average dark signal voltage of all effective pixels.

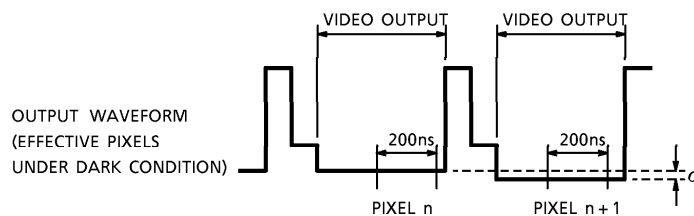
(Note 9) DSNU is defined as different voltage between V_{DRK} and V_{MDK} , when V_{MDK} is maximum dark voltage.



(Note 10) DC Signal Output Voltage is defined as follows:



(Note 11) Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark condition) calculated by the following procedure.



- 1) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
- 2) Each of the output levels at video output periods averaged over 200 nanosecond period to get V_n and V_{n+1} .
- 3) V_{n+1} is subtracted from V_n to get ΔV .

$$\Delta V = V_n - V_{n+1}$$
- 4) The standard deviation of ΔV is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30} \sum_{i=1}^{30} |\Delta V_i| \quad \sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} (|\Delta V_i| - \overline{\Delta V})^2}$$

- 5) Procedure 2), 3) and 4) are repeated 10 times to get 10 sigma values.

$$\overline{\sigma} = \frac{1}{10} \sum_{j=1}^{10} \sigma_j$$

- 6) $\overline{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify the random noise as follows.

$$\text{Random noise} = \frac{1}{\sqrt{2}} \overline{\sigma}$$

OPERATING CONDITION

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Pulse Voltage	"H" Level	$V\phi 1A$	4.5	5.0	5.5	V	
	"L" Level	$V\phi 2A$	0	—	0.5		
Final Stage Clock Pulse Voltage	"H" Level	$V\phi 1B$	4.5	5.0	5.5	V	
	"L" Level	$V\phi 2B$	0	—	0.5		
Shift Pulse Voltage	"H" Level	V_{SH}	$V\phi A"H"-0.5$	$V\phi A"H"$	$V\phi A"H"$	V	(Note 12)
	"L" Level		0	—	0.5		
Reset Pulse Voltage	"H" Level	V_{RS}	4.5	5.0	5.5	V	
	"L" Level		0	—	0.5		
Sample and Hold Pulse Voltage	"H" Level	V_{SP}	4.5	5.0	5.5	V	(Note 13)
	"L" Level		0	—	0.5		
Clamp Pulse Voltage	"H" Level	V_{CP}	4.5	5.0	5.5	V	
	"L" Level		0	—	0.5		
Power Supply Voltage		V_{OD} V_{DD}	11.4	12.0	13.0	V	

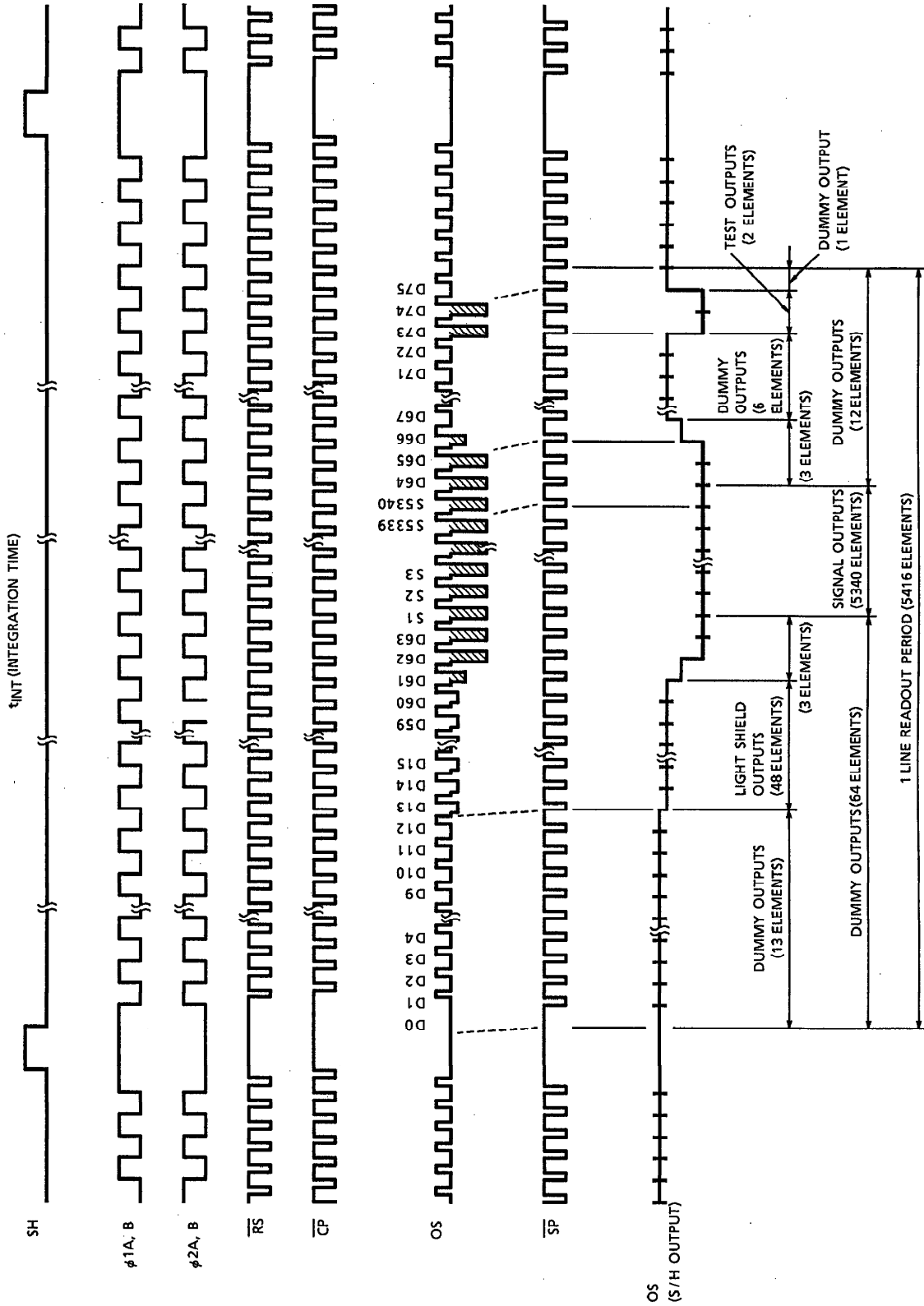
(Note 12) $V\phi A"H"$ means the high level voltage of $V\phi A$ when SH pulse is high level.

(Note 13) Supply "L" Level to \overline{SP} terminal when sample and hold circuitry is not used.

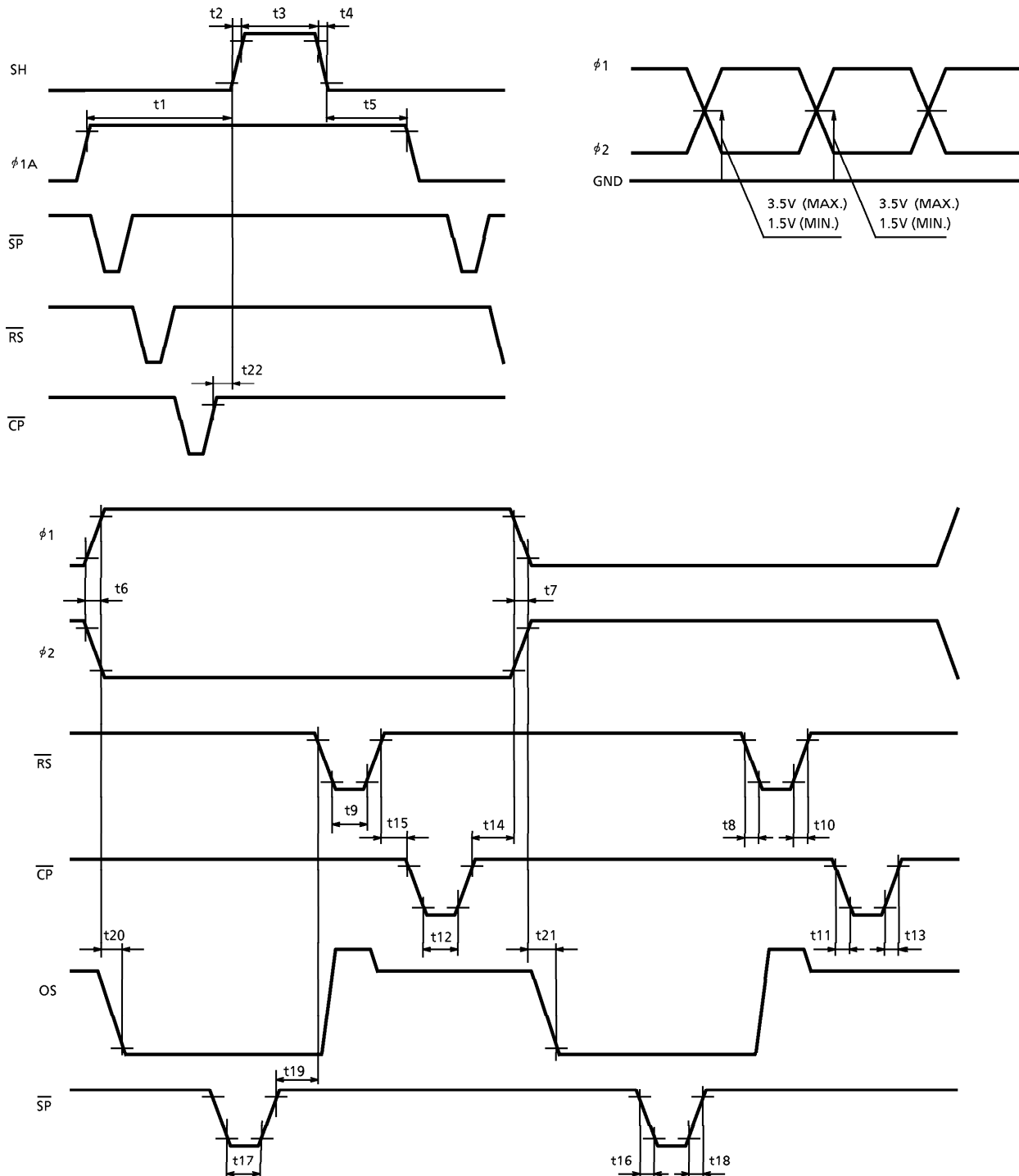
CLOCK CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Pulse Frequency	$f\phi$	—	0.5	3	MHz	
Reset Pulse Frequency	f_{RS}	—	1	6	MHz	
Sample and Hold Pulse Frequency	f_{SP}	—	1	6	MHz	
Clamp Pulse Frequency	f_{CP}	—	1	6	MHz	
Clock Capacitance	$C\phi A$	—	700	—	pF	
Final Stage Clock Capacitance	$C\phi B$	—	50	—	pF	
Shift Gate Capacitance	C_{SH}	—	20	—	pF	
Reset Gate Capacitance	C_{RS}	—	20	—	pF	
Sample and Hold Gate Capacitance	C_{SP}	—	20	—	pF	
Clamp Gate Capacitance	C_{CP}	—	20	—	pF	

TIMING CHART



TIMING REQUIREMENTS



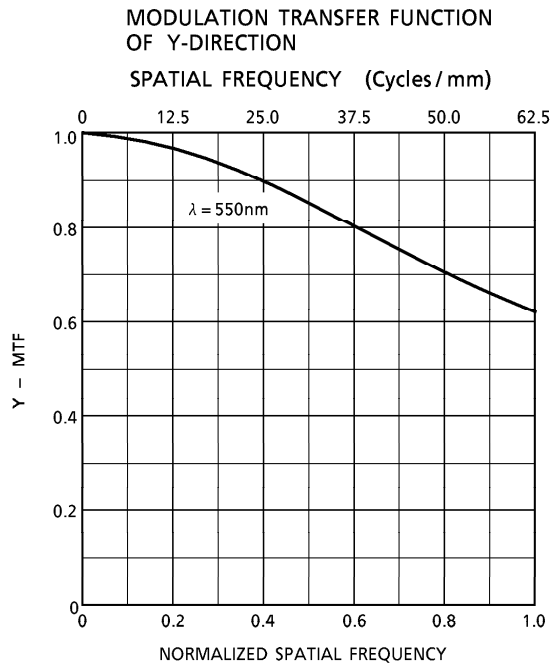
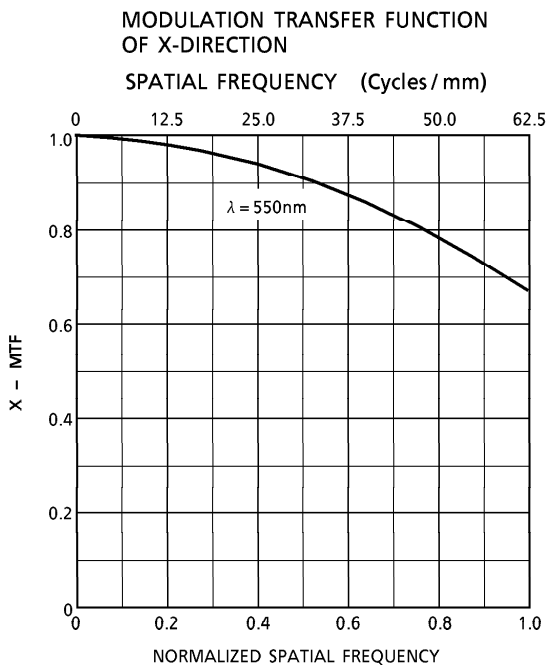
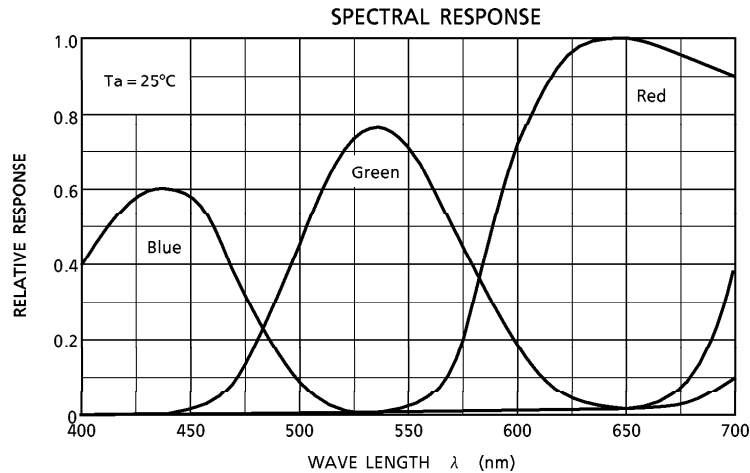
TIMING REQUIREMENTS (Cont'd)

CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 14)	MAX.	UNIT
Pulse Timing of SH and ϕ 1A	t1	110	1000	—	ns
	t5	200	1000	—	
SH Pulse Rise Time, Fall Time	t2, t4	0	50	—	ns
ϕ 1, ϕ 2 Pulse Rise Time, Fall Time	t6, t7	0	50	—	ns
RS Pulse Rise Time, Fall Time	t8, t10	0	20	—	ns
\overline{SP} Pulse Rise Time, Fall Time	t16, t18	0	20	—	ns
\overline{CP} Pulse Rise Time, Fall Time	t11, t13	0	20	—	ns
SH Pulse Width	t3	1000	2000	—	ns
RS Pulse Width	t9	50	100	—	ns
\overline{SP} Pulse Width	t17	50	100	—	ns
Pulse Timing of \overline{RS} and \overline{SP}	t19	0	20	—	ns
Video Data Delay Time (Note 15)	t20, t21	—	50	—	ns
\overline{CP} Pulse Width	t12	10	100	—	ns
Pulse Timing of ϕ 1B, ϕ 2B and \overline{CP}	t14	5	40	—	ns
Pulse Timing of \overline{RS} and \overline{CP}	t15	0	20	—	ns
Pulse Timing of SH and \overline{CP}	t22	0	500	—	ns

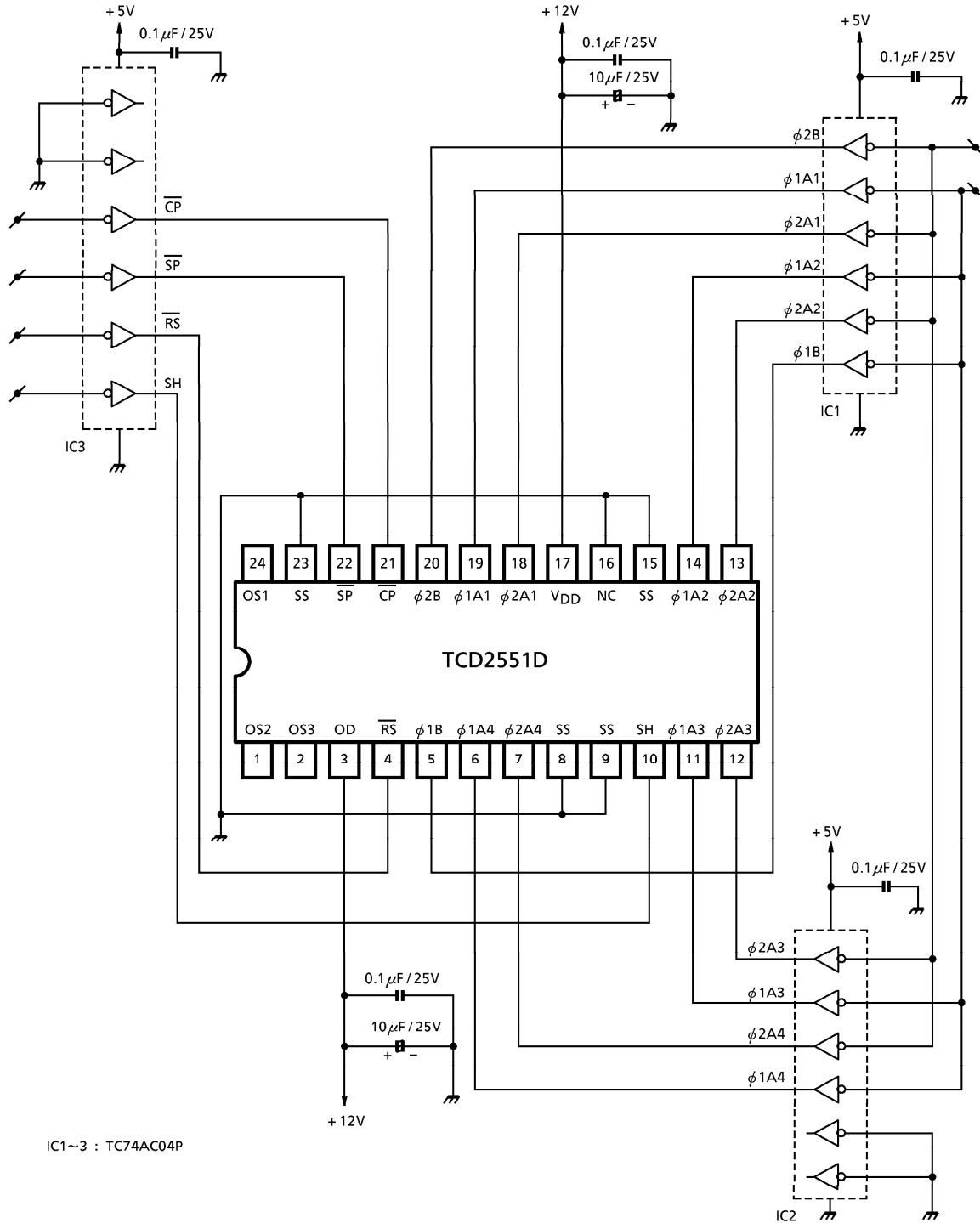
(Note 14) TYP. is the case of $f_{RS} = 1.0\text{MHz}$.

(Note 15) Load Resistance is $100\text{k}\Omega$.

TYPICAL PERFORMANCE CURVES



TYPICAL DRIVE CIRCUIT



IC1~3 : TC74AC04P

CAUTION**1. Window Glass**

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂.

Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

CCD sensor is sensitive to infrared light.

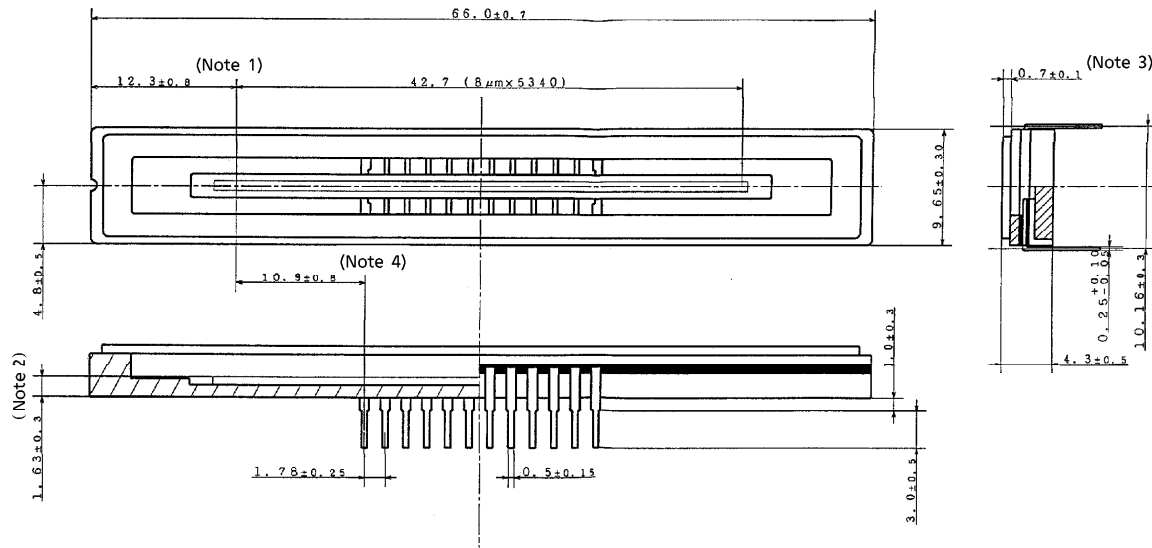
Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Lead Frame Forming

Since this package is not strong against mechanical stress, you should not reform the lead frame. We recommend to use a IC-inserter when you assemble to PCB.

OUTLINE DRAWING

Unit : mm



- (Note 1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
- (Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
- (Note 3) GLASS THICKNES ($n = 1.5$)
- (Note 4) No. 1 SENSOR ELEMENT (S1) TO EDGE OF NO. 1 PIN.

Weight : 6.5g (Typ.)