Ultra Low Power/Voltage CMOS SRAM
128K X 16 bit

BS616UV2019

■ FEATURES

- Wide Vcc operation voltage :
  C-grade: 1.8V~3.6V
  I-grade: 1.9V~3.6V
  (Vcc_min.=1.65V at 25ºC)
- Ultra low power consumption :
  Vcc = 2.0V C-grade: 8mA (Max.) operating current
  I -grade: 10mA (Max.) operating current
  0.20uA (Typ.) CMOS standby current
  Vcc = 3.0V C-grade: 11mA (Max.) operating current
  I -grade: 13mA (Max.) operating current
  0.30uA (Typ.) CMOS standby current
- High speed access time :
  -85 85ns (Max.)
  -10 100ns (Max.)
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Easy expansion with $\overline{CE}$ and $\overline{OE}$ options
- I/O Configuration x8/x16 selectable by $\overline{LB}$ and $\overline{UB}$ pin
- Data retention supply voltage as low as 1.0V

■ DESCRIPTION

The BS616UV2019 is a high performance, ultra low power CMOS Static Random Access Memory organized as 131,072 words by 16 bits and operates from a wide range of 1.8V to 3.6V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.2uA at 2.0V/25ºC and maximum access time of 85ns at 85ºC.

Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$), active LOW output enable($\overline{OE}$) and three-state output drivers.

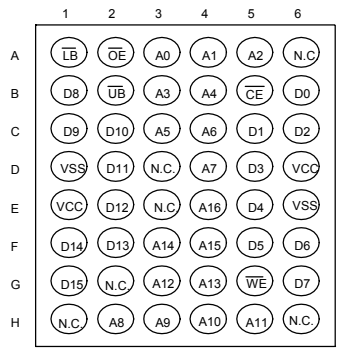
The BS616UV2019 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

The BS616UV2019 is available in DICE form, JEDEC standard 48-pin TSOP Type I package and 48-ball BGA package.

■ PRODUCT FAMILY

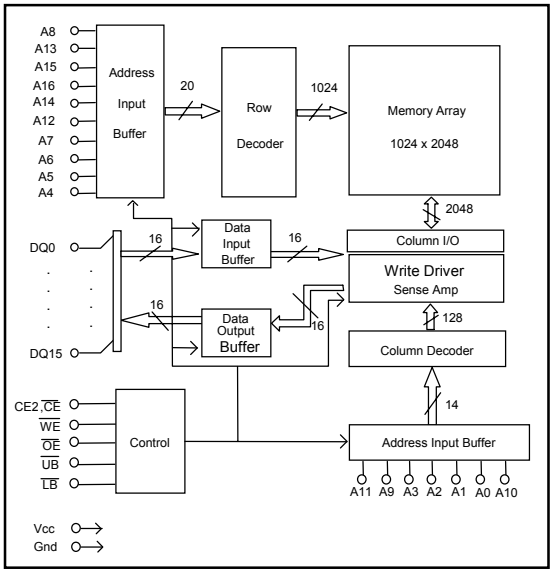
PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED (ns)	POWER DISSIPATION				PKG TYPE
				STANDBY (I_{CCSB1}, Max)		Operating (I_{CC}, Max)		
			C-grade:1.8~3.6V I-grade:1.9~3.6V	Vcc=3.0V	Vcc=2.0V	Vcc=3.0V	Vcc=2.0V	
BS616UV2019DC	+0 ºC to +70 ºC	1.8V ~3.6V	85/100	3.0uA	2.0uA	11mA	8mA	DICE
BS616UV2019TC								TSOP1-48
BS616UV2019AC								BGA-48-0608
BS616UV2019DI	-40 ºC to +85 ºC	1.9V ~ 3.6V	85/100	5.0uA	3.0uA	13mA	10mA	DICE
BS616UV2019TI								TSOP1-48
BS616UV2019AI								BGA-48-0608

■ PIN CONFIGURATIONS



48-ball BGA top view

■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Function
A0-A16 Address Input	These 17 address inputs select one of the 131,072 x 16-bit words in the RAM.
$\overline{CE}$ Chip Enable 1 Input **CE2 Chip Enable 2 Input**	$\overline{CE}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected. (48B BGA ignore CE2 pin)
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
$\overline{LB}$ and $\overline{UB}$ Data Byte Control Input	Lower byte and upper byte data input/output control pins.
DQ0 - DQ15 Data Input/Output Ports	These 16 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
Gnd	Ground

■ TRUTH TABLE

MODE	$\overline{CE}$	CE2 (1)	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	D0~D7	D8~D15	Vcc CURRENT
Not selected (Power Down)	H	X	X	X	X	X	High Z	High Z	I_{CCSB} , I_{CCSB1}
	X	L	X	X	X	X	High Z	High Z	I_{CCSB} , I_{CCSB1}
	X	X	X	X	H	H	High Z	High Z	I_{CCSB} , I_{CCSB1}
Output Disabled	L	H	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	H	L	L	L	Dout	Dout	I_{CC}
					H	L	High Z	Dout	I_{CC}
					L	H	Dout	High Z	I_{CC}
Write	L	H	L	X	L	L	Din	Din	I_{CC}
					H	L	X	Din	I_{CC}
					L	H	Din	X	I_{CC}

1. 48B BGA ignore CE2 condition.

■ ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +85	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	$0^{O}C$ to $+70^{O}C$	1.8V ~ 3.6V
Industrial	$-40^{O}C$ to $+85^{O}C$	1.9V ~ 3.6V

■ CAPACITANCE (1) (TA = 25ºC, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	6	pF
CDQ	Input/Output Capacitance	VI/O=0V	8	pF

1. This parameter is guaranteed and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS (TA = -40 to + 85ºC)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN.	TYP. (1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		Vcc=2.0V	-0.3 (6)	--	0.6	V
			Vcc=3.0V			0.8	
V_{IH}	Guaranteed Input High Voltage(2)		Vcc=2.0V	1.4	--	Vcc+0.3	V
			Vcc=3.0V	2.0			
I_{IL}	Input Leakage Current	Vcc = Max, V_{IN}= 0V to Vcc		--	--	1	uA
I_{LO}	Output Leakage Current	Vcc = Max, $\overline{CE}$ = V_{IH} , or CE2(4) = V_{IL}, or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}		--	--	1	uA
V_{OL}	Output Low Voltage	I_{OL} = 0.1mA ; Vcc=Max	Vcc=2.0V	--	--	0.2	V
		I_{OL} = 2.0mA ; Vcc=Max	Vcc=3.0V			0.4	
V_{OH}	Output High Voltage	I_{OH} = -0.1mA ; Vcc=Min	Vcc=2.0V	Vcc-0.2	--	--	V
		I_{OH} = -1.0mA ; Vcc=Min	Vcc=3.0V	2.4			
I_{CC}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, I_{DQ} = 0mA, F = Fmax(3) CE2 = V_{IH}(4)	Vcc=2.0V	--	--	10	mA
			Vcc=3.0V	--	--	13	
I_{CCSB}	Standby Current TTL	$\overline{CE}$ = V_{IH} or CE2 = V_{IL}(4) , I_{DQ} = 0mA	Vcc=2.0V	--	--	0.1	mA
			Vcc=3.0V	--	--	0.5	
I_{CCSB1} (5)	Standby Current CMOS	$\overline{CE}$ ≧ Vcc-0.2V, or CE2 ≦ 0.2V;(4) V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	Vcc=2.0V	--	0.20	3.0	uA
			Vcc=3.0V	--	0.30	5.0	

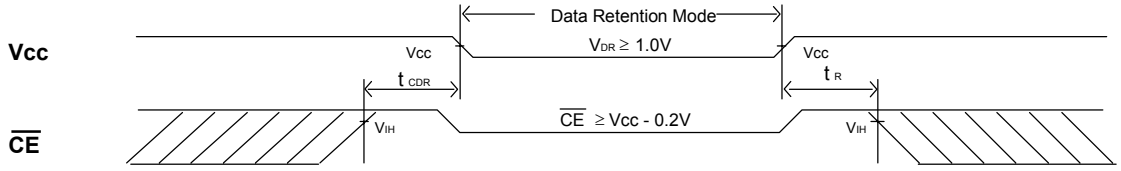
1. Typical characteristics are at T_A = 25ºC.
2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
3. Fmax = $1/t_{RC}$. **4**. 48B BGA ignore CE2 condition. **5**.I_{CCSB1} is 2.0uA/3.0uA at Vcc=2.0V/3.0V and T_A=70ºC.
6. V_{IL} = -1.5V for pulse width less than 30ns

■ DATA RETENTION CHARACTERISTICS (TA = -40 to + 85ºC)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V_{DR}	Vcc for Data Retention	$\overline{CE}$ ≧ Vcc - 0.2V or CE2 ≦ 0.2V(3) V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	1.0	--	--	V
I_{CCDR} (4)	Data Retention Current	$\overline{CE}$ ≧ Vcc - 0.2V or CE2 ≦ 0.2V(3) V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	--	0.1	1.0	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		T_{RC} (2)	--	--	ns

1. Vcc = 1.0V, T_A = + 25ºC
2. t_{RC} = Read Cycle Time
3. 48B BGA ignore CE2 condition.
4. I_{CCDR} is 0.7uA at T_A=70ºC.

■ LOW V_{CC} DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



■AC TEST CONDITIONS

(Test Load and Input/Output Reference)

Input Pulse Levels	Vcc / 0V
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	0.5Vcc
Output Load	C_L = 100pF+1TTL C_L = 30pF+1TTL

■ KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF "STATE

■ AC ELECTRICAL CHARACTERISTICS (TA = -40 to + 85°C)

READ CYCLE (48B BGA ignore CE2 condition)

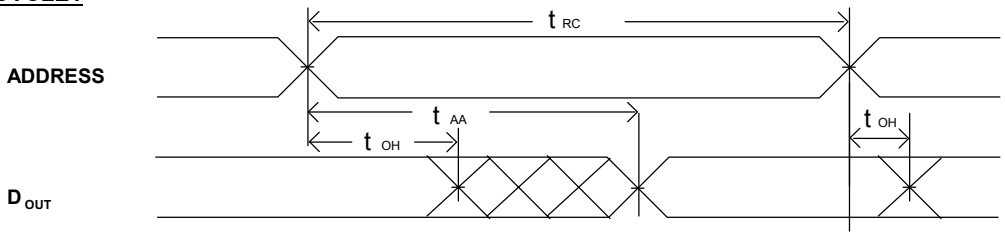
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION		CYCLE TIME : 100ns (Vcc = 1.9~3.6V) MIN.	TYP.	MAX.	CYCLE TIME : 85ns (Vcc = 1.9~3.6V) MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time		100	--	--	85	--	--	ns
t_{AVQV}	t_{AA}	Address Access Time		--	--	100	--	--	85	ns
t_{ELQV}	$t_{ACS1,2}$	Chip Select Access Time	($\overline{CE}$,CE2)	--	--	100	--	--	85	ns
t_{BA}	t_{BA} (1)	Data Byte Control Access Time	($\overline{LB}$,$\overline{UB}$)	--	--	50	--	--	40	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		--	--	50	--	--	40	ns
t_{E1LQX}	t_{CLZ}	Chip Select to Output Low Z	($\overline{CE}$,CE2)	15	--	--	15	--	--	ns
t_{BE}	t_{BE}	Data Byte Control to Output Low Z	($\overline{LB}$,$\overline{UB}$)	15	--	--	15	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z		15	--	--	15	--	--	ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	($\overline{CE}$,CE2)	--	--	40	--	--	35	ns
t_{BDO}	t_{BDO}	Data Byte Control to Output High Z	($\overline{LB}$,$\overline{UB}$)	--	--	40	--	--	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		--	--	35	--	--	30	ns
t_{AXOX}	t_{OH}	Data Hold from Address Change		15	--	--	15	--	--	ns

NOTE :

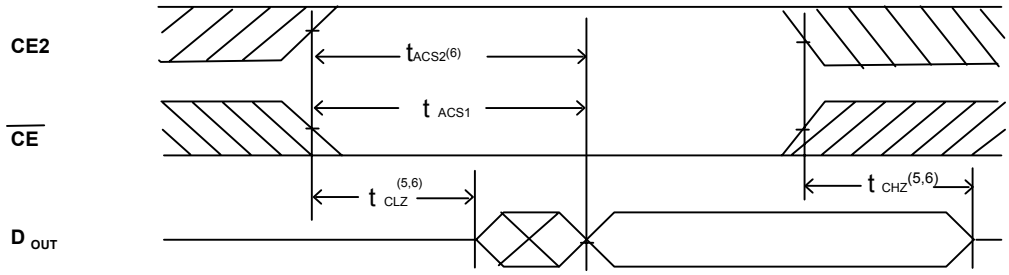
1. t_{BA} is 50ns/40ns (@speed=100ns/85ns) with address toggle. ; t_{BA} is 100ns/85ns (@speed=100ns/85ns) without address toggle.

■ SWITCHING WAVEFORMS (READ CYCLE)

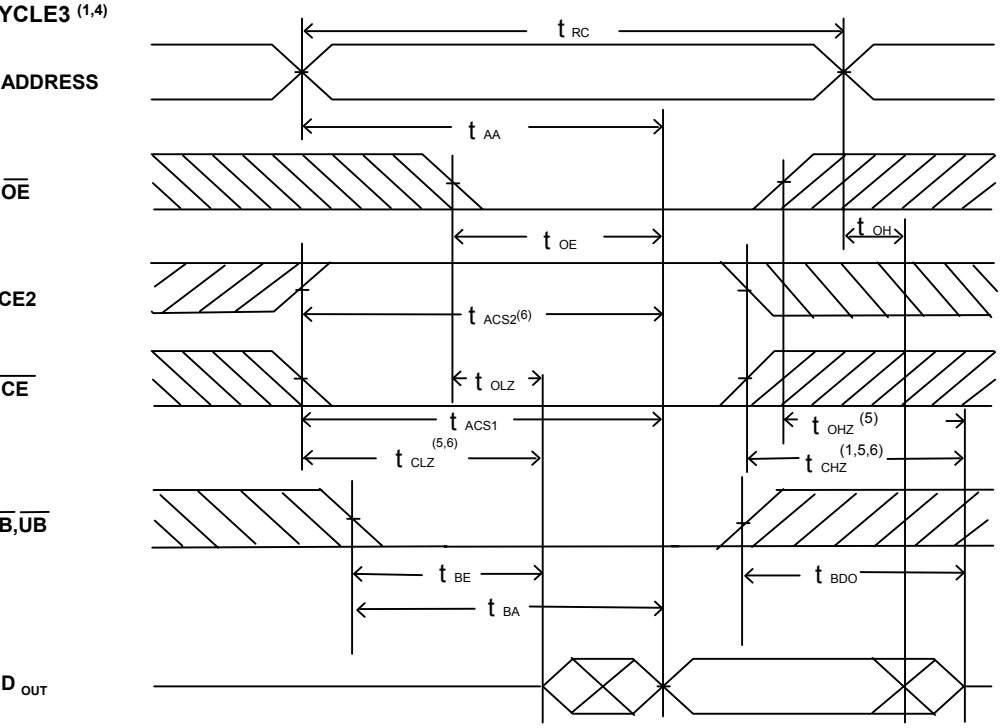
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:
1. $\overline{WE}$ is high in read Cycle.
2. Device is continuously selected when $\overline{CE}$ = V_{IL} and CE2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL} .
5. The parameter is guaranteed but not 100% tested.
6. 48B BGA ignore this parameters related to CE2 .

■ AC ELECTRICAL CHARACTERISTICS (TA = -40 to + 85°C)

WRITE CYCLE (48B BGA ignore CE2 condition)

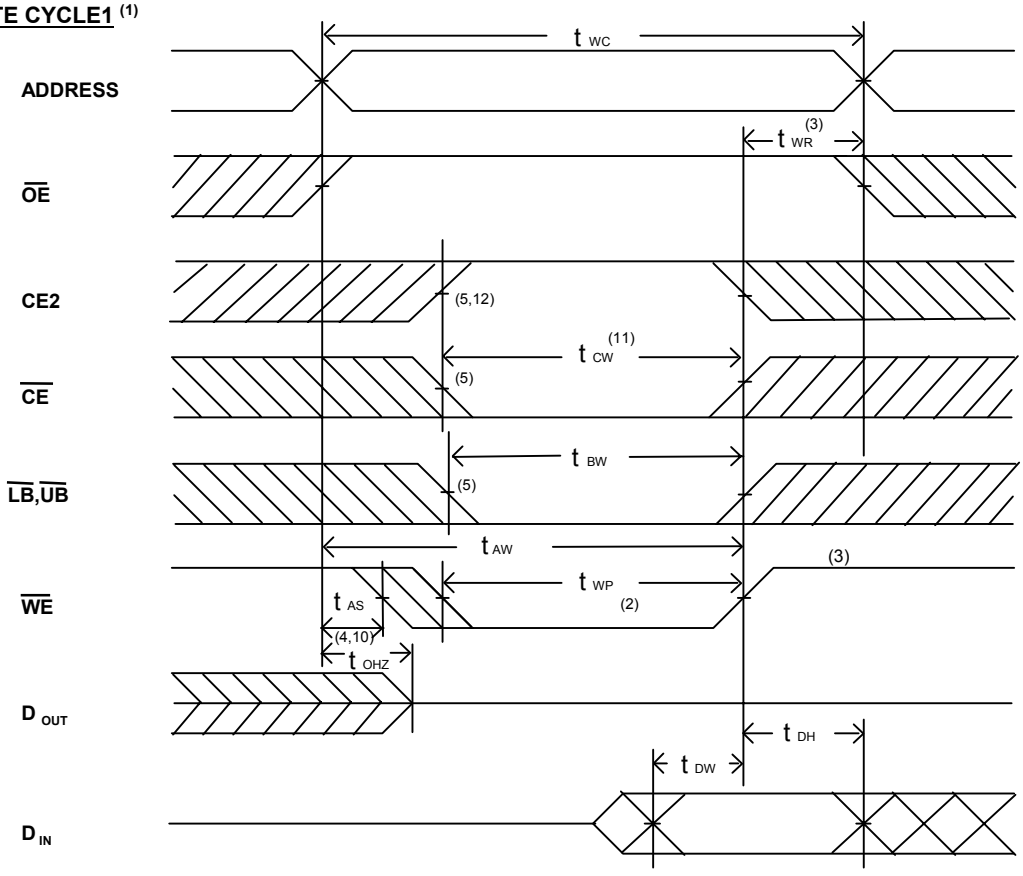
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 100ns (Vcc = 1.9~3.6V) MIN.	TYP.	MAX.	CYCLE TIME : 85ns (Vcc = 1.9~3.6V) MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	100	--	--	85	--	--	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write ($\overline{CE}$,CE2)	100	--	--	85	--	--	ns
t_{AVWL}	t_{AS}	Address Setup Time	0	--	--	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	100	--	--	85	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	50	--	--	40	--	--	ns
t_{WHAX}	t_{WR}	Write recovery Time ($\overline{CE}$,CE2,$\overline{WE}$)	0	--	--	0	--	--	ns
t_{BW}	t_{BW} (1)	Date Byte Control to End of Write ($\overline{LB}$,$\overline{UB}$)	40	--	--	35	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	--	--	40	--	--	35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	40	--	--	35	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	40	--	--	35	ns
t_{WHOX}	t_{OW}	End of Write to Output Active	10	--	--	10	--	--	ns

NOTE :

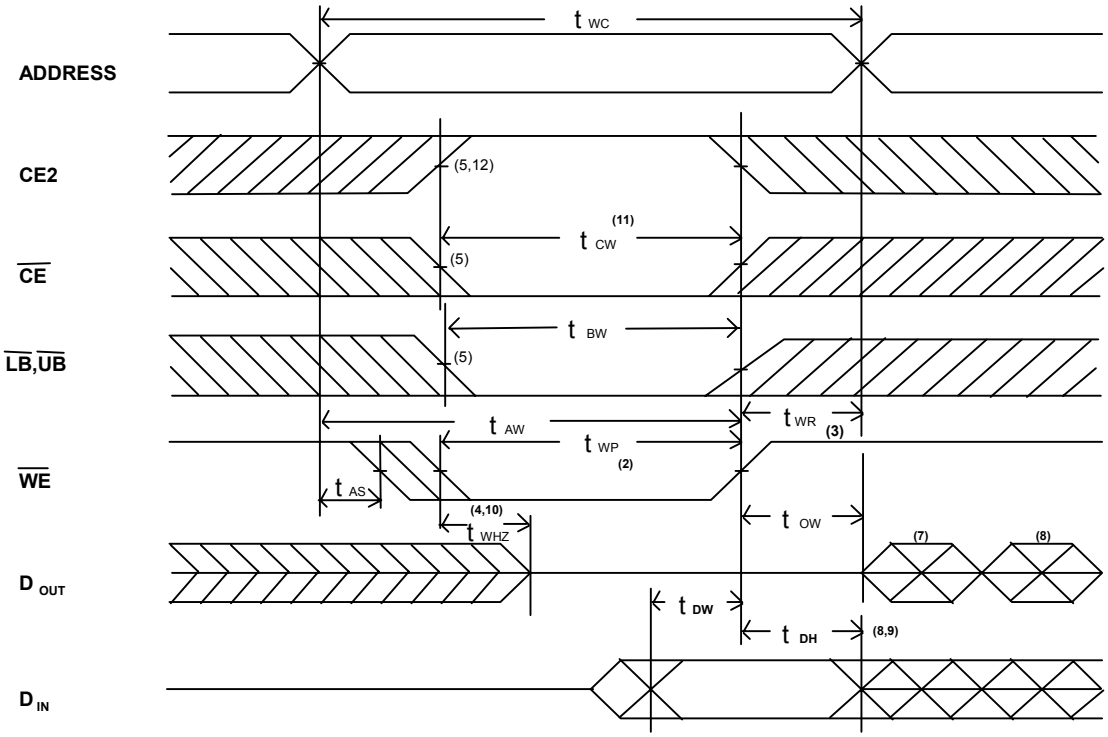
1. t_{BW} is 40ns/35ns (@speed=100ns/85ns) with address toggle. ; t_{BW} is 100ns/85ns (@speed=100ns/85ns) without address toggle.

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (1)

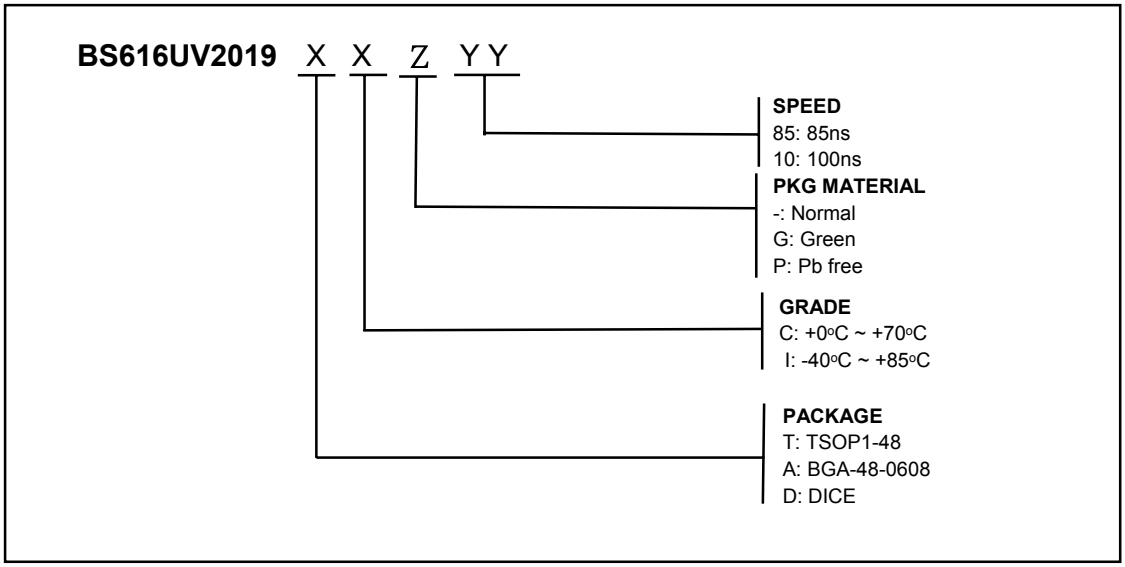


WRITE CYCLE2 (1,6)



NOTES:
1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of CE2, $\overline{CE}$ and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of CE2 going low, or $\overline{CE}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CE2 high transition or $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If CE2 is high or $\overline{CE}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of CE2 going high or $\overline{CE}$ going low to the end of write.
12. 48B BGA ignore this parameters related to CE2 .

■ ORDERING INFORMATION



Note:
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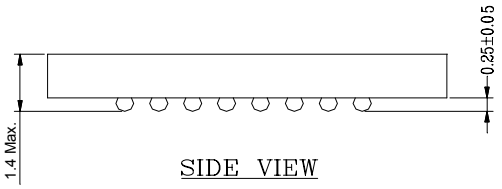
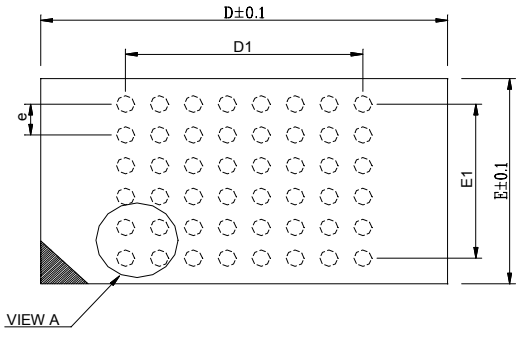
■ PACKAGE DIMENSIONS

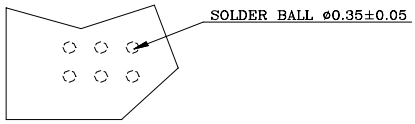


NOTES:
1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

BALL PITCH e = 0.75				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75



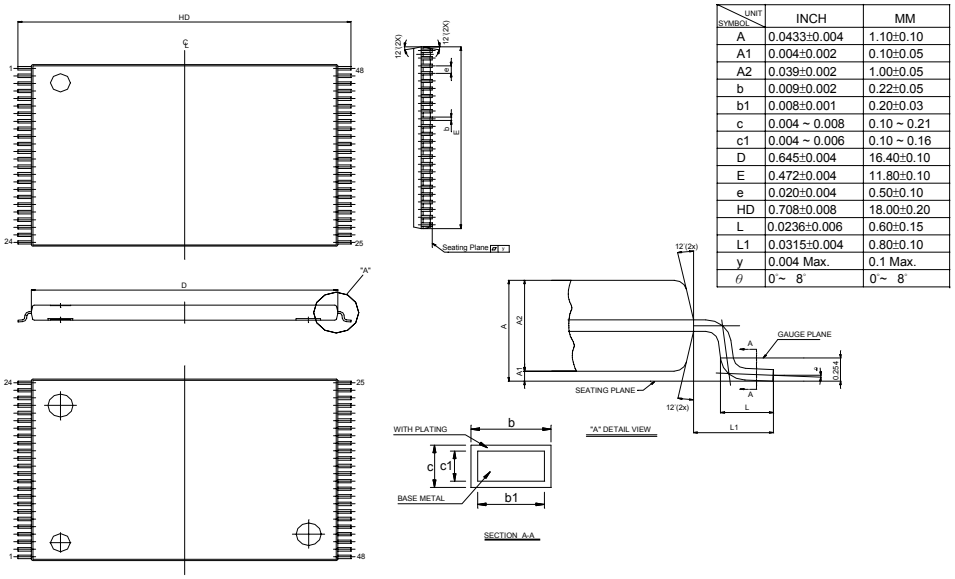
TOP VIEW



VIEW A

48 mini-BGA (6 x 8)

■ PACKAGE DIMENSIONS



SYMBOL \ UNIT	INCH	MM
A	0.0433±0.004	1.10±0.10
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.009±0.002	0.22±0.05
b1	0.008±0.001	0.20±0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.645±0.004	16.40±0.10
E	0.472±0.004	11.80±0.10
e	0.020±0.004	0.50±0.10
HD	0.708±0.008	18.00±0.20
L	0.0236±0.006	0.60±0.15
L1	0.0315±0.004	0.80±0.10
y	0.004 Max.	0.1 Max.
θ	0°~ 8°	0°~ 8°

TSOP1-48PIN