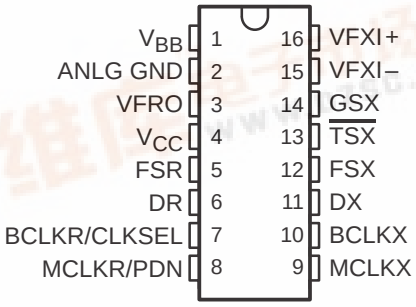
TCM320AC54
MONOLITHIC SERIAL INTERFACE COMBINED PCM CODEC AND FILTER

SCTS043A – NOVEMBER 1994 – REVISED JULY 1996

- **Complete PCM Codec and Filtering System Includes:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter With (sin x)/x Correction**
  - **Active RC Noise Filters**
  - **μ-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Autozero Circuitry**
- **μ-Law Coding**
- **DTAD and DSP Interface Codec**
- **±5-V Operation**
- **Low Operating Power . . . 50 mW Typ**
- **Power-Down Standby Mode . . . 3 mW Typ**
- **Automatic Power Down**
- **TTL- or CMOS-Compatible Digital Interface**
- **Maximizes Line Interface Card Circuit Density**

DW OR N PACKAGE
(TOP VIEW)



description

The TCM320AC54 is comprised of a single-chip PCM codec (pulse-code-modulated encoder and decoder) and PCM line filter. This device provides all the functions required to interface a full-duplex (2-wire) voice telephone circuit with a TDM (time-division-multiplexed) system. Primary applications include:

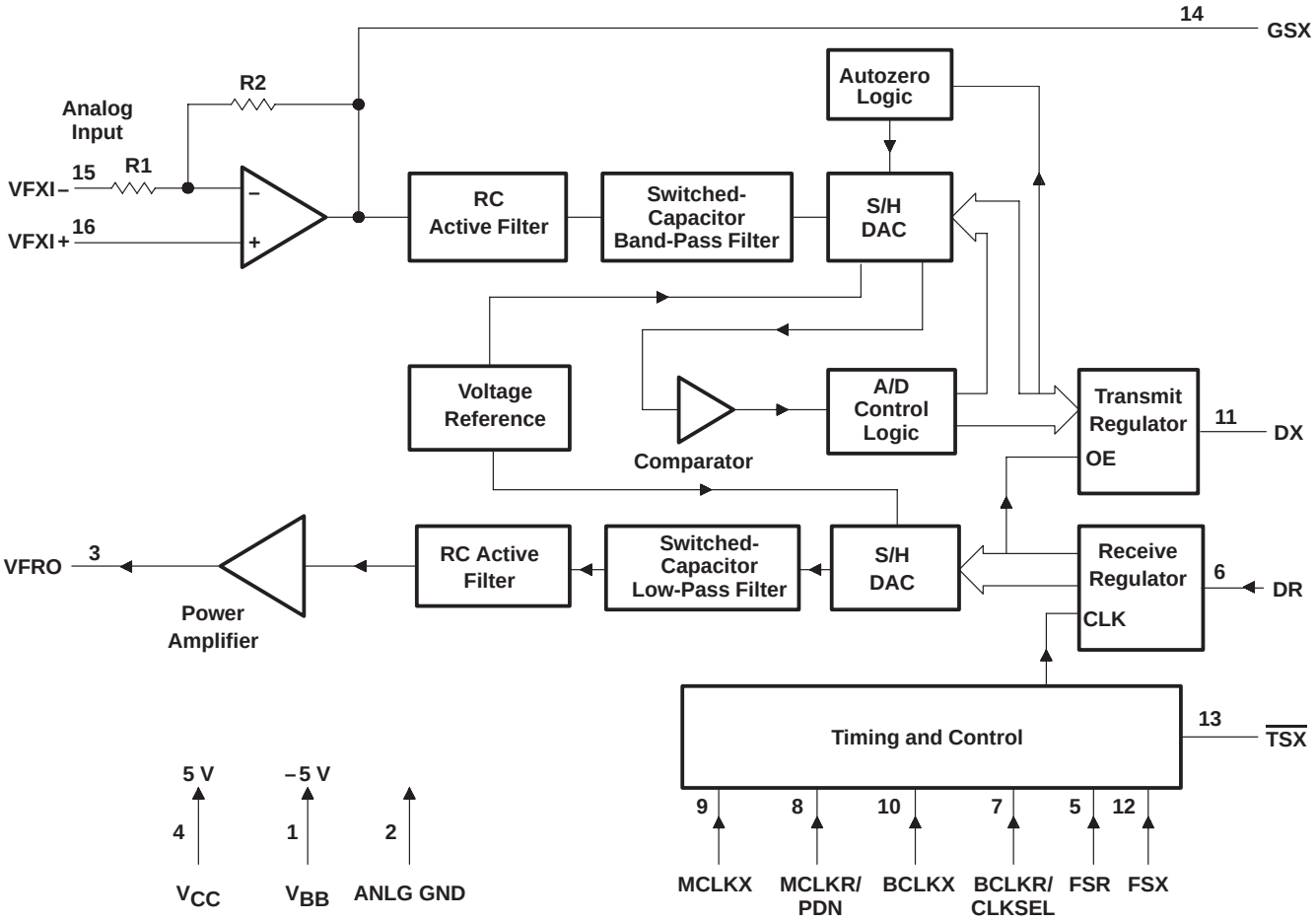
- Line interface for digital transmission and switching of T1 carrier, PABX, and central office telephone systems
- Subscriber line concentrators
- Digital-encryption systems
- Digital signal processing

The device is designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a PCM system. It is intended to be used at the analog termination of a PCM line or trunk. The device requires two transmit and receive master clocks that may be asynchronous (1.536 MHz, 1.544 MHz, or 2.048 MHz), transmit and receive data clocks that are synchronous with the master clock (but can vary from 64 kHz to 2.048 MHz), and transmit and receive frame-sync pulses. The TCM320AC54 provides the band-pass filtering of the analog signals prior to encoding and after decoding of voice and call progress tones.

The TCM320AC54 is characterized for operation from 0°C to 70°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the CMOS gates.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
ANLG GND	2	Analog ground. All signals are referenced to ANLG GND.
BCLKR/CLKSEL	7	Receive bit (data) clock/clock select terminal for master clock. BCLKR/CLKSEL shifts data into DR after the FSR leading edge and can vary from 64 kHz to 2.048 MHz. Alternately, BCLKR/CLKSEL can be a logic input that selects either 1.536 MHz/1.544 MHz or 2.048 MHz for the master clock in the synchronous mode. BCLKX is used for both transmit and receive directions (see Table 1).
BCLKX	10	Transmit bit (data) clock. BCLKX shifts out the PCM data on DX and can vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLKX.
DR	6	Receive data input. PCM data is shifted into DR following the FSR leading edge.
DX	11	The 3-state PCM data output that is enabled by FSX
FSR	5	Frame sync clock input for receive channel. FSR is an 8-kHz pulse train that enables BCLKR to shift PCM data in DR (see Figures 1 and 2 for timing details).
FSX	12	Frame sync clock input for transmit channel. FSX is an 8-kHz pulse train that enables BCLKX to shift out the PCM data on DX (see Figures 1 and 2 for timing details).
GSX	14	Analog output of the transmit input amplifier. GSX is used to externally set gain.
$\overline{\text{MCLKR}}$/PDN	8	Receive master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). $\overline{\text{MCLKR}}$/PDN may be synchronous with MCLKX but should be synchronous with MCLKX for best performance. When the input is continuously low, MCLKX is selected for all internal timing. When the input is continuously high, the device is powered down.
MCLKX	9	Transmit master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). MCLKX may be asynchronous with MCLKR.
$\overline{\text{TSX}}$	13	Transmit time-slot strobe. $\overline{\text{TSX}}$ is an open-drain output that pulses low during the encoder time slot.
V_{BB}	1	Negative power supply. $V_{BB} = -5\ V \pm 10\%$
V_{CC}	4	Positive power supply. $V_{CC} = 5\ V \pm 10\%$
VFRO	3	Analog output of the receive filter
VFXI+	16	Noninverting input of the transmit input amplifier
VFXI–	15	Inverting input of the transmit input amplifier

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Supply voltage, V_{BB} (see Note 1) . . . . . –7 V
Voltage range at any analog input or output . . . . . V_{CC} +0.3 V to V_{BB} –0.3 V
Voltage range at any digital input or output . . . . . V_{CC} +0.3 V to ANLG GND –0.3 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range,T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{BB}	–4.5	–5	–5.5	V
High-level input voltage, V_{IH}	2.2			V
Low-level input voltage, V_{IL}			0.6	V
Common-mode input voltage range, V_{ICR}‡			±2.5	V
Load resistance, GSX, R_L	10			kΩ
Load capacitance, GSX, C_L			50	pF
Operating free-air temperature, T_A	0		70	°C

‡ Measured with CMRR > 60 dB.

NOTE 2: To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

supply current

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Power down	No load		0.5	3	mA
		Active			6	11	
I_{BB}	Supply current from V_{BB}	Power down	No load		0.5	3	mA
		Active			6	11	

electrical characteristics at V_{CC} = 5 V ±5%, V_{BB} = –5 V ±5%, GND at 0 V, T_A = 25°C (unless otherwise noted)

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	DX	I_H = –3.2 mA	2.4		V
V_{OL}	Low-level output voltage	DX	I_L = 3.2 mA		0.4	V
		$\overline{TSX}$	I_L = 3.2 mA, Drain open		0.4	
I_{IH}	High-level input current		$V_I = V_{IH}$ to V_{CC}		±15	µA
I_{IL}	Low-level input current	All digital inputs	V_I = GND to V_{IL}		±15	µA
V_{OL}	Output current in high-impedance state	DX	V_O = GND to V_{CC}		±15	µA

analog interface with transmit amplifier input

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	VFXI+ or VFXI–	V_I = –2.5 V to 2.5 V			±200	nA
r_i	Input resistance	VFXI+ or VFXI–	V_I = –2.5 V to 2.5 V	10			MΩ
r_o	Output resistance		Closed loop		1	3	Ω
	Output dynamic range	GSX	$R_L \geq 10$ kΩ			±2.8	V
A_V	Open-loop voltage amplification	VFXI+ to GSX		5000			
B_I	Unity-gain bandwidth	GSX		1	2		MHz
V_{IO}	Input offset voltage	VFXI+ or VFXI–				±20	mV
CMRR	Common-mode rejection ratio			60			dB
K_{SVR}	Supply-voltage rejection ratio			60			dB

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.

analog interface with receive filter

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output resistance	VFRO			1	3	Ω
Load resistance		VFRO = ±2.5 V	600			Ω
Load capacitance	VFRO to GND				500	pF
Output dc offset voltage	VFRO to GND				±200	mV

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.

operating characteristics, V_{CC} = 5 V ±5%, V_{BB} = –5 V ±5%, GND at 0 V, V_I = 1.2276 V, f = 1.02 kHz, T_A = 0°C to 70°C, transmit input amplifier connected for unity gain, noninverting (unless otherwise noted)

timing requirements

			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$f_{clock(M)}$	Frequency of master clock (see Table 1)	MCLKX and MCLKR	Depends on BCLKX/CLKSEL		1.536 1.544 2.048		MHz
$f_{clock(B)}$	Frequency of bit clock, transmit	BCLKX		64		2.048	kHz
t_{w1}	Pulse duration, MCLKX and MCLKR high			160			ns
t_{w2}	Pulse duration, MCLKX and MCLKR low			160			ns
t_{r1}	Rise time of master clock	MCLKX and MCLKR	Measured from 20% to 80%			50	ns
t_{f1}	Fall time of master clock	MCLKX and MCLKR				50	ns
t_{r2}	Rise time of bit clock, transmit	BCLKX	Measured from 20% to 80%			50	ns
t_{f2}	Fall time of bit clock, transmit	BCLKX				50	ns
t_{su1}	Setup time, BCLKX high (and FSX in long-frame sync mode) before MCLKX↓		First bit clock after the leading edge of FSX	100			ns
t_{w3}	Pulse duration, BCLKX and BCLKR high		V_{IH} = 2.2 V	160			ns
t_{w4}	Pulse duration, BCLKX and BCLKR low		V_{IL} = 0.6 V	160			ns
t_{h1}	Hold time, frame sync low after bit clock low (long frame only)			0			ns
t_{h2}	Hold time, BCLKX high after frame sync↑ (short frame only)			0			ns
t_{su2}	Setup time, frame sync high before bit clock↓ (long frame only)			80			ns
t_{d1}	Delay time, BCLKX high to data valid		Load = 150 pF plus 2 LSTTL loads‡	0		140	ns
t_{d2}	Delay time, BCLKX high to $\overline{TSX}$ low		Load = 150 pF plus 2 LSTTL loads‡			140	ns
t_{d3}	Delay time, BCLKX (or 8 clock FSX in long frame only) low to data output disabled			50		165	ns
t_{d4}	Delay time, FSX or BCLKX high to data valid (long frame only)		C_L = 0 pF to 150 pF	20		165	ns
t_{su3}	Setup time, DR valid before BCLKR↓			50			ns
t_{h3}	Hold time, DR valid after BCLKR or BCLKX↓			50			ns
t_{su4}	Setup time, FSR or FSX high before BCLKR or BCLKR↓		Short-frame sync pulse (1 or 2 bit clock periods long) (see Note 3)	50			ns
t_{h4}	Hold time, FSX or FSR high after BCLKX or BCLKR↓		Short-frame sync pulse (1 or 2 bit clock periods long) (see Note 3)	100			ns
t_{h5}	Hold time, frame sync high after bit clock↓		Long-frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
t_{w5}	Minimum pulse duration of the frame sync pulse (low level)		64-kbps operating mode	160			ns

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.
‡ Nominal input value for an LSTTL load is 18 kΩ.
NOTE 3: For short-frame sync timing, FSR and FSX must go high while their respective bit clocks are high.

filter gains and tracking errors

PARAMETER	TEST CONDITIONS‡	MIN	TYP†	MAX	UNIT
Maximum peak transmit overload level	3.17 dBm0		2.501		V
Transmit filter gain, absolute (at 0 dBm0)	T_A = 25°C	–1.5		1.5	dB
Transmit filter gain, relative to absolute	f = 16 Hz			–35	dB
	f = 50 Hz			–25	
	f = 60 Hz			–21	
	f = 200 Hz	–2		0.5	
	f = 300 Hz to 3000 Hz	–0.5		0.5	
	f = 3300 Hz	–0.55		0.5	
	f = 3400 Hz	–1.5		1.5	
	f = 4000 Hz			–10	
	f ≥ 4600 Hz (measure response from 0 Hz to 4000 Hz)			–25	
Absolute transmit gain variation with temperature and supply voltage	Relative to absolute transmit gain	–0.1		0.1	dB
Transmit gain tracking error with level	Sinusoidal test method, Reference level = –10 dBm0				dB
	3 dBm0 ≥ input level ≥ –40 dBm0			±0.4	
	–40 dBm0 > input level ≥ –50 dBm0			±0.8	
Receive filter gain, absolute (at 0 dBm0)	Input is digital code sequence for 0 dBm0 signal, T_A = 25°C	–1.5		1.5	dB
Receive filter gain, relative to absolute	f = 0 Hz to 3000 Hz, T_A = 25°C	–0.5		0.5	dB
	f = 3300 Hz	–0.55		0.5	
	f = 3400 Hz	–1.5		1.5	
	f = 4000 Hz			–10	
Absolute receive gain variation with temperature and supply voltage		–0.1		0.1	dB
Receive gain tracking error with level	Sinusoidal test method; reference input PCM code corresponds to an ideally encoded –10 dBm0 signal				dB
	3 dBm0 ≥ input level ≥ –40 dBm0			±0.4	
	–40 dBm0 > input level ≥ –50 dBm0			±0.8	
Receive output drive voltage	R_L = 10 kΩ			±2.5	V

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.
‡ Absolute rms signal levels are defined as follows: V_I = 1.2276 V = 0 dBm0 = 4 dBm at f = 1.02 kHz with R_L = 600 Ω.

envelope delay distortion with frequency

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit delay, absolute (at 0 dBm0)	f = 1600 Hz		290	315	µs
Transmit delay, relative to absolute	f = 500 Hz to 600 Hz		195	220	µs
	f = 600 Hz to 800 Hz		120	145	
	f = 800 Hz to 1000 Hz		50	75	
	f = 1000 Hz to 1600 Hz		20	40	
	f = 1600 Hz to 2600 Hz		55	75	
	f = 2600 Hz to 2800 Hz		80	105	
	f = 2800 Hz to 3000 Hz		130	155	
Receive delay, absolute (at 0 dBm0)	f = 1600 Hz		180	200	µs
Receive delay, relative to absolute	f = 500 Hz to 1000 Hz	–40	–25		µs
	f = 1000 Hz to 1600 Hz	–30	–20		
	f = 1600 Hz to 2600 Hz		70	90	
	f = 2600 Hz to 2800 Hz		100	125	
	f = 2800 Hz to 3000 Hz		140	175	

noise

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise, C-message weighted	VFXI = 0 V		5	19	dBrnC0
Receive noise, C-message weighted	PCM code equals alternating positive and negative zero		2	10	dBrnC0
Noise, single frequency	VFXI+ = 0 V, f = 0 kHz to 100 kHz, Loop-around measurement			–53	dBm0

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.

power-supply rejection

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Positive power-supply rejection, transmit	V_{CC} = 5 V + 100 mVrms, f = 0 kHz to 50 kHz	VFXI+ = –50 dBm0,	25		dBC‡
Negative power-supply rejection, transmit	V_{BB} = 5 V + 100 mVrms, f = 0 kHz to 50 kHz	VFXI+ = –50 dBm0,	25		dBC‡
Positive power-supply rejection, receive	PCM code equals positive zero, V_{CC} = 5 V + 100 mVrms	f = 0 Hz to 50 kHz	25		dBC‡
Negative supply-voltage rejection, receive	PCM code equals positive zero, V_{BB} = –5 V + 100 mVrms	f = 0 Hz to 50 kHz	25		dBC‡
Spurious out-of-band signals at the channel output (VFRO)	0 dBm0, 300-Hz to 3400-Hz input applied to DR (measure individual image signals at VFRO)			–25	dB
	f = 4600 Hz to 7600 Hz			–28	dB
	f = 7600 Hz to 100 Hz			–35	

‡ The unit dBC applies to C-message weighting.

distortion

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Signal-to-distortion ratio, transmit or receive half-channel‡	Level = 3 dBm0		28		dBC†
	Level = 0 dBm0 to –30 dBm0		30		
	Level = –40 dBm0	Transmit	25		
		Receive	25		
Single-frequency distortion products, transmit				–41	dB
Single-frequency distortion products, receive				–41	dB
Intermodulation distortion	Loop-around measurement, VFXI+ = –4 dBm0 to –21 dBm0, Two frequencies in the range of 300 Hz to 3400 Hz			–35	dB

† The unit dBC applies to C-message weighting.
‡ Sinusoidal test method. The TCM320A54 is measured using a C-message weighted filter.

crosstalk

PARAMETER	TEST CONDITIONS		MIN	TYP§	MAX	UNIT
Crosstalk, transmit-to-receive	f = 300 Hz to 3000 Hz,	DR at steady PCM code		–90	–75	dB
Crosstalk, receive-to-transmit (see Note 4)	VFXI = 0 V,	f = 300 Hz to 3000 Hz		–90	–75	dB

§ All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.
NOTE 4: Receive-to-transmit crosstalk is measured with a – 50-dBm0 activation signal applied at VFXI+.

PARAMETER MEASUREMENT INFORMATION

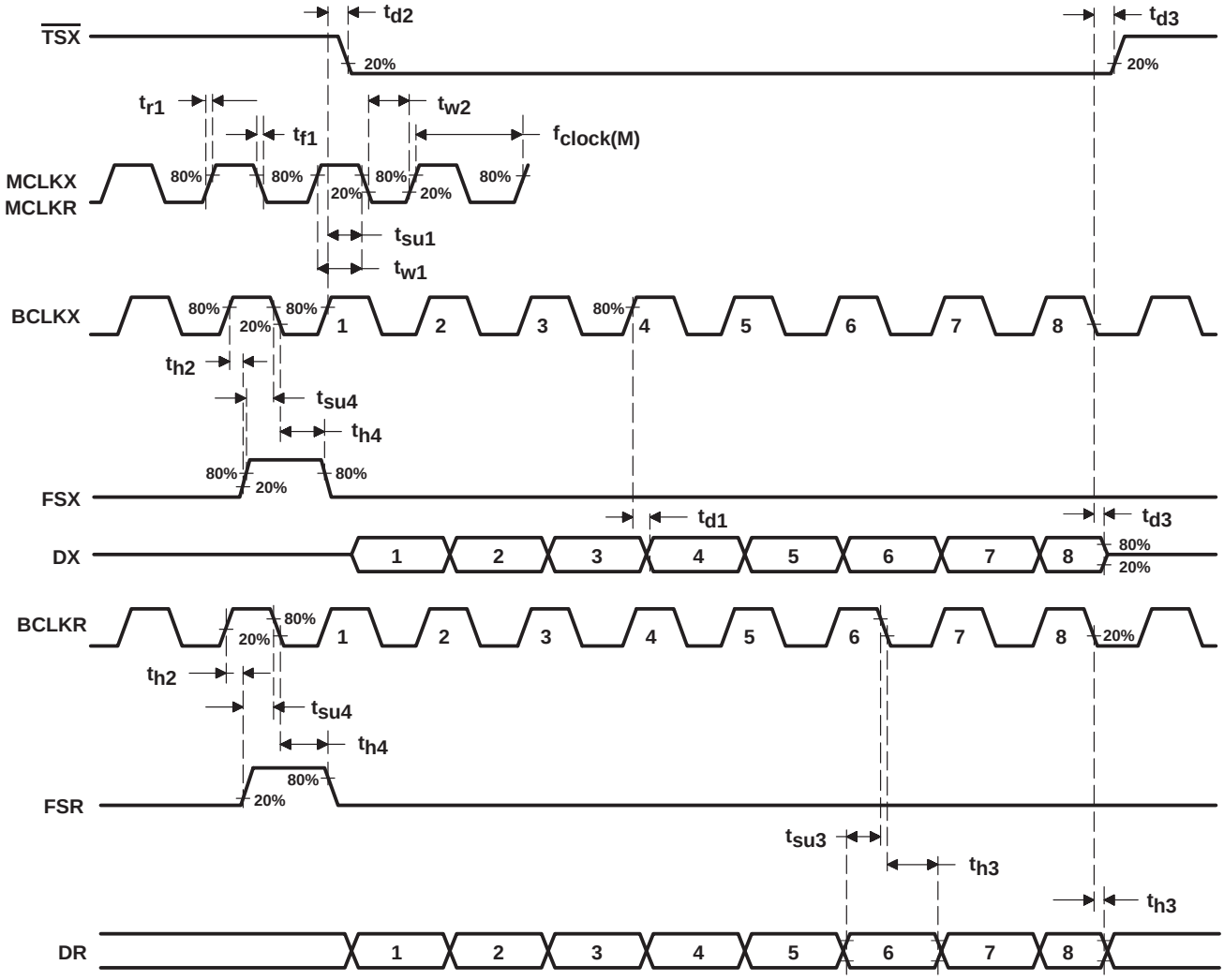


Figure 1. Short-Frame Sync Timing

PARAMETER MEASUREMENT INFORMATION

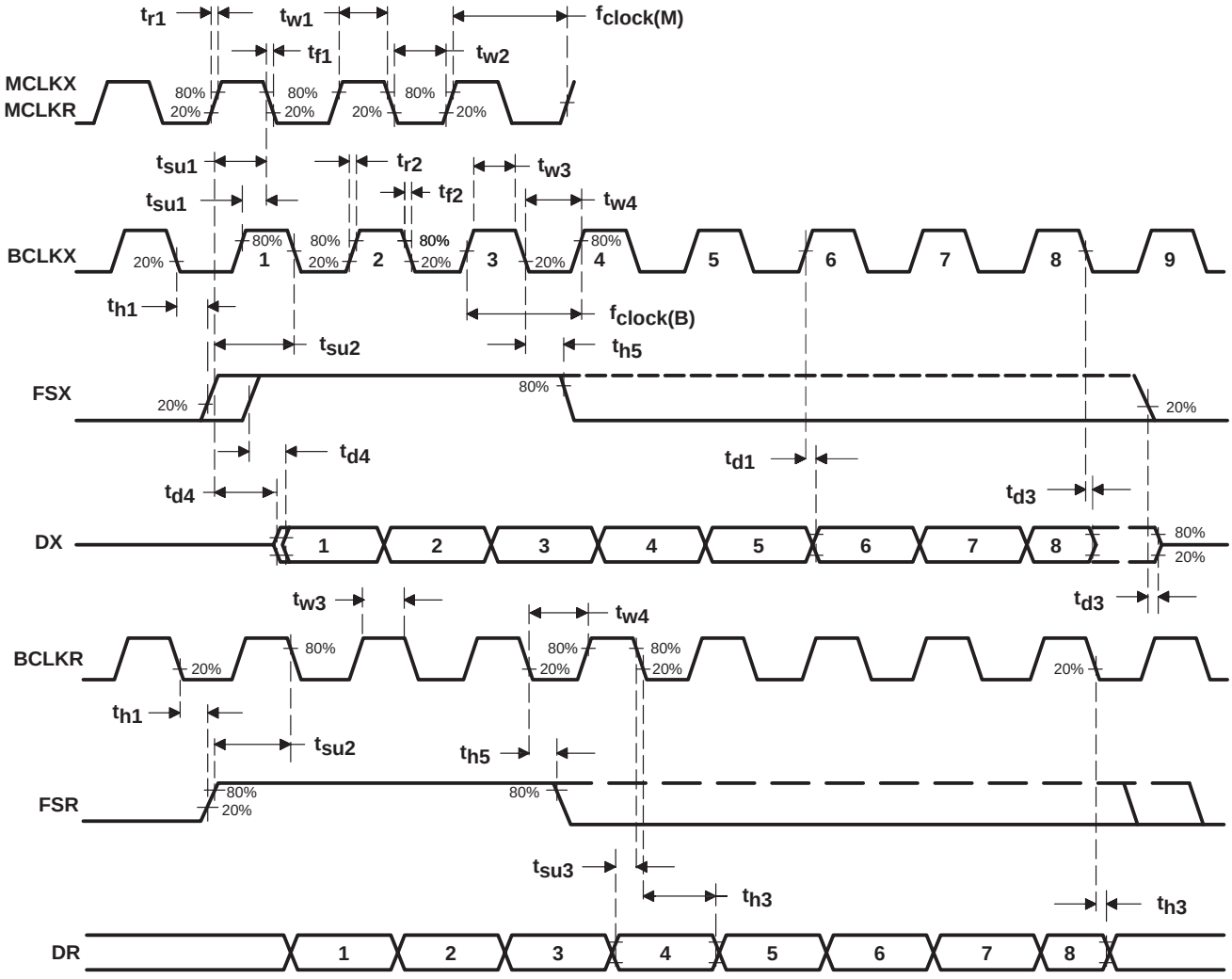


Figure 2. Long-Frame Sync Timing

PRINCIPLES OF OPERATION

system reliability and design considerations

TCM320AC54 system reliability and design considerations are described in the following paragraphs.

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TCM320AC54 is heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V – 1N5711 or equivalent) between the power supply and GND (see Figure 3). If it is possible that a TCM320AC54-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power down condition.
8. Apply FS synchronization pulses.
9. Apply the signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

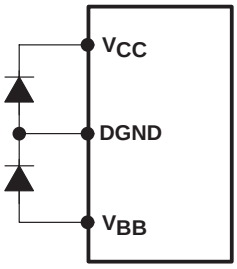


Figure 3. Latch-Up Protection Diode Connection

internal sequencing

Power-on reset circuitry initializes the TCM320AC54 when power is first applied, placing it into the power-down mode. DX and VFRO outputs go into high-impedance states and all nonessential circuitry is disabled. A low level or clock applied to MCLKR/PDN powers up the device and activates all circuits. DX, a 3-state PCM data output, remains in the high-impedance state until the arrival of the second FSX pulse.

synchronous operation

For synchronous operation, a clock is applied to MCLKX. MCLKR/PDN is used as a power-down control. A low level on MCLKR/PDN powers up the device and a high level powers it down. In either case, MCLKX is selected as the master clock for both receive and transmit direction. BCLKX must also have a bit clock applied to it. The selection of the proper internal divider for a master-clock frequency of 1.536 MHz, 1.544 MHz, or 2.048 MHz can be done via BCLKR/CLKSEL. The device automatically compensates for the 193rd clock pulse of each frame.

A fixed level on BCLKR/CLKSEL selects BCLKX as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation that can be selected depending on the state of BCLKR/CLKSEL. In the synchronous mode, BCLKX can be in the range from 64 kHz to 2.048 MHz but must be synchronous with MCLKX.

Table 1. Selection of Master-Clock Frequencies

BCLKR/CLKSEL	MASTER-CLOCK FREQUENCY SELECTED
Clock input	1.536 MHz or 1.544 MHz
Logic input L (sync mode only)	2.048 MHz
Logic input H (open) (sync mode only)	1.536 MHz or 1.544 MHz

The encoding cycle begins with each FSX pulse, and the PCM data from the previous cycle is shifted out of the enabled DX output on the rising edge of BCLKX. After eight bit-clock periods, the 3-state DX output is returned to the high-impedance state. With an FSR pulse, PCM data is latched via DR on the falling edge of BCLKX (or BCLKR, if running). FSX and FSR must be synchronous with MCLKX and MCLKR.

PRINCIPLES OF OPERATION

asynchronous operation

For asynchronous operation, separate transmit and receive clocks can be applied. MCLKX and MCLKR must be 1.536 MHz or 1.544 MHz and need not be synchronous. For best performance, however, MCLKR should be synchronous with MCLKX. This is easily achieved by applying only static logic levels to MCLKR/PDN. This connects MCLKX to all internal MCLKR functions. For 1.544-MHz operation, the device compensates for the 193rd clock pulse of each frame. Each encoding cycle is started with FSX and FSX must be synchronous with MCLKX and BCLKX. Each decoding cycle is started with FSR and FSR must be synchronous with BCLKR. The logic levels shown in Table 1 are not valid in the asynchronous mode. BCLKX and BCLKR can operate from 64 kHz to 2.048 MHz.

short-frame sync operation

The device can operate with either a short- or a long-frame sync pulse. On power up, the device automatically goes into the short-frame mode where both FSX and FSR must be one bit-clock period long with timing relationships specified in Figure 1. With FSX high during a falling edge of BCLKX, the next rising edge of BCLKX enables the 3-state output buffer, DX, which outputs the sign bit. The remaining seven bits are clocked out on the following seven rising edges and the next falling edge disables DX. With FSR high during a falling edge of BCLKR (BCLKX in synchronous mode), the next falling edge of BCLKR latches in the sign bit. The following seven falling edges latch in the seven remaining bits. The short-frame sync pulse can be utilized in either the synchronous or asynchronous mode.

long-frame sync operation

Both FSX and FSR must be three or more bit-clock periods long to use the long-frame sync mode with timing relationships as shown in Figure 2. Using the transmit frame sync (FSX), the device detects whether a short- or long-frame sync pulse is being used. For 64-kHz operation, the frame-sync pulse must be kept low for a minimum of 160 ns. The rising edge of FSX or BCLKX, whichever occurs later, enables the DX 3-state output buffer. The first bit clocked out is the sign bit. The next seven rising edges of BCLKX edges clock out the remaining seven bits. The falling edge of BCLKX following the eighth rising edge or FSX going low, whichever occurs later, disables DX. A rising edge on FSR, the receive-frame sync pulse, causes the PCM data at DR to be latched in on the next eight falling edges of BCLKR (BCLKX in synchronous mode). The long-frame sync pulse can be utilized in either the synchronous or asynchronous mode.

transmit section

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. The low-noise and wide-bandwidth characteristics of this device provide gain in excess of 20 dB across the audio passband. The operational amplifier drives a unity-gain filter consisting of an RC active prefilter followed by an eighth-order switched-capacitor band-pass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. As per μ-law coding conventions, the ADC is a companding type. A precision voltage reference provides a nominal input overload of 2.5 V peak. The sampling of the filter output is controlled by the FSX frame-sync pulse. Then, the successive-approximation encoding cycle begins. The 8-bit code is loaded into a buffer and shifted out through DX at the next FSX pulse. The total encoding delay is approximately 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign-bit integration.

PRINCIPLES OF OPERATION

receive section

The receive section consists of an expanding DAC that drives a fifth-order low-pass filter clocked at 256 kHz. The decoder and the fifth-order low-pass filter corrects for the (sin x)/x attenuation caused by the 8-kHz sample-and-hold circuit. The filter is followed by a second-order RC active post-filter/power amplifier capable of driving a 600-Ω load to a level of 7.2 dBm. The receive section is unity gain. At FSR, the data at DR is clocked in on the falling edge of the next eight BCLKR (BCLKX) periods. At the end of the decoder time slot, the decoding cycle begins and 10 μs later, the decoder DAC output is updated. The decoder delay is about 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), or a total of approximately 180 μs.

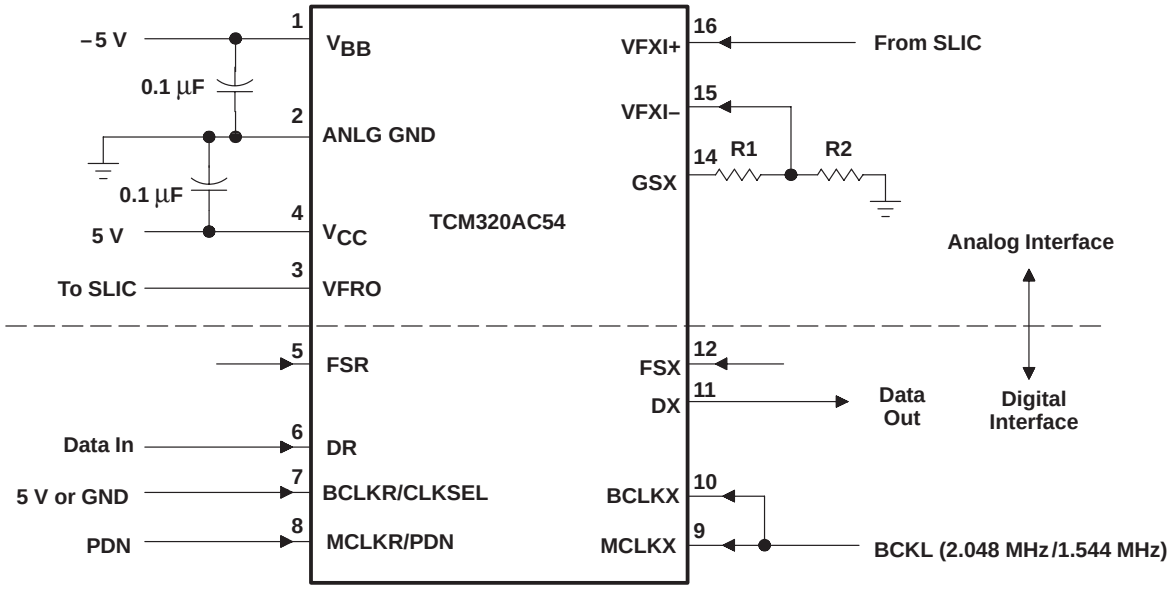
APPLICATION INFORMATION

power supplies

While the terminals of the TCM320AC54 are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications in which the printed-circuit board can be plugged into a hot socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to ANLG GND. This minimizes the interaction of ground return currents flowing through a common bus impedance. V_{CC} and V_{BB} supplies should be decoupled by connecting 0.1-μF decoupling capacitors to this common point. These bypass capacitors must be connected as close as possible to V_{CC} and V_{BB}.

For best performance, the ground point of each codec/filter on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10-μF capacitors.



NOTE A: Transmit gain = 20 log $\left(\frac{R1 + R2}{R2}\right)$, $(R1 + R2) \geq 10\ k\Omega$

Figure 4. Typical Synchronous Application

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