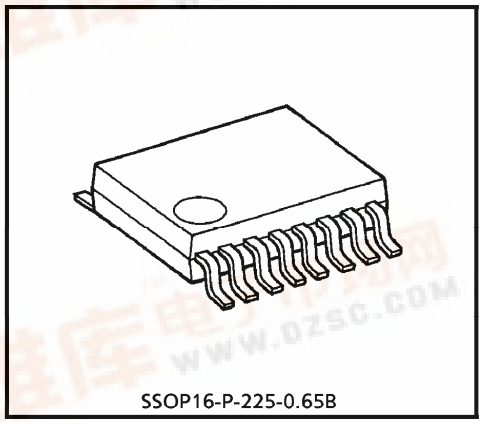
TENTATIVE TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD7623AFN

3-WIRE AND I^2C BUS SYSTEM, 2.3 GHz DIRECT TWO MODULUS-TYPE FREQUENCY SYNTHESIZER FOR CATV

The TD7623AFN can be combined with a micro CPU to create a highly functional frequency synthesizer. The control data conforms to 3-wire bus and standard I^2C bus formats. BUS-SW can be used to easily switch for easy tuner system set-up.



SSOP16-P-225-0.65B

Weight : 0.07 g (Typ.)

FEATURES

- Direct two modulus-type frequency synthesizer
- Standard I^2C bus format control with built-in read mode
- 3-wire bus 27-bit format control
- 4-bit bandswitch drive transistor
- 5-level A / D converter (when I^2C bus selected)
- Frequency step : 50 kHz, 62.5 kHz, 250 kHz, and 333.3 kHz (at 4 MHz X'tal used)
- Phase lock detector
- Various function settings via program data
- Four address settings via address selector (when I^2C bus selected)
- Power on reset circuit
- Flat, compact package : SSOP16 (0.65 mm pitch)
- Power on reset operation condition

  Bandswitch register 1 to 4 : OFF

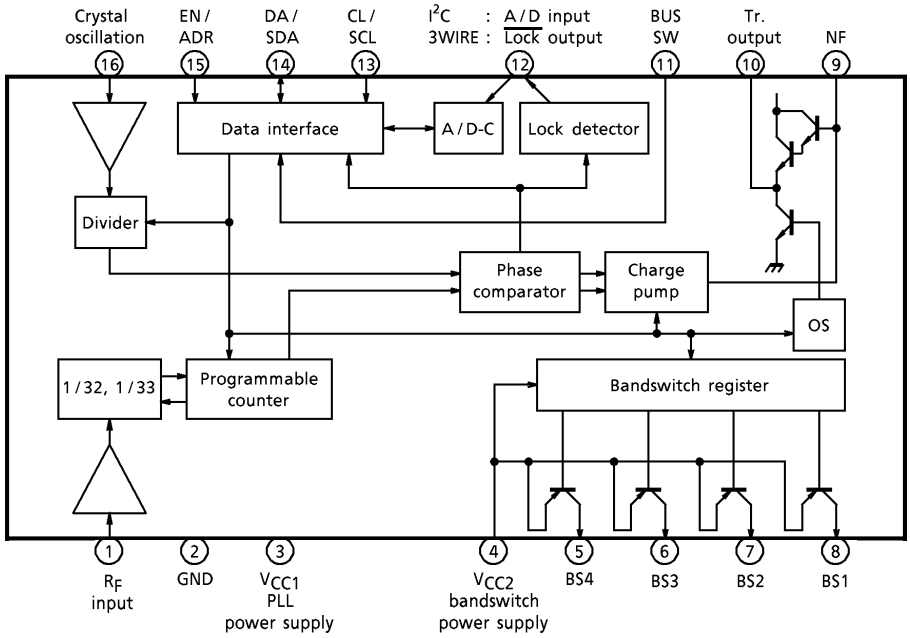
  Tuning amplifier : ON

  Charge-pump output current : ±200 μA

  Phase comparator reference frequency divider ratio : 1 / 80

(Note) These devices are easy to be damaged by high static voltage or electric fields. In regards to this, please handle with care.

BLOCK DIAGRAM



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage 1	V_{CC1}	6.0	V
Supply Voltage 2	V_{CC2}	12	V
Power Consumption	P_D	560	mW
Operating Temperature	T_{opr}	−20~85	°C
Storage Temperature	T_{stg}	−55~150	°C

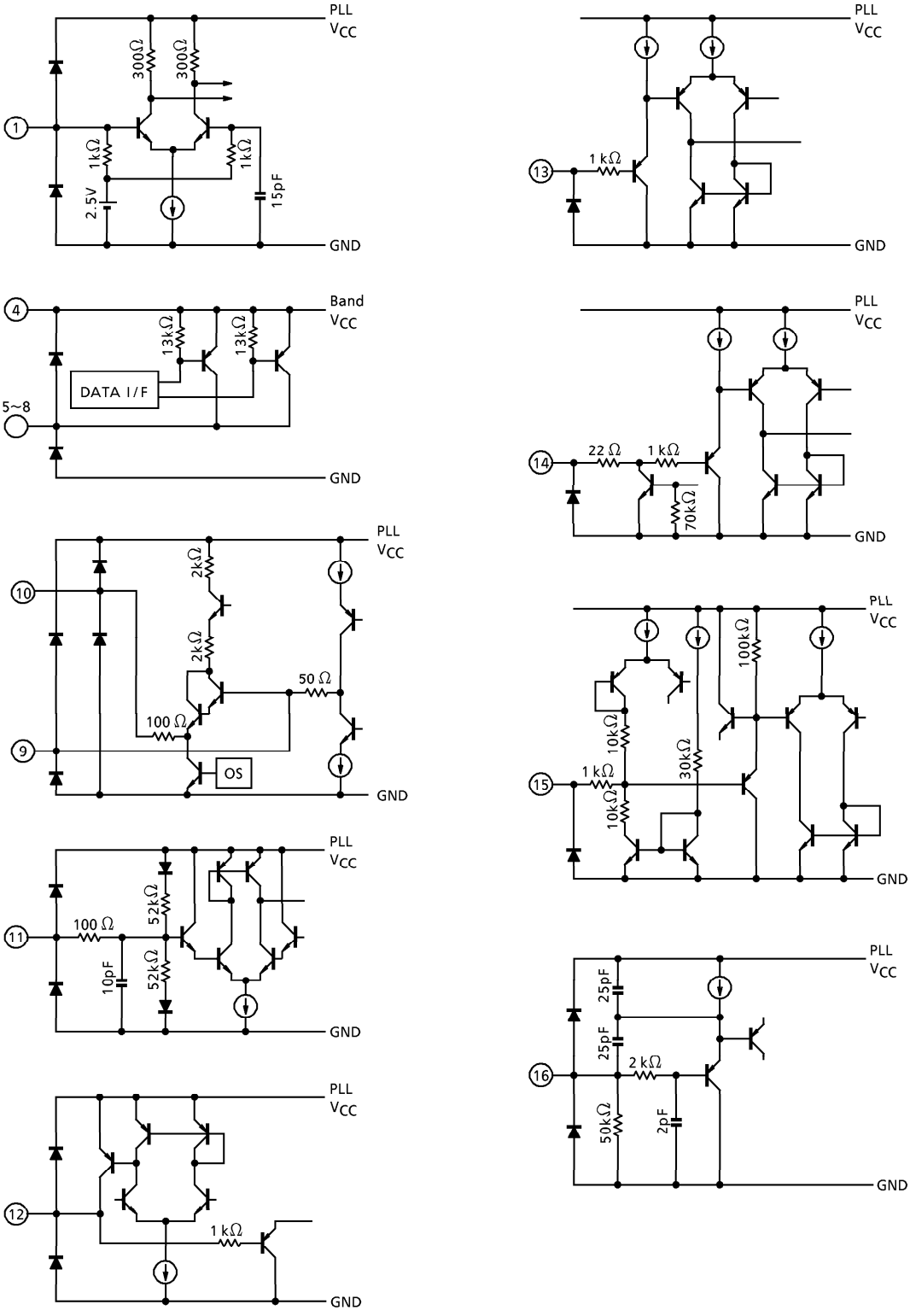
(Note 1) When using the device at above Ta = 25°C, decrease the power dissipation by 4.5 mW for each increase of 1°C.

(Note 2) These devices are easy to be damaged by high static voltage or electric fields. In regards to this, please handle with care.

RECOMMENDED SUPPLY VOLTAGE

PIN No.	PIN NAME	MIN	TYP.	MAX	UNIT
3	V_{CC1} : PLL Power Supply	4.5	5.0	5.5	V
4	V_{CC2} : Band Switch Power Supply	V_{CC1}	—	9.9	V

PIN INTERFACE



ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC1} = 5 V, V_{CC2} = 9 V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage 1	V_{CC1}	—	—	4.5	5.0	5.5	V
Supply Current 1	I_{CC1}	1	Bandswitch : OFF V_t : OFF	24	32	40	mA
Supply Voltage 2	V_{CC2}	—	—	V_{CC1}	—	9.9	V
Supply Current 2	I_{CC2}-1	1	Bandswitch : 1 Band ON I_{BD} = 20 mA (LOAD)	—	24	26	mA
	I_{CC2}-2		Bandswitch : 2 Band ON I_{BD} = 30 mA (TOTAL LOAD)	—	38	42	
Bandswitch Drive Current	I_{BD}	3	Maximum Drive Current / 1 port	—	—	20	mA
Bandswitch Drive Maximum LOAD	I_{BDMAX}	3	Maximum Total Drive Current	—	—	40	mA
Bandswitch Drive Voltage Drop	V_{BD} Sat	3	I_{BD} = 20 mA	—	0.2	0.4	V
X'tal Operating Range	$OSCf_{in}$	—	—	3.2	—	4.5	MHz
X'tal Negative Resistance	OSC_R	1	—	1.0	1.5	—	kΩ
X'tal External Input Level	OSC_{in}	—	3.2 MHz~4.5 MHz, Rx = 91 kΩ	250	—	1000	mV_{p-p}
Ratio Setting Range	N	—	15-bit counter	1024	—	32767	Ratio
Prescaler Input Sensitivity	V_{inRF}	2	f = 500~2300 MHz	− 15	—	+ 5	dBmW
Lock Output Low Voltage	V_{LkL}	1	(lock mode, 3-wire bus mode)	—	—	0.4	V
Lock Output High Voltage	V_{LkH}	1	(unlock mode, 3-wire bus mode)	4.6	—	—	V
Logic Input Low Voltage	V_{BsL}	1	Pins 13 to 15	− 0.3	—	1.5	V
Logic Input High Voltage	V_{BsH}	1	Pins 13 to 15	2.5	—	V_{CC1} + 0.3	V
Logic Input Current (low)	I_{BsL}	1	Pins 13 to 15	− 20	—	10	μA
Logic Input Current (high)	I_{BsH}	1	Pins 13 to 15	− 10	—	20	
BUS-SW Low Input Voltage	V_{BIL}	1	—	0.0	—	0.8	V
BUS-SW High Input Voltage	V_{BIH}	1	—	4.2	—	V_{CC1}	
BUS-SW Low Current (low)	I_{BIL}	1	—	− 200	—	—	μA
BUS-SW Low Current (high)	I_{BIH}	1	—	—	—	200	
Charge Pump Output Current	I_{chg}	2	CP = 〖 0 〗	± 150	± 200	± 300	μA
			CP = 〖 1 〗	± 600	± 800	± 1200	
ACK Output Voltage	V_{ACK}	1	I_{SINK} = 3 mA (I^2C-bus mode)	—	—	0.4	V

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Set-up Time	T_S	—	(3-wire bus mode) Refer to data timing chart	2	—	—	μs
Enable Hold Time	T_{sL}			2	—	—	
Next Enable Stop Time	T_{NE}			6	—	—	
Next Clock Stop Time	T_{NC}			6	—	—	
Clock Width	T_C			2	—	—	
Enable Set-up Time	T_L			10	—	—	
Data Hold Time	T_H			2	—	—	
SCL Clock Frequency	f_{SCL}		(I^2C bus mode) Refer to data timing chart	0	—	100	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}			4.7	—	—	μs
Hold Time (Repeated) START Condition	$t_{HD;STA}$			4.0	—	—	
Low Period of the SCL Clock	t_{LOW}			4.7	—	—	
High Period of the SCL Clock	t_{HIGH}			4.0	—	—	
Set-up Time for a Repeated START Condition	$t_{SU;STA}$			4.7	—	—	
Data Hold Time	$t_{HD;DAT}$			0	—	—	
Data Set-up Time	$t_{SU;DAT}$			250	—	—	ns
Rise Time of both SDA and SCL Signals	t_R			—	—	1000	
Fall Time of both SDA and SCL Signals	t_F			—	—	300	
Set-up Time for STOP Condition	$t_{SU;STO}$			4.0	—	—	μs

Fig.1 3-wire bus data timing chart (Falling edge timing)

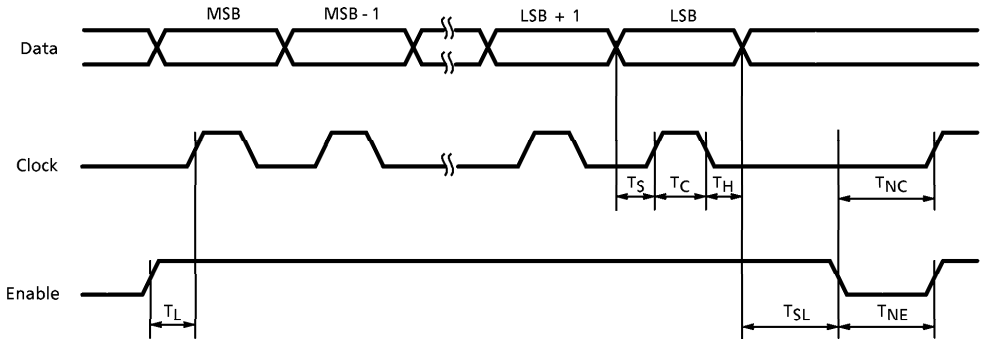
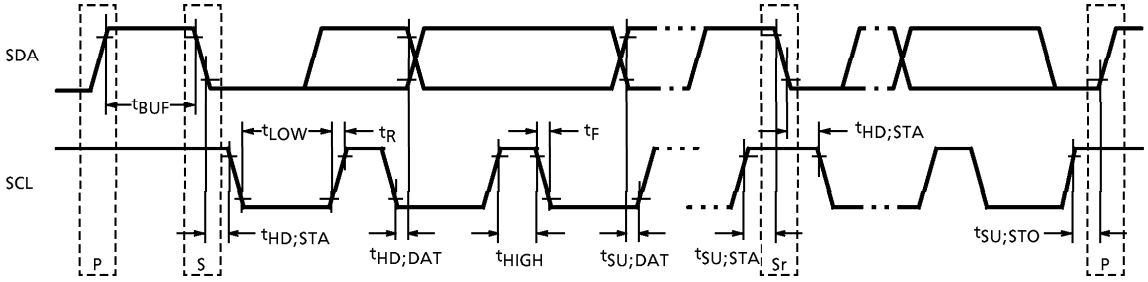


Fig.2 I²C bus data timing chart (Falling edge timing)



OPERATION INSTRUCTIONS

The TD7623AFN can be controlled with either the 3-wire bus or standard I^2C bus.
The 3-wire bus mode, the device is controlled by 27-bit serial data.
The I^2C bus conforms to the standard I^2C bus format. The bus supports two-way bus communications control, consisting of WRITE mode where data are received and READ mode where data are transmitted. In READ mode, the voltage applied on the A / D converter input pin can be transmitted and output with 5-level resolution.
(This function is only valid when the I^2C bus is selected. When the 3-wire bus is selected, the A / D converter input pin function as the $\overline{LOCK}$ output pin.)
Addresses can be set using the hardware bits. Three programmable addresses are supported. 3-wire bus and standard I^2C bus are switches by the voltage applied on the BUS-SW pin.
When the supply voltage (V_{CC1}) is applied, the power-on reset circuit operates. Before data are input, counter data are all initialized to 『 0 』 : band switches are all initialized to off.

FUNCTION CHART

NAME	3-WIRE BUS MODE	I^2C BUS MODE
BUS-SW	「 V_{CC} 」	「 GND 」
CL / SCL	CLOCK INPUT	SCL INPUT
DA / SDA	DATA INPUT	SDA IN / OUTPUT
EN / ADR	ENABLE INPUT	ADDRESS
$\overline{LOCK}$ / ADC	$\overline{LOCK}$	ADC

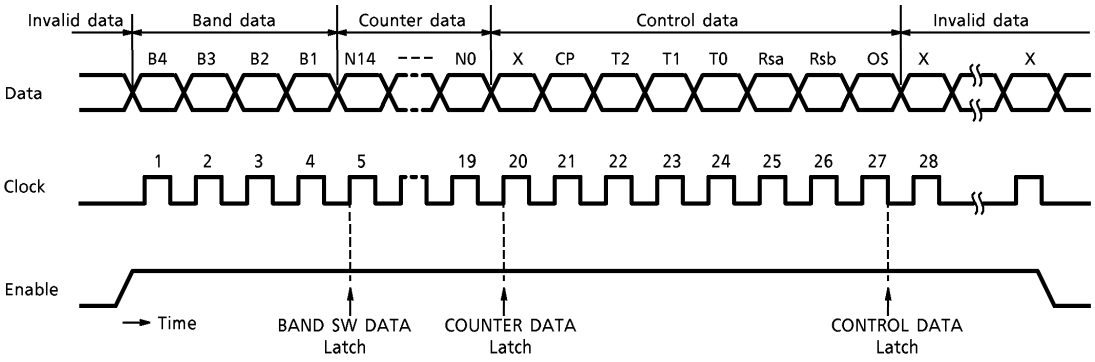
— 3-WIRE BUS COMMUNICATIONS CONTROL —

The 3-wire bus mode, the device is controlled by 27-bit serial data.
The 3-wire bus sets the following data : (bandswitch information and programmable counter information, charge-pump current setting, reference frequency divider ratio setting, and testing item functions.)
The program frequency can be calculated in the following formula :

$$fosc = f_r \times N$$

fosc : Program frequency
f_r : Phase comparator reference frequency (Step frequency)
N : Counter total ratio

Figure 3. 3-wire bus data format



- 27-bit DATA TRANSMISSION

  During a high level of the enable signal, the data is clocked into the register on the falling edge of the clock.
  The clock number during a high level of the enable signal must be set to 27-bit or more of clock and data transmission.
  The data are latched at the 27th falling edge of the clock signal, validating the previous 27-bit data.
  The 4-bit bandswitch data are latched at the 5th bit rising edge of the clock signal, and the data is updated.
  The programmable counter data are latched at the 20th bit rising edge of the clock signal, and the data is updated.
  The control data are latched at the 27th bit falling edge of the clock signal, and the data is updated.
  Details of the data timing, see the data timing chart. (Figure 1)

TEST DATA SPECIFICATIONS

- B4~B1 : Band drive data
  『0』: OFF
  『1』: ON
- N14~N0 : Programmable divider data
- CP : Charge pump output current
  『0』: ±200 μA (Typ.)
  『1』: ±800 μA (Typ.)
- T2, T1, T0 : Test mode setting bits

CHARACTERISTIC	T2	T1	T0	NOTE
Normal operation	0	0	1	—
Reference signal output	1	0	0	Reference signal output : B4, Counter output : B2
1/2 counter divider output	1	0	1	Reference signal output : B4, 1/2 counter output : B2
Phase comparator test	0	0	0	Comparative signal input : DA Reference signal input : CL (check output : NF)

X : Don't care

(Note) When testing the counter divider output, programmable counter data input is necessary.

- Rsa, Rsb : X'tal Reference frequency divider ratio select bits

RSa	RSb	DIVIDER RATIO	STEP FREQUENCY	TUNING FREQUENCY
0	0	1/12	333.3 k	500 MHz~2300 MHz
0	1	1/16	250.0 k	500 MHz~2300 MHz
1	0	1/64	62.5 k	500 MHz~2000 MHz
1	1	1/80	50.0 k	500 MHz~1600 MHz

- OS : Tuning amplifier control bit
  『0』: Tuning amp ON (Normal operation)
  『1』: Tuning amp OFF (Tr. Output is Low Level)
- X : Don't care

— I^2C BUS COMMUNICATIONS CONTROL—

The TD7623AFN conform to standard I^2C bus format.
The I^2C bus mode enables two-way bus communications with the WRITE mode, which receives data, and READ mode, which status data.
WRITE and READ mode are set using the last bit (R / W bit) of the address byte.
If the last address bit is set to 『 0 』, WRITE mode is set ; if set to 『 1 』 READ mode is set.
Address can be set using the hardware bits. Three programmable address can be programmed.
With this setting, multiple frequency synthesizers can be used in the same I^2C bus line.
The address for the hardware bit setting can be selected by applying voltage to the address setting pin (ADR : Pin 15). An address is selected according to the set bits.
When the correct address byte is received, during acknowledgment, serial data (SDA) line is "Low".
If WRITE mode is set at this time, when the data byte is programmed, the serial data (SDA) line is "Low" during the next acknowledgment.

a) WRITE mode (setting command)

When WRITE mode is set, byte 1 segment the address data ; bytes 2 and 3 segment the frequency data ; byte 4 segment the divider ratio setting and function setting data ; and byte 5 segment the output port data.
Data are latched and transferred at the end of byte 3, byte 4 and byte 5.
Byte 2 and byte 3 are latched and transferred is done with a two byte set (byte 2 + byte 3).
Once a correct address is received and acknowledged, the data type is determined according to 『 0 』 or 『 1 』 set in the first bit of the next byte. That is, if the first bit is 『 0 』, the data are frequency data ; if 『 1 』, function setting or output port data.
Until the I^2C bus STOP CONDITION is detected, the additional data can be input without transmitting the address again. (Ex : Frequency sweep is possible with additional frequency data.)
If data transmission is aborted, data programmed before the abort are valid.
Byte 1 can set the hardware bit with address data.
The hardware bit is set with voltage applied to the address setting pin (ADR : Pin 15).
Bytes 2 and 3 are stored in the 15-bit shift register with counter data for the frequency setting, and control the 15-bit programmable counter ratio.
The program frequency can be calculated in the following formula :

$fosc = f_r \times N$

fosc : Program frequency
f_r : Phase comparato reference frequency (Step frequency)
N : Counter total ratio

f_r is calculated using the crystal oscillator frequency and the reference frequency divider ratio set in byte 4 (control byte). (f_r = X'tal oscillator frequency / reference frequency divider ratio)
The reference frequency divider ratio can be set to 1 / 12, 1 / 16, 1 / 64 and 1 / 80.
When using a 4 MHz crystal oscillator, f_r = 333.33 kHz, 250 kHz, 62.5 kHz and 50 kHz.

The step frequency are 333.33 kHz, 250 kHz, 62.5 kHz and 50 kHz.
Byte 4 is a control byte used to set function. Bit 2 (CP) controls the output current of the charge-pump circuit. When bit 2 is set to 『 0 』 : the output current is set to ± 200 μA ; when set to 『 1 』 , ± 800 μA.
Bit 3 (T_2), bit 4 (T_1) and bit 5 (T_0) are used to set test mode. They are used to set the phase comparator reference signal output, and counter divider output.
For details of test mode, see the test mode setting table.
Bit 6 (RSa) and bit 7 (RSb) are used to set the X'tal reference frequency divider ratio.
For details of the X'tal reference frequency divider ratios, see the table for X'tal reference frequency divider ratios.
Bit 8 (OS) is used to set the charge-pump drive amplifier output setting. When bit 8 is set to 『 0 』 the output is ON (Normal Use) ; when set to 『 1 』 the output is OFF (Tr. Output is Low Level).
Byte 5 is used to set and control the output port (Bands 1~4).
When an output port set to 『 0 』 is OFF ; when set to 『 1 』 is ON.
Two output ports can be operation turned on, but be sure to keep the total output current under 40 mA.

b) READ mode (status request)

When READ mode is set, power-on reset operation status, phase comparator lock detector output status, and 5-level A / D converter pin input voltage status are output to the master device.
Bit 1 (POR) indicates the power-on reset operation status. When the power supply of V_{CC1} stops, bit 1 is set to 『 1 』 . The condition for reset to 『 0 』 , voltage supplied to V_{CC1} is 3 V or higher, transmission is requested in READ mode, and the status is output. (when V_{CC1} is turned on, bit 1 is also set to 『 1 』 .)
Bit 2 (FL) indicates the phase comparator lock status. When locked, 『 1 』 is output ; when unlocked, 『 0 』 is output.
But 6, 7 and 8 (A2, A1, A0) indicate the 5-level A / D converter status. The voltage applied to the A / D converter input pin (pin 12) is output through a 5-level resolution.
For the voltage applied on the A / D converter input pin, 5-level resolution, and the output bits, see the table.

DATA FORMAT

a) WRITE MODE

BYTE		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W=0	ACK
2	Divider Byte①	0	N14	N13	N12	N11	N10	N9	N8	ACK
3	Divider Byte②	N7	N6	N5	N4	N3	N2	N1	N0	ACKⓁ
4	Control Byte	1	CP	T2	T1	T0	RSa	RSb	OS	ACKⓁ
5	Band SW Byte	×	×	×	×	B4	B3	B2	B1	ACKⓁ

× : DON'T Care
ACK : Acknowledged
Ⓛ : Latch and transfer timing

b) READ MODE

BYTE		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W = 1	ACK
2	Status Byte	POR	FL	1	1	1	A2	A1	A0	—

ACK : Acknowledged

DATA SPECIFICATIONS

- MA1, MA0 : Programmable hardware address bits

ADDRESS PIN APPLIED VOLTAGE	MA1	MA0
$0 \sim 0.1\ V_{CC1}$	0	0
$0.4\ V_{CC1} \sim 0.6\ V_{CC1}$	1	0
$0 \sim V_{CC1}$	0	1
$0.9\ V_{CC1} \sim V_{CC1}$	1	1

- CP : Charge-pump output current setting

『0』 : ±200 μA (Typ.)
『1』 : ±800 μA (Typ.)

- T2, T1, T0 : Test mode setting

CHARACTERISTIC	T2	T1	T0	NOTE
Normal operation	0	0	1	—
Reference signal output	1	0	0	Reference signal output : B4, Counter output : B2
1/2 counter divider output	1	0	1	Reference signal output : B4, 1/2 counter output : B2
Phase comparator test	0	0	0	Comparative signal input : SDA Reference signal input : SCL (check output : NF)

X : Don't care

(Note) When testing the counter divider output, programmable counter data input is necessary.

- RSa, RSb : X'tal reference frequency divider ratio select bits

RSa	RSb	DIVIDER RATIO	STEP FREQUENCY	TUNING FREQUENCY
0	0	1/12	333.3 k	500 MHz~2300 MHz
0	1	1/16	250.0 k	500 MHz~2300 MHz
1	0	1/64	62.5 k	500 MHz~2000 MHz
1	1	1/80	50.0 k	500 MHz~1600 MHz

- OS : Tuning amplifier control setting
  『0』: Tuning amp ON (Normal operation)
  『1』: Tuning amp OFF (Tr. Output is Low Level)

- POR : Power-on reset flag
  『0』: Normal operation
  『1』: Reset operation

- FL : Lock detect flag
  『0』: Unlocked
  『1』: Locked

- A2, A1, A0 : 5-level A/D converter status.

ADC PIN APPLIED VOLTAGE	A2	A1	A0
0.60 V_{CC1}~V_{CC1}	1	0	0
0.45 V_{CC1}~0.60 V_{CC1}	0	1	1
0.30 V_{CC1}~0.45 V_{CC1}	0	1	0
0.15 V_{CC1}~0.30 V_{CC1}	0	0	1
0~0.15 V_{CC1}	0	0	0

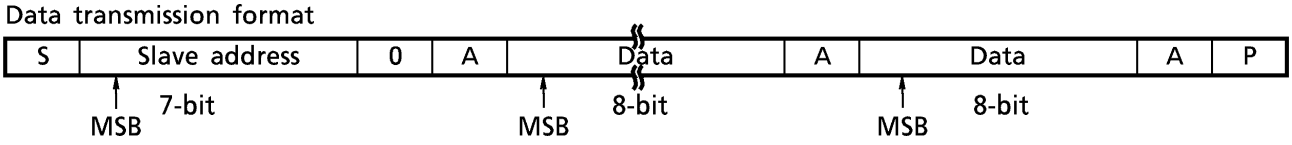
(*) Accuracy is $\pm 0.03 \times V_{CC1}$

- X : DON'T Care

I²C BUS CONTROL SUMMARY

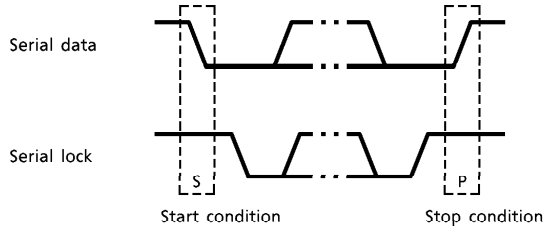
The bus control format of TD7623AFN conforms to the Philips I²C bus control format.

Data transmission format

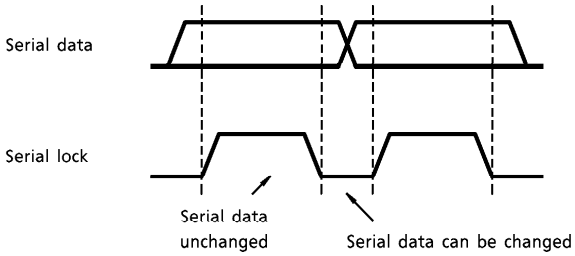


S : Start condition
P : Stop condition
A : Acknowledge

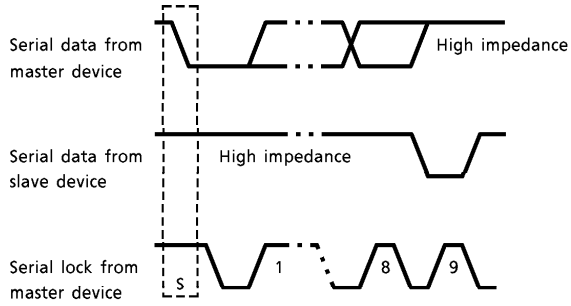
(1) Start / Stop condition



(2) Bit transfer



(3) Acknowledge

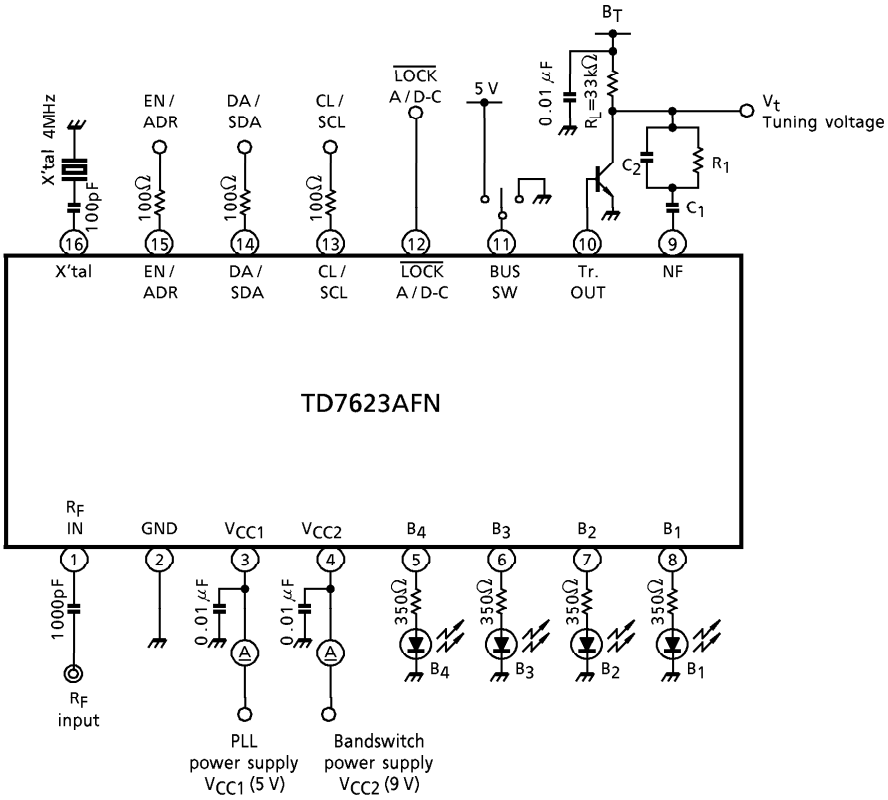


(4) Slave address

A_6	A_5	A_4	A_3	A_2	A_1	A_0	R / $\overline{W}$
1	1	0	0	0	*	*	0

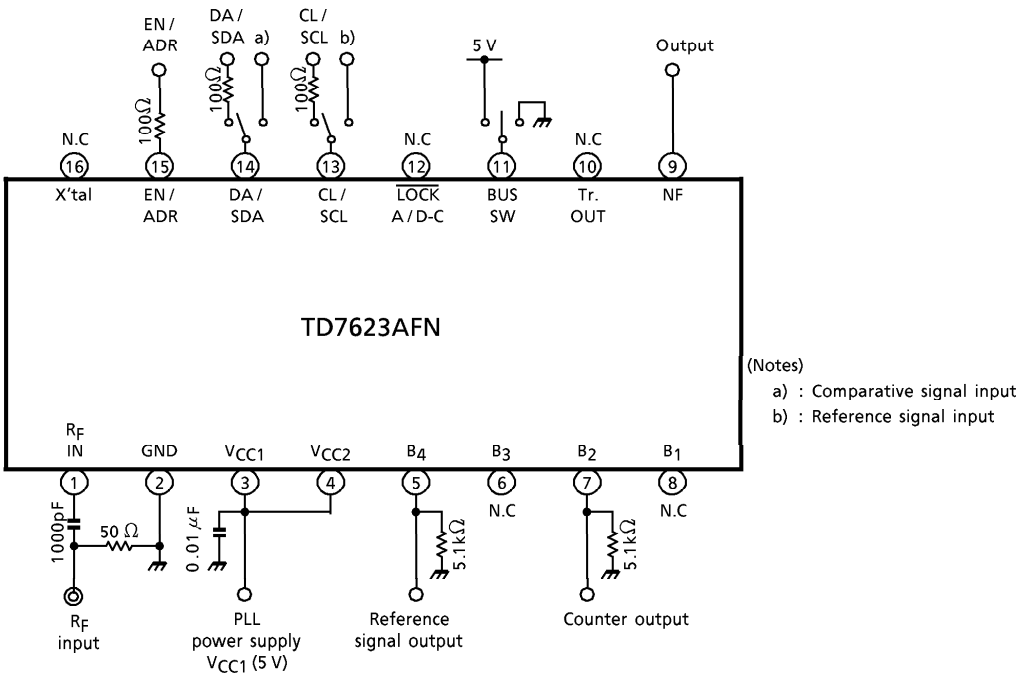
Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Tights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

TEST CIRCUIT 1
Evaluation circuit board

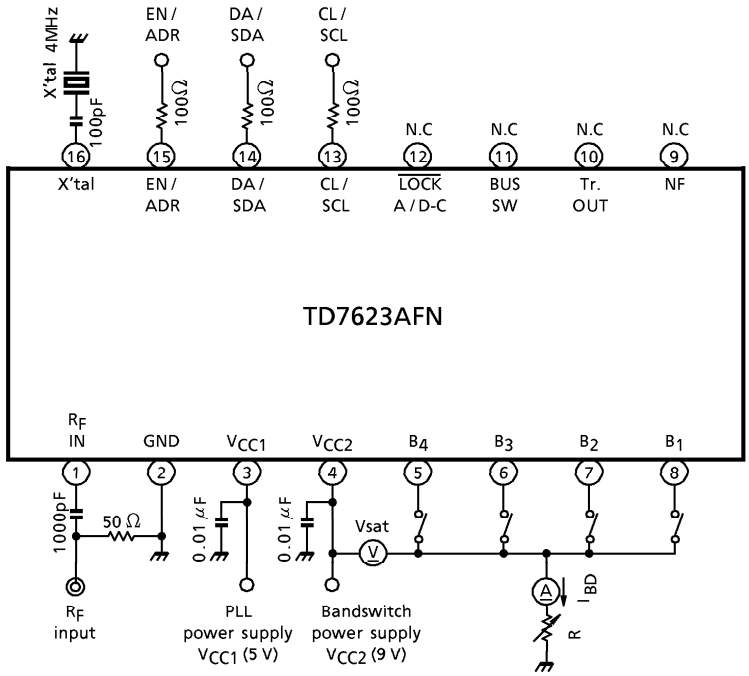


TEST CIRCUIT 2
Input sensitivity test circuit

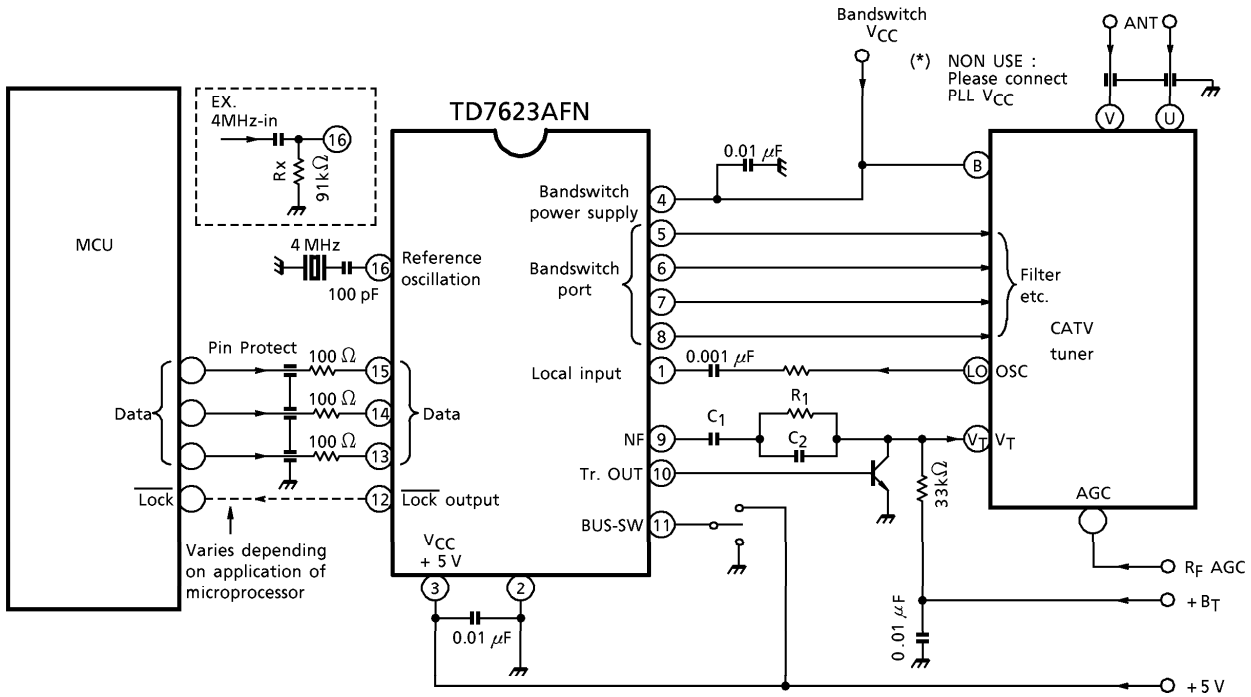
Test mode circuit



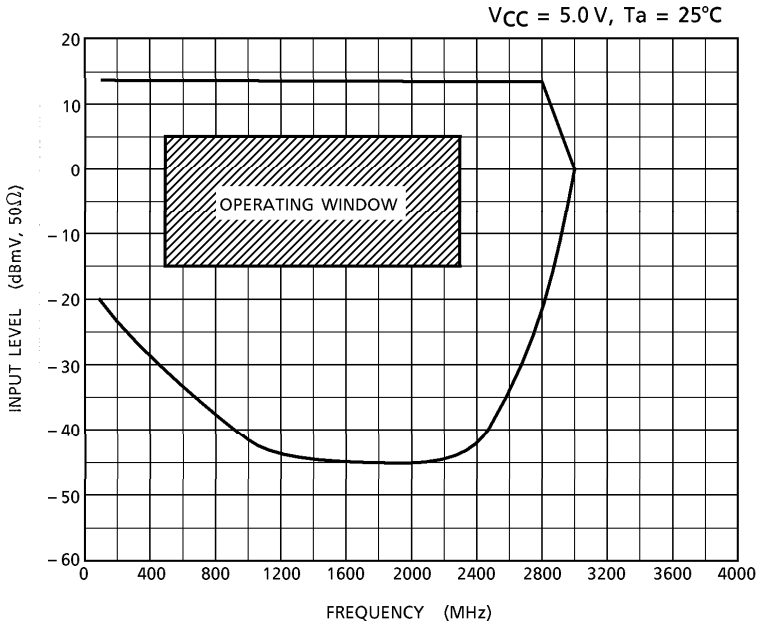
TEST CIRCUIT 3
Bandswitch drive test circuit



SYSTEM APPLICATION DIAGRAM



TYPICAL INPUT SENSITIVITY CURVE



FILTER COMPONENT EXPRESSION

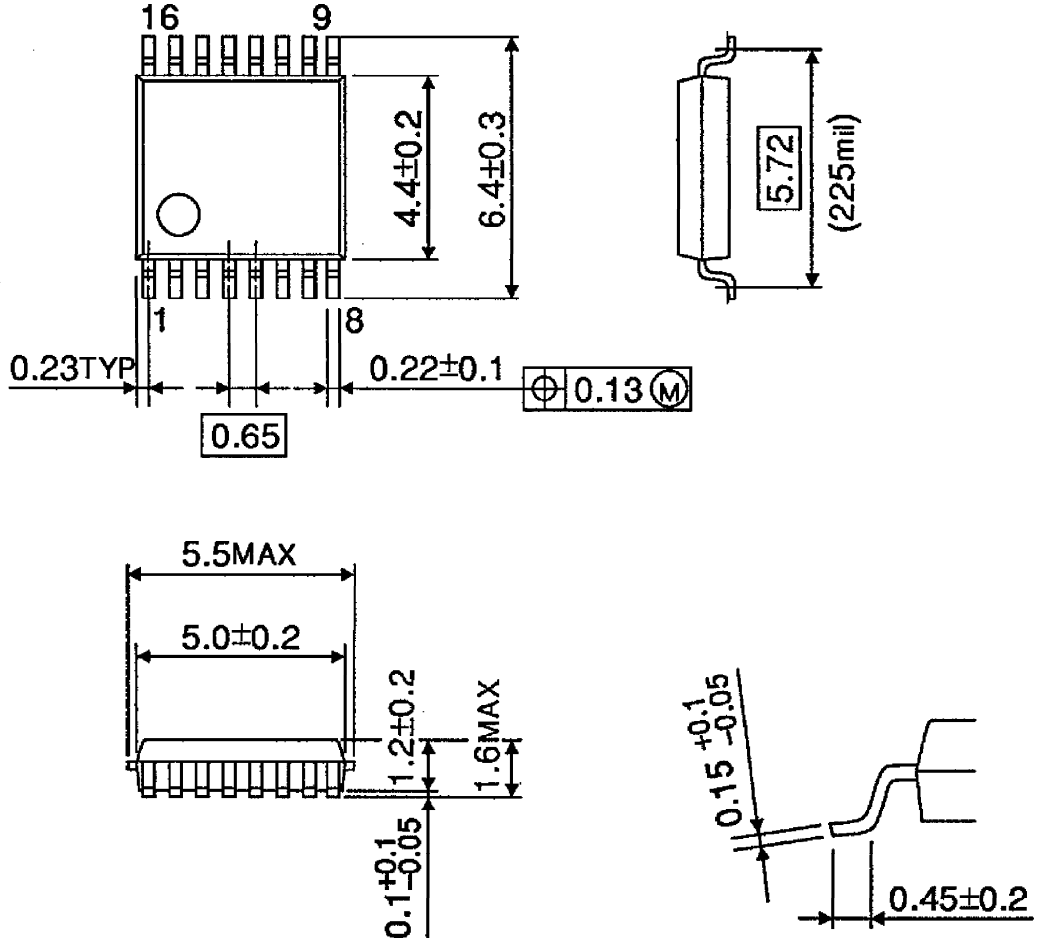
C1 = [Kv * Icomp / (2π)] / (ωn^2 * N)
R1 = [2 * ε] / (ωn * C1)
C2 = 1 / (2π * fc * R1)

with :
Kv = Oscillator control sensitivity (radian / Second / Volts)
Icomp = Charge-pump current (A)
ωn = Natural radian frequency (radian / Second)
N = Total counter ratio
ε = Dumping-factor (generaly : dumping-factor is about 0.5~1.0)
fc = filter cut-off frequency with combination resistor R1.
(generally : fc is about fr (reference frequency) / 20)

OUTLINE DRAWING

SSOP16-P-225-0.65B

Unit : mm



Weight : 0.07 g (Typ.)