

BUCKET BRIGADE DELAY LINE FOR ANALOGUE SIGNALS

The TDA1022 is a MOS monolithic integrated circuit, generally intended to delay analogue signals (e.g. delay time = $512/2 f_\phi$).

It can be used with clock frequencies in the range 5 kHz to 500 kHz.

The device contains 512 stages, so the input signal can be delayed from 51,2 ms to 0,512 ms.

Applications in which the device can be used:

- variation of fixed delays of analogue signals, vox control, equalizing speech delay in public address systems;
- in electronic organs and other musical instruments for vibrato and chorus effects;
- reverberation effects;
- variable compression and expansion of speech in tape-recorders;
- in communication systems for speech scrambling and time scale conversion.

QUICK REFERENCE DATA

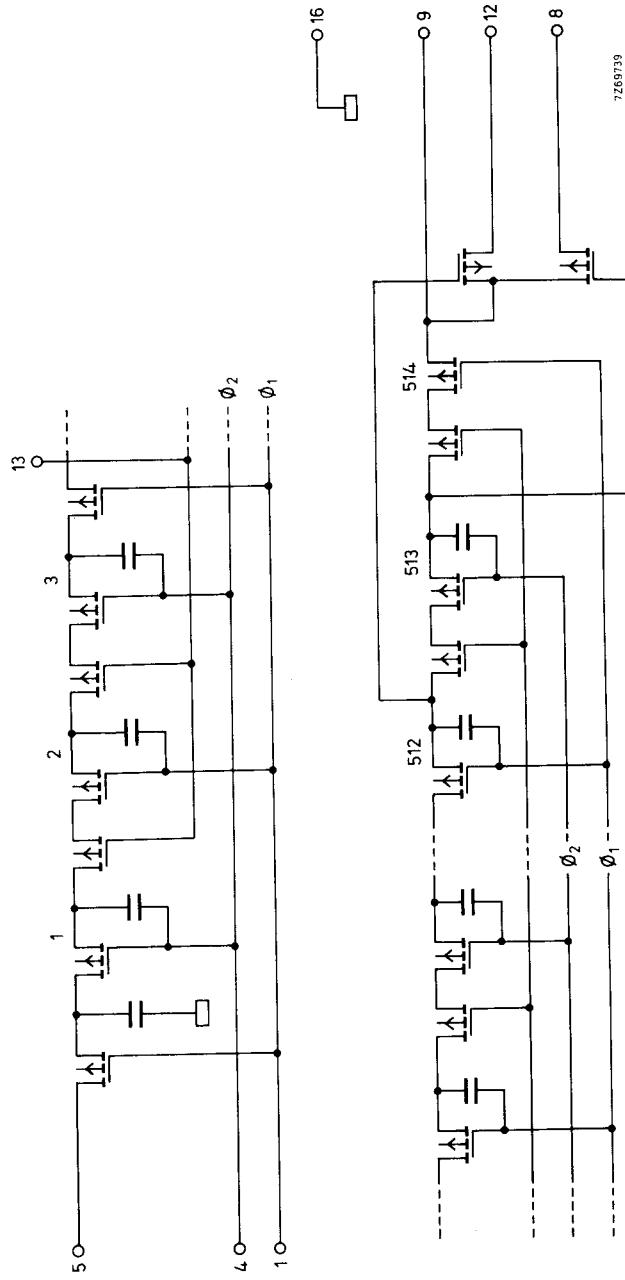
Supply voltage (pin 9)	V _{DD}	nom.	-15	V
Clock frequency	f _φ	5 to 500	kHz	
Number of stages			512	
Signal delay range	t _d	51,2 to 0,512	ms	
Signal frequency range	f _s	0 (d.c.) to 45	kHz	
Input voltage at pin 5 (peak-to-peak value)	V _{5-16(p-p)}	typ.	7	V
Line attenuation		typ.	4	dB 1)

PACKAGE OUTLINE plastic 16-lead dual in-line (see general section).



See note 1 on page 4.

CIRCUIT DIAGRAM



PINNING

1. Clock input 1 (V_{CL1})
2. Not connected
3. Not connected
4. Clock input 2 (V_{CL2})
5. Signal input
6. Not connected
7. Not connected
8. Output 513
9. Negative supply (V_{DD})
10. Not connected
11. Not connected
12. Output 512
13. Tetrode gate (V_{13-16})
14. Not connected
15. Not connected
16. Ground (substrate)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages (see note)

Supply voltage	V ₉₋₁₆	0 to -20	V
Clock input, data input, output voltage and V ₁₃₋₁₆		0 to -18	V

Current

Output current	I ₈ ; I ₁₂	0 to 5	mA
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Temperatures

Storage temperature	T _{stg}	-40 to +150	°C
Operating ambient temperature	T _{amb}	-20 to +85	°C

Note

Though MOS integrated circuits incorporate protection against electrostatic discharge, they can nevertheless be damaged by accidental over-voltages.
To be totally safe, it is desirable to take handling precautions into account.

CHARACTERISTICS at T_{amb} = -20 to +55 °C; V_{DD} = -15 V; V_{φ1} = V_{φ2} = -15 V;
V₁₃₋₁₆ = -14 V; R_L = 47 kΩ (unless otherwise specified)

Supply voltage range	V _{DD}	-10 to -18	V	1)
Supply current	I ₉	typ.	0,3	mA
Clock frequency	f _{φ1} ; f _{φ2}		5 to 500	kHz 2)
Clock pulse width	t _{φ1} ; t _{φ2}	≤	0,5T	3)
Clock pulse rise time	t _{φ1r} ; t _{φ2r}	typ.	0,05T	3)
fall time	t _{φ1f} ; t _{φ2f}	typ.	0,05T	3)
Clock pulse voltage levels; HIGH	V _{φ1H} ; V _{φ2H}		0 to -1,5	V
LOW	V _{φ1L} ; V _{φ2L}	typ.	-15	V 1)
			-10 to -18	V 1)

Signal input voltage at 1% output voltage
distortion (r.m.s. value)

V_{S(rms)} typ. 2,5 V

Signal frequency

f_S 0(d.c.) to 45 kHz

1) It is recommended that V₁₃₋₁₆ = V_{φ1L} + 1 V = V_{φ2L} + 1 V; V_{DD} more negative than V_{φL}.

2) In theory the clock frequency must be higher than twice the highest signal frequency; in practice f_S ≤ 0,3 f_φ to 0,5 f_φ is recommended, depending on the characteristics of the output filter.

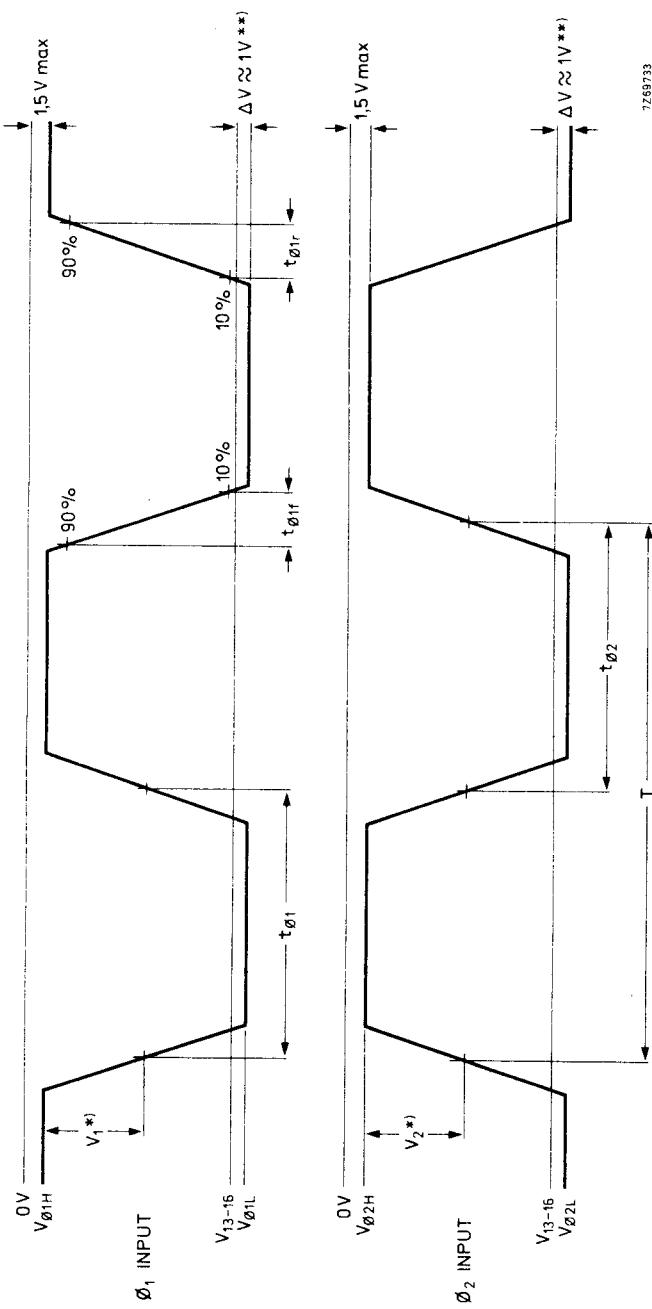
3) T = period time = 1/f_φ. The data on fall and rise times are given to eliminate overlap between the two clock pulses. To be independent of these rise and fall times a clock generator with simple gating can be used. See also pages 5 and 8.

CHARACTERISTICS (continued)

Attenuation from input to output $f_\phi = 40 \text{ kHz}; f_S = 1 \text{ kHz}$	typ. <	4 7	dB dB	1)
Change in output at $f_S = 1 \text{ kHz}; V_S(\text{rms}) = 1 \text{ V}$ when f_ϕ varies from 5 to 100 kHz	typ. <	0,5 1	dB dB	
when f_ϕ varies from 100 to 300 kHz	typ. <	0,5 1	dB dB	
D.C. voltage shift when f_ϕ varies from 5 to 300 kHz	<	0,5	V	
Noise output voltage (r.m.s. value) $f_\phi = 100 \text{ kHz}$ (weighted by "A" curve)	$V_N(\text{rms})$	typ.	0,25	mV
Signal-to-noise ratio at max. output voltage	S/N	typ.	74	dB
Load resistance	R_L	> typ.	10 47	$\text{k}\Omega$ $\text{k}\Omega$
				1)

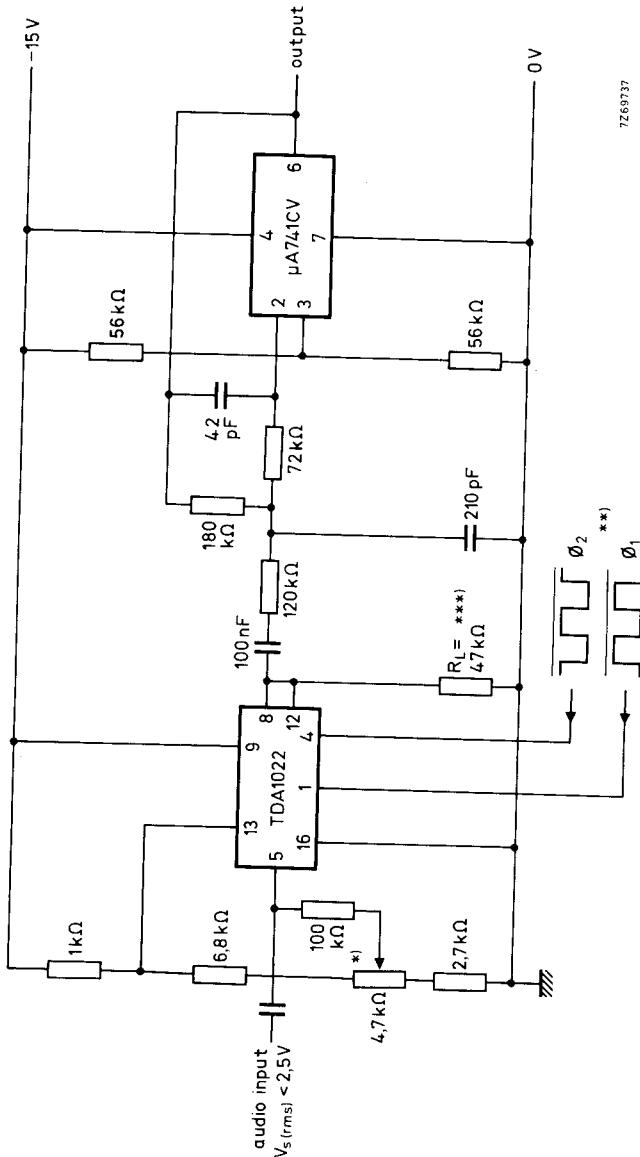
1) Attenuation can be reduced to typ. 2,5 dB if load resistor is replaced by a current source of 100 to 400 μA .

TIMING DIAGRAM



$* |V_1 + V_2| \leq |V_{\phi 1L}| ; V_{\phi 1L} = V_{\phi 2L}$.

**) For maximum dynamic range adjust V_{13-16} so that $\Delta V = V_{13-16} - V_{\phi L} \approx 1 \text{ V}$.



Single delay line connection

*) Adjust d.c. voltage for class-A operation (≈ 5 V).

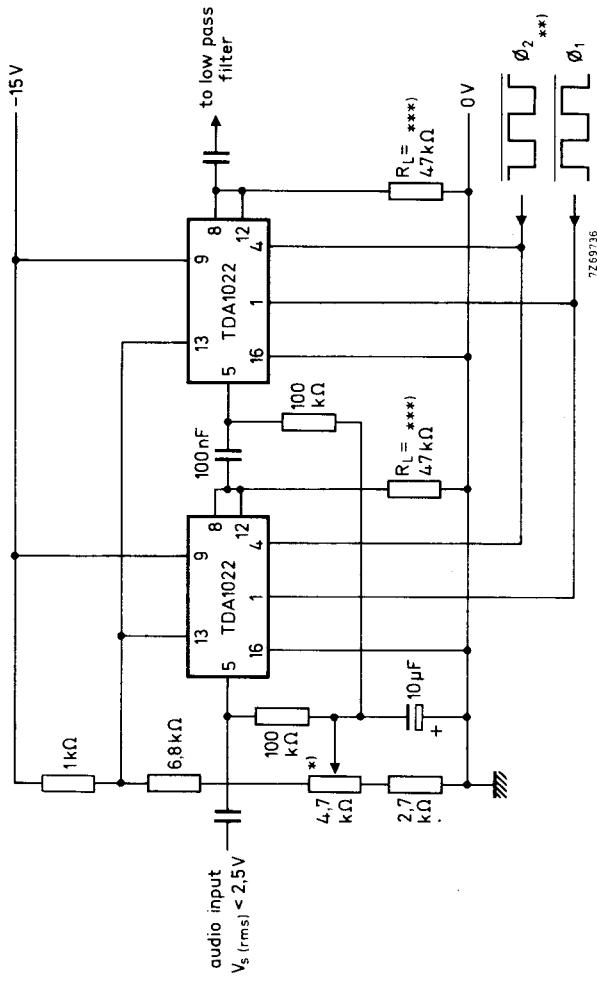
Conditions : low pass filter μ A741CV (12 dB per octave);
 gain = +3, 5 dB (compensation for line attenuation);
 $f_0 = 50$ kHz (min.);
 cut-off frequency = 15 kHz.

**) Clock input voltage amplitude: $V_{CL} = -15$ V.

(***) Can be replaced by a current source of
 100 to 400 μ A (see also note 1 on page 4).

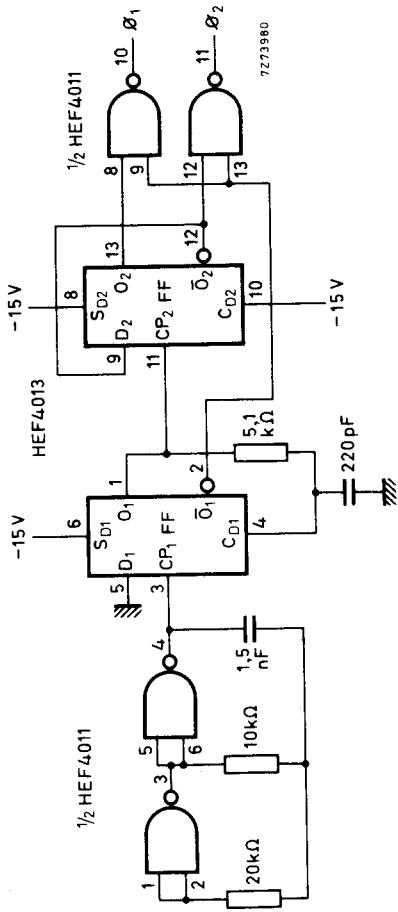
APPLICATION INFORMATION (continued)

October 1975



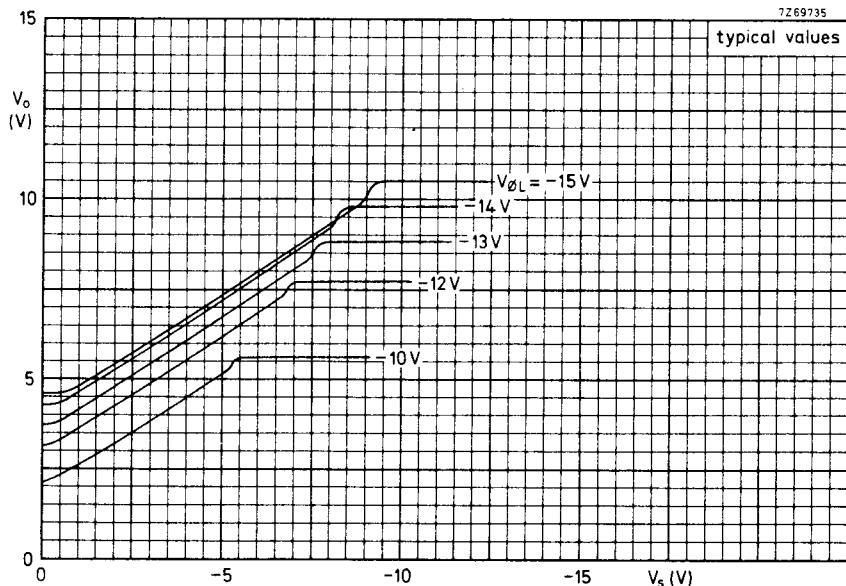
Series connection of two lines TDA1022

*) Adjust d. c. voltage for class-A operation ($\approx 5\text{ V}$).**) Clock input voltage amplitude: $V_{CL} \approx -15\text{ V}$.***) Can be replaced by a current source of 100 to 400 μA (see also note 1 on page 4).



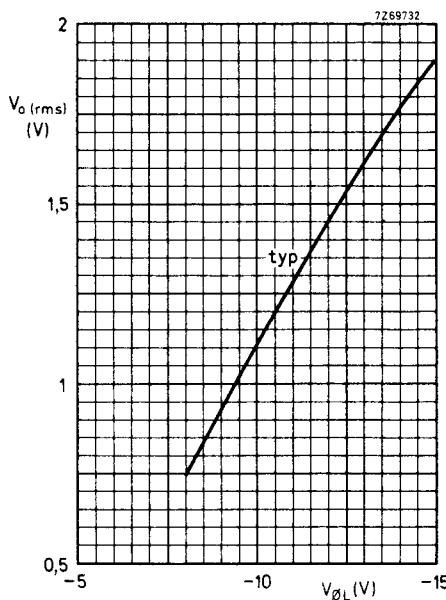
$V_{DD} = 0$
 $V_{SS} = -15 \text{ V}$
 $f_\phi = 15 \text{ kHz}$

Clock oscillator and driver circuit with elimination of overlap (for max. 6 x TDA1022)



Conditions for the graph above:

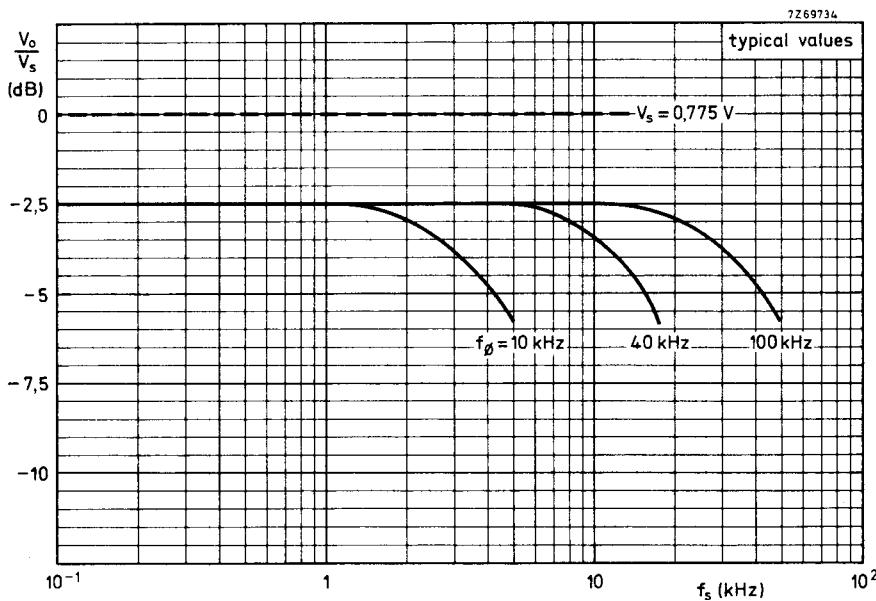
$V_{DD} = -15V$
 $V_{13-16} = -14V$
 $V_{\phi H} = 0V$
 $f_{\phi} = 40\text{ kHz}$
 $R_L = 47\text{ k}\Omega$



Conditions for the left-hand graph:

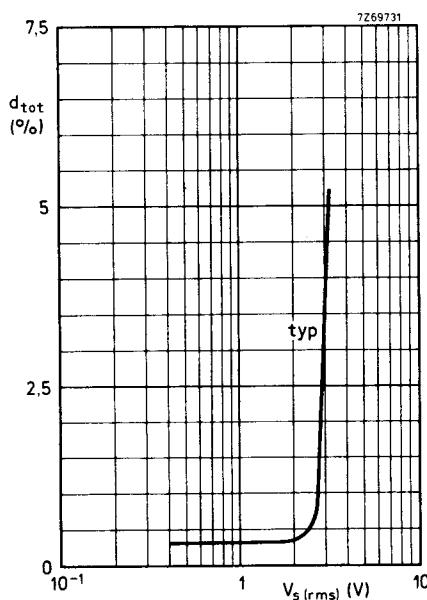
$V_{DD} = -15V$
 $V_{13-16} = -14V$
 $V_{\phi H} = 0V$
 $f_{\phi} = 40\text{ kHz}$
 $f_S = 1\text{ kHz}$
 $R_L = 47\text{ k}\Omega$

TDA1022



Conditions for the graph above:

$$\begin{aligned} V_{DD} &= -15 \text{ V} \\ V_{13-16} &= -14 \text{ V} \\ V_\phi &= 0 \text{ to } -15 \text{ V} \end{aligned}$$



Conditions for the left-hand graph:

$$\begin{aligned} f_s &= 1 \text{ kHz} \\ V_S &= -5, 2 \text{ V} \\ V_{DD} &= -15 \text{ V} \\ V_{13-16} &= -14 \text{ V} \\ V_\phi &= 0 \text{ to } -15 \text{ V} \\ f_\phi &= 40 \text{ kHz} \end{aligned}$$