CY74FCT257T QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

SCCS019D - MAY 1994 - REVISED NOVEMBER 2001

- Function, Pinout, and Drive Compatible
 With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- 64-mA Output Sink Current
 32-mA Output Source Current
- 3-State Outputs

Q OR SO PACKAGE (TOP VIEW) 16**∏** V_{CC} S 15 OE l_{0a} [] 2 14 🛮 I_{0c} I_{1a} [] 3 Y_a [] 4 13 🛮 I_{1c} 12 Y_C I_{0b} [] 5 I_{1b} [] 6 11 I I_{0d} 10 🛮 I_{1d} Y_b []7 GND [8 9 🛮 Y_d

description

The CY74FCT257T has four identical two-input multiplexers that select four bits of data from two sources under the control of a common data-select (S) input. The I_0 inputs are selected when S is low, and the I_1 inputs are selected when S is high. Data at the output is noninverted.

The CY74FCT257T is a logic implementation of a four-pole, two-position switch, where the position of the switch is determined by the logic levels at S. Outputs are in the high-impedance state when the output-enable (\overline{OE}) input is high.

All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. $\overline{\text{OE}}$ inputs must ensure that there is no overlap when outputs of 3-state devices are tied together.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	DESCRIPTION						
I	Data inputs						
S	Common data-select input						
ŌĒ	Output-enable input (active low)						
Y	Data outputs						



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



ORDERING INFORMATION

TA	PACKAGE [†]		PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QSOP – Q	Tape and reel	4.3	CY74FCT257CTQCT	FT257-3		
-40°C to 85°C	SOIC - SO	Tube	4.3	CY74FCT257CTSOC	FCT257C		
		Tape and reel	4.3	CY74FCT257CTSOCT	FC1237C		
	QSOP – Q	Tape and reel	5	CY74FCT257ATQCT	FT257-1		
	QSOP – Q	Tape and reel	6	CY74FCT257TQCT	FT257		

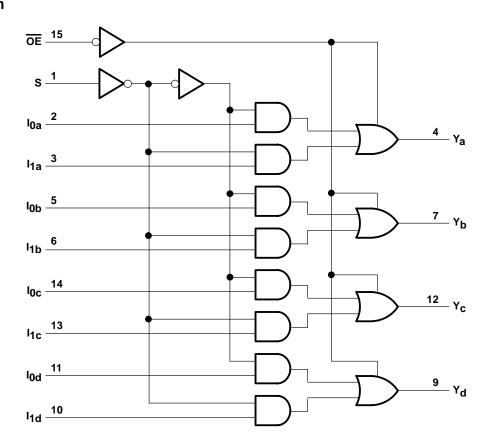
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

	OUTPUT			
OE	S	l ₀	l ₁	Y
Н	Х	Х	Х	Z
L	Н	X	L	L
L	Н	X	Н	Н
L	L	L	X	L
L	L	Н	X	Н

H = High logic level, L = Low logic level, X = Don't care, Z = High-impedance state

logic diagram





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ _{JA} (see Note 1): Q package	90°C/W
SO package	57°C/W
Ambient temperature range with power applied, T _A	–65°C to 135°C
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.25	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
ІОН	High-level output current			-32	mA
loL	Low-level output current			64	mA
TA	Operating free-air temperature	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP [†]	MAX	UNIT		
VIK	$V_{CC} = 4.75,$		-0.7	-1.2	V		
V _{OH}	$V_{CC} = 4.75,$	I _{OH} = -32 mA		2			V
V _{OL}	$V_{CC} = 4.75,$	I _{OL} = 64 mA			0.3	0.55	V
V _{hys}	All inputs				0.2		V
lį	V _{CC} = 5.25 V,	V _{IN} = 5.25 V				5	μΑ
lН	$V_{CC} = 5.25 \text{ V},$	$V_{IN} = 2.7 \text{ V}$				±1	μΑ
I _{IL}	$V_{CC} = 5.25 \text{ V},$	$V_{IN} = 0.5 V$				±1	μΑ
lozh	$V_{CC} = 5.25 \text{ V},$	V _{OUT} = 2.7 V				10	μΑ
lozL	$V_{CC} = 5.25 \text{ V},$	$V_{CC} = 5.25 \text{ V}, \qquad V_{OUT} = 0.5 \text{ V}$					
los [‡]	$V_{CC} = 5.25 \text{ V},$	V _{CC} = 5.25 V, V _{OUT} = 0 V					
l _{off}	$V_{CC} = 0 V$,	V _{CC} = 0 V, V _{OUT} = 4.5 V					
Icc	$V_{CC} = 5.25 \text{ V},$	$V_{IN} \le 0.2 V$,	$V_{IN} \ge V_{CC} - 0.2 \text{ V}$		0.1	0.2	mA
ΔlCC	V _{CC} = 5.25 V, V _{IN} =	: 3.4 V\$, f ₁ = 0, Outputs op	en		0.5	2	mA
ICCD¶		nput switching at 50% duty 2 V or V _{IN} ≥ V _{CC} – 0.2 V	cycle, Outputs open,		0.06	0.12	mA/ MHz
		One input switching at f ₁ = 10 MHz	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$		0.7	1.4	
I _C #	V _{CC} = 5.25 V,	at 50% duty cycle	V _{IN} = 3.4 V or GND		1	2.4	mA
IC"	Outputs open, OE = GND	Four bits switching at f ₁ = 2.5 MHz	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$		0.7	1.4	IIIA
		at 50% duty cycle	$V_{IN} = 3.4 \text{ V or GND}$		1.7	5.4	
C _i					5	10	pF
Co					9	12	pF

[†] Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

Where:

IC = Total supply current

ICC = Power-supply current with CMOS input levels

 ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4 \text{ V}$)

D_H = Duty cycle for TTL inputs high N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

N₁ = Number of inputs changing at f₁

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.



[‡] Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, IOS tests should be performed last.

[§] Per TTL-driven input (VIN = 3.4 V); all other inputs at VCC or GND

This parameter is derived for use in total power-supply calculations.

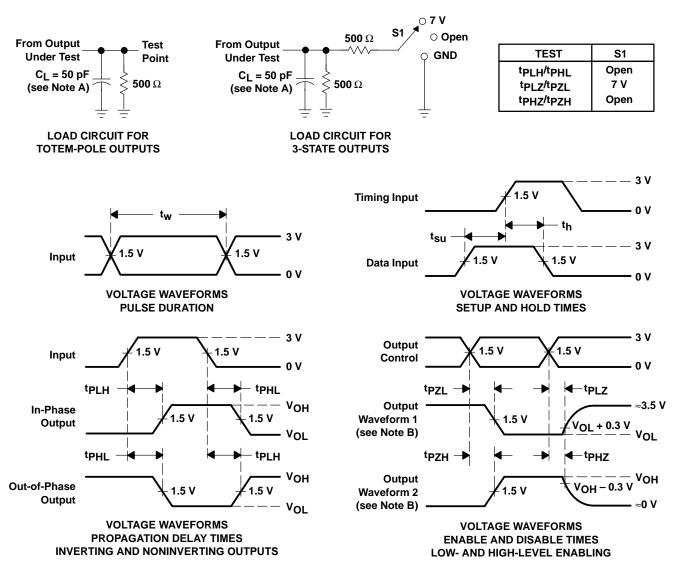
 $^{^{\#}}$ IC = ICC + Δ ICC \times DH \times NT + ICCD(f₀/2 + f₁ \times N₁)

CY74FCT257T **QUAD 2-INPUT MULTIPLEXER** WITH 3-STATE OUTPUTS SCCS019D - MAY 1994 - REVISED NOVEMBER 2001

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM	то	CY74FCT257T		CY74FCT257AT		CY74FCT257CT		UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _{PLH}	,	V	1.5	6	1.5	5	1.5	4.3	ns
^t PHL	'	ī	1.5	6	1.5	5	1.5	4.3	110
t _{PLH}	S	Y	1.5	10.5	1.5	7	1.5	5.2	20
^t PHL	3		1.5	10.5	1.5	7	1.5	5.2	ns
^t PZH		V	1.5	8.5	1.5	7	1.5	6	no
tPZL	ŌĒ	ī	1.5	8.5	1.5	7	1.5	6	ns
^t PHZ	ŌĒ	OE V	1.5	6	1.5	5.5	1.5	5	no
tPLZ	OE	ī	1.5	6	1.5	5.5	1.5	5	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms









PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CY74FCT257ATD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257ATDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257ATDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257ATDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257ATQCT	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT257ATQCTE4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT257CTD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257CTDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257CTDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257CTDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257CTQCT	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT257CTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT257CTSOC	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257CTSOCE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257CTSOCT	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257CTSOCTE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT257TQCT	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT257TQCTE4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

 $^{^{(1)}}$ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

Pb-Free (RoHS): Tl's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.



PACKAGE OPTION ADDENDUM

30-Aug-2005

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AC.



DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



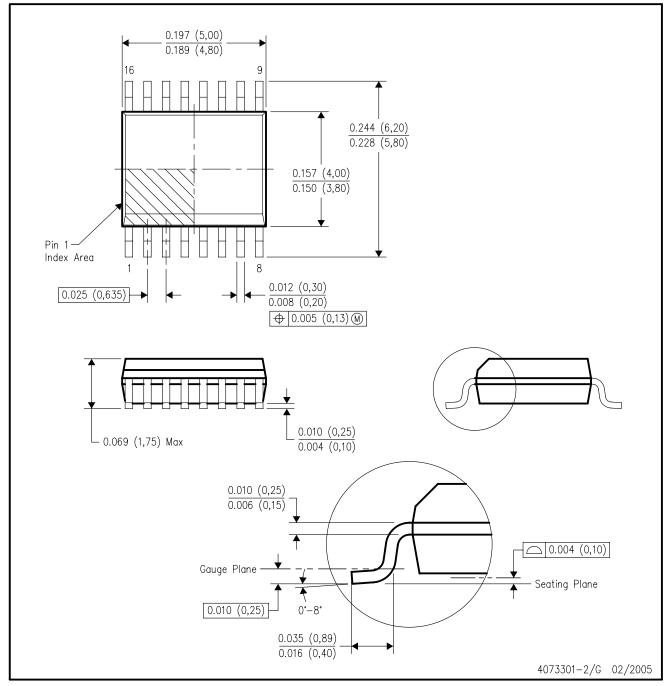
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



DBQ (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AB.



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