FAIRCHILD SEMICONDUCTOR™

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# 74LVT16373 • 74LVTH16373
# Low Voltage 16-Bit Transparent Latch with 3-STATE Outputs

## General Description

The LVT16373 and LVTH16373 contain sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state.

The LVTH16373 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These latches are designed for low-voltage (3.3V) $V_{CC}$ applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16373 and LVTH16373 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

## Features

- Input and output interface capability to systems at 5V $V_{CC}$
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH16373), also available without bushold feature (74LVT16373)
- Live insertion/extraction permitted
- Power Up/Power Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Functionally compatible with the 74 series 16373
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

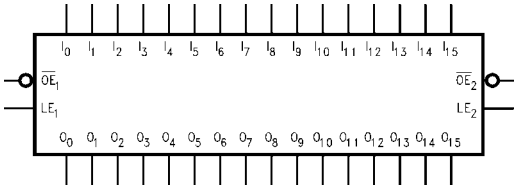
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74LVT16373GX (Note 1) | BGA54A (Preliminary) | 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL] |
| 74LVT16373MEA (Note 2) | MS48A | 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide |
| 74LVT16373MTD (Note 2) | MTD48 | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |
| 74LVTH16373GX (Note 1) | BGA54A (Preliminary) | 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL] |
| 74LVTH16373MEA (Note 2) | MS48A | 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide |
| 74LVTH16373MTD (Note 2) | MTD48 | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

**Note 1:** BGA package available in Tape and Reel only.

**Note 2:** Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

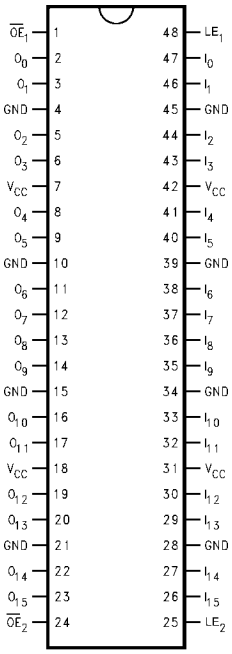
## Logic Symbol



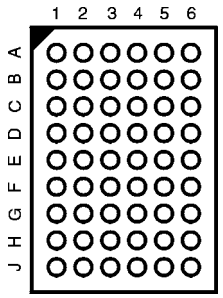

 

## Connection Diagrams

**Pin Assignment for SSOP and TSSOP**




**Pin Assignment for FBGA**




**(Top Thru View)**

## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OE}_n$ | Output Enable Input (Active LOW) |
| $LE_n$ | Latch Enable Input |
| $I_0$–$I_{15}$ | Inputs |
| $O_0$–$O_{15}$ | 3-STATE Outputs |
| NC | No Connect |

## FBGA Pin Assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | $O_0$ | NC | $\overline{OE}_1$ | $LE_1$ | NC | $I_0$ |
| **B** | $O_2$ | $O_1$ | NC | NC | $I_1$ | $I_2$ |
| **C** | $O_4$ | $O_3$ | $V_{CC}$ | $V_{CC}$ | $I_3$ | $I_4$ |
| **D** | $O_6$ | $O_5$ | GND | GND | $I_5$ | $I_6$ |
| **E** | $O_8$ | $O_7$ | GND | GND | $I_7$ | $I_8$ |
| **F** | $O_{10}$ | $O_9$ | GND | GND | $I_9$ | $I_{10}$ |
| **G** | $O_{12}$ | $O_{11}$ | $V_{CC}$ | $V_{CC}$ | $I_{11}$ | $I_{12}$ |
| **H** | $O_{14}$ | $O_{13}$ | NC | NC | $I_{13}$ | $I_{14}$ |
| **J** | $O_{15}$ | NC | $\overline{OE}_2$ | $LE_2$ | NC | $I_{15}$ |

## Truth Tables

| Inputs | | | Outputs |
|---|---|---|---|
| $LE_1$ | $\overline{OE}_1$ | $I_0$–$I_7$ | $O_0$–$O_7$ |
| X | H | X | Z |
| H | L | L | L |
| H | L | H | H |
| L | L | X | $O_o$ |

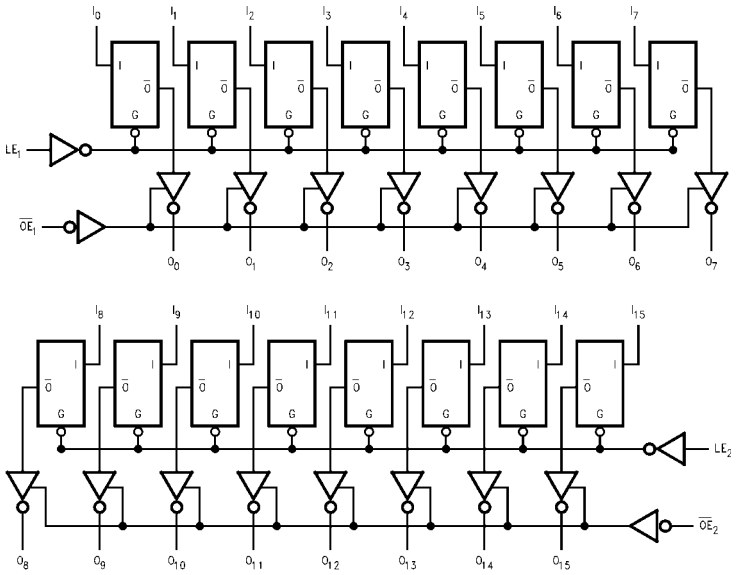
| Inputs | | | Outputs |
|---|---|---|---|
| $LE_2$ | $\overline{OE}_2$ | $I_8$–$I_{15}$ | $O_8$–$O_{15}$ |
| X | H | X | Z |
| H | L | L | L |
| H | L | H | H |
| L | L | X | $O_o$ |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
$O_o$ = Previous output prior to HIGH-to-LOW transition of LE

## Functional Description

The LVT16373 and LVTH16373 contain sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable ($LE_n$) input is HIGH, data on the $D_n$ enters the latches. In this condition the latches are transparent, i.e, a latch output will change states each time its D input changes. When $LE_n$ is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of $LE_n$. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## Logic Diagrams




Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 3)

| Symbol | Parameter | Value | Conditions | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 to +4.6 | | V |
| $V_I$ | DC Input Voltage | −0.5 to +7.0 | | V |
| $V_O$ | DC Output Voltage | −0.5 to +7.0 | Output in 3-STATE | V |
| | | −0.5 to +7.0 | Output in HIGH or LOW State (Note 4) | |
| $I_{IK}$ | DC Input Diode Current | −50 | $V_I$ < GND | mA |
| $I_{OK}$ | DC Output Diode Current | −50 | $V_O$ < GND | mA |
| $I_O$ | DC Output Current | 64 | $V_O > V_{CC}$ Output at HIGH State | mA |
| | | 128 | $V_O > V_{CC}$ Output at LOW State | |
| $I_{CC}$ | DC Supply Current per Supply Pin | ±64 | | mA |
| $I_{GND}$ | DC Ground Current per Ground Pin | ±128 | | mA |
| $T_{STG}$ | Storage Temperature | −65 to +150 | | °C |

## Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.7 | 3.6 | V |
| $V_I$ | Input Voltage | 0 | 5.5 | V |
| $I_{OH}$ | HIGH Level Output Current | | −32 | mA |
| $I_{OL}$ | LOW Level Output Current | | 64 | mA |
| $T_A$ | Free-Air Operating Temperature | −40 | 85 | °C |
| $\Delta t/\Delta V$ | Input Edge Rate, $V_{IN}$ = 0.8V–2.0V, $V_{CC}$ = 3.0V | 0 | 10 | ns/V |

**Note 3:** Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

**Note 4:** $I_O$ Absolute Maximum Rating must be observed.

## DC Electrical Characteristics

| Symbol | Parameter | | $V_{CC}$ (V) | $T_A$ = −40°C to +85°C Min | $T_A$ = −40°C to +85°C Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input Clamp Diode Voltage | | 2.7 | | −1.2 | V | $I_I$ = −18 mA |
| $V_{IH}$ | Input HIGH Voltage | | 2.7–3.6 | 2.0 | | V | $V_O \le$ 0.1V or |
| $V_{IL}$ | Input LOW Voltage | | 2.7–3.6 | | 0.8 | V | $V_O \ge V_{CC}$ − 0.1V |
| $V_{OH}$ | Output HIGH Voltage | | 2.7–3.6 | $V_{CC}$ − 0.2 | | V | $I_{OH}$ = −100 μA |
| | | | 2.7 | 2.4 | | | $I_{OH}$ = −8 mA |
| | | | 3.0 | 2.0 | | | $I_{OH}$ = −32 mA |
| $V_{OL}$ | Output LOW Voltage | | 2.7 | | 0.2 | V | $I_{OL}$ = 100 μA |
| | | | 2.7 | | 0.5 | | $I_{OL}$ = 24 mA |
| | | | 3.0 | | 0.4 | | $I_{OL}$ = 16 mA |
| | | | 3.0 | | 0.5 | | $I_{OL}$ = 32 mA |
| | | | 3.0 | | 0.55 | | $I_{OL}$ = 64 mA |
| $I_{I(HOLD)}$ (Note 5) | Bushold Input Minimum Drive | | 3.0 | 75 | | μA | $V_I$ = 0.8V |
| | | | | −75 | | | $V_I$ = 2.0V |
| $I_{I(OD)}$ (Note 5) | Bushold Input Over-Drive Current to Change State | | 3.0 | 500 | | μA | (Note 6) |
| | | | | −500 | | | (Note 7) |
| $I_I$ | Input Current | | 3.6 | | 10 | μA | $V_I$ = 5.5V |
| | | Control Pins | 3.6 | | ±1 | | $V_I$ = 0V or $V_{CC}$ |
| | | Data Pins | 3.6 | | −5 | | $V_I$ = 0V |
| | | | | | 1 | | $V_I$ = $V_{CC}$ |
| $I_{OFF}$ | Power Off Leakage Current | | 0 | | ±100 | μA | 0V ≤ $V_I$ or $V_O$ ≤ 5.5V |
| $I_{PU/PD}$ | Power Up/Down 3-STATE Output Current | | 0–1.5V | | ±100 | μA | $V_O$ = 0.5V to 3.0V, $V_I$ = GND or $V_{CC}$ |
| $I_{OZL}$ | 3-STATE Output Leakage Current | | 3.6 | | −5 | μA | $V_O$ = 0.5V |
| $I_{OZH}$ | 3-STATE Output Leakage Current | | 3.6 | | 5 | μA | $V_O$ = 3.0V |
| $I_{OZH^+}$ | 3-STATE Output Leakage Current | | 3.6 | | 10 | μA | $V_{CC} < V_O \le$ 5.5V |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = -40°C$ to $+85°C$ | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| $I_{CCH}$ | Power Supply Current | 3.6 | | 0.19 | mA | Outputs HIGH |
| $I_{CCL}$ | Power Supply Current | 3.6 | | 5 | mA | Outputs LOW |
| $I_{CCZ}$ | Power Supply Current | 3.6 | | 0.19 | mA | Outputs Disabled |
| $I_{CCZ+}$ | Power Supply Current | 3.6 | | 0.19 | mA | $V_{CC} \le V_O \le 5.5V$, Outputs Disabled |
| $\Delta I_{CC}$ | Increase in Power Supply Current (Note 8) | 3.6 | | 0.2 | mA | One Input at $V_{CC} - 0.6V$ Other Inputs at $V_{CC}$ or GND |

**Note 5:** Applies to bushold versions only (74LVTH16373).

**Note 6:** An external driver must source at least the specified current to switch from LOW-to-HIGH.

**Note 7:** An external driver must sink at least the specified current to switch from HIGH-to-LOW.

**Note 8:** This is the increase in supply current for each input that is at the specified voltage level rather than $V_{CC}$ or GND.

## Dynamic Switching Characteristics (Note 9)

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = 25°C$ | | | Units | Conditions $C_L = 50$ pF, $R_L = 500\Omega$ |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 3.3 | | 0.8 | | V | (Note 10) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 3.3 | | –0.8 | | V | (Note 10) |

**Note 9:** Characterized in SSOP package. Guaranteed parameter, but not tested.

**Note 10:** Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $C_L = 50$pF, $R_L = 500\Omega$ | | | | Units |
|---|---|---|---|---|---|---|
| | | $V_{CC} = 3.3V \pm 0.3V$ | | $V_{CC} = 2.7V$ | | |
| | | Min | Max | Min | Max | |
| $t_{PHL}$ | Propagation Delay | 1.5 | 3.9 | 1.5 | 4.3 | ns |
| $t_{PLH}$ | $D_n$ to $O_n$ | 1.5 | 3.8 | 1.5 | 4.2 | |
| $t_{PHL}$ | Propagation Delay | 1.9 | 4.2 | 1.9 | 4.4 | ns |
| $t_{PLH}$ | LE to $O_n$ | 1.6 | 4.3 | 1.6 | 4.8 | |
| $t_{PZL}$ | Output Enable Time | 1.3 | 4.3 | 1.3 | 4.9 | ns |
| $t_{PZH}$ | | 1.0 | 4.3 | 1.0 | 5.1 | |
| $t_{PLZ}$ | Output Disable Time | 1.5 | 4.7 | 1.5 | 4.8 | ns |
| $t_{PHZ}$ | | 2.0 | 5.0 | 2.0 | 5.4 | |
| $t_S$ | Setup Time, $D_n$ to LE | 1.0 | | 0.8 | | ns |
| $t_H$ | Hold Time, $D_n$ to LE | 1.0 | | 1.1 | | ns |
| $t_W$ | LE Pulse Width | 3.0 | | 3.0 | | ns |
| $t_{OSHL}$ | Output to Output Skew (Note 11) | | 1.0 | | 1.0 | ns |
| $t_{OSLH}$ | | | 1.0 | | 1.0 | |

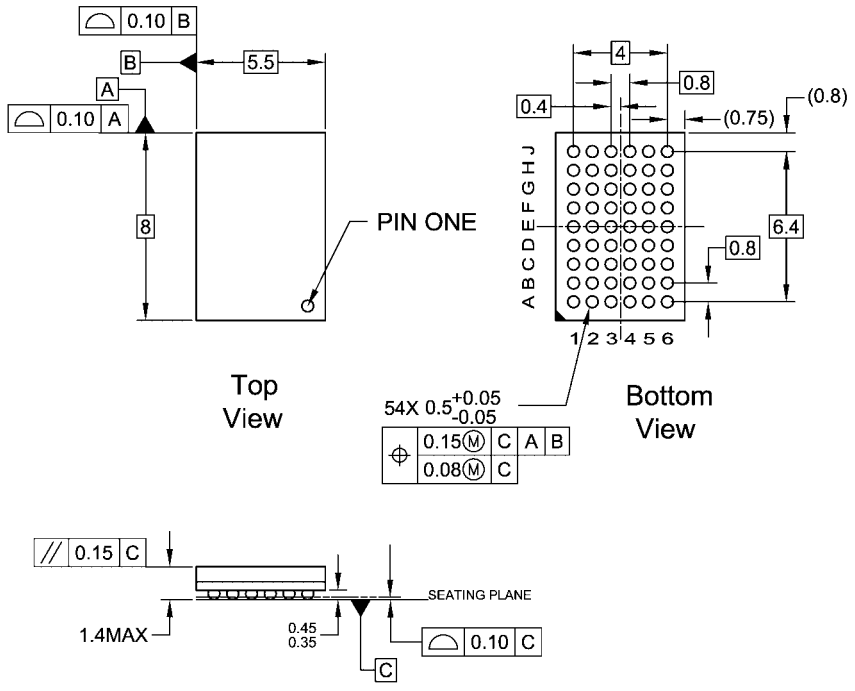
**Note 11:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$).

## Capacitance (Note 12)

| Symbol | Parameter | Conditions | Typical | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = Open, $V_I = 0V$ or $V_{CC}$ | 4 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC} = 3.0V$, $V_O = 0V$ or $V_{CC}$ | 8 | pF |

**Note 12:** Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

## Physical Dimensions inches (millimeters) unless otherwise noted



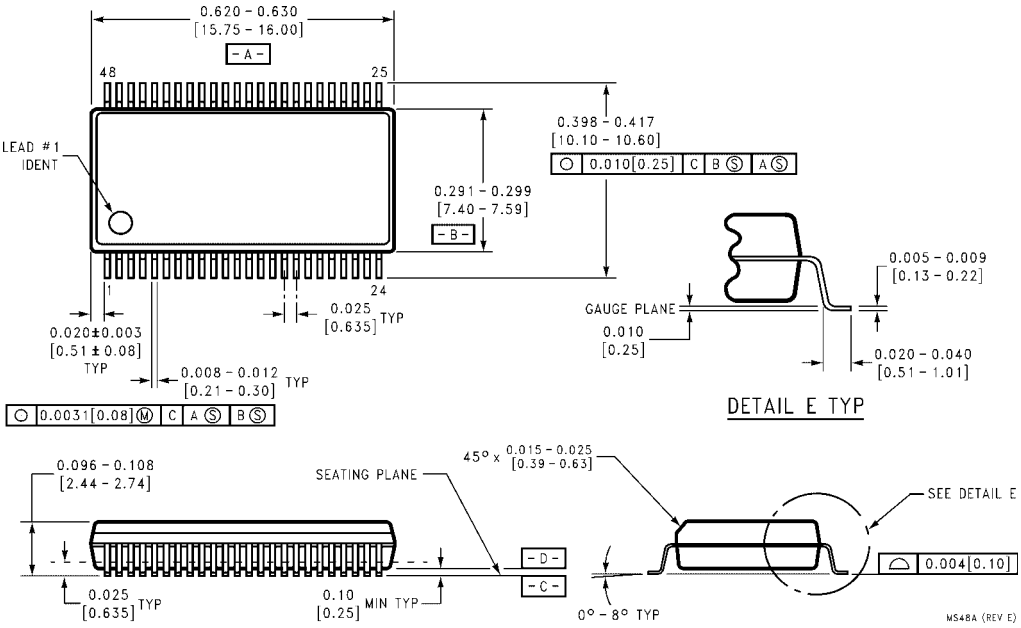

NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

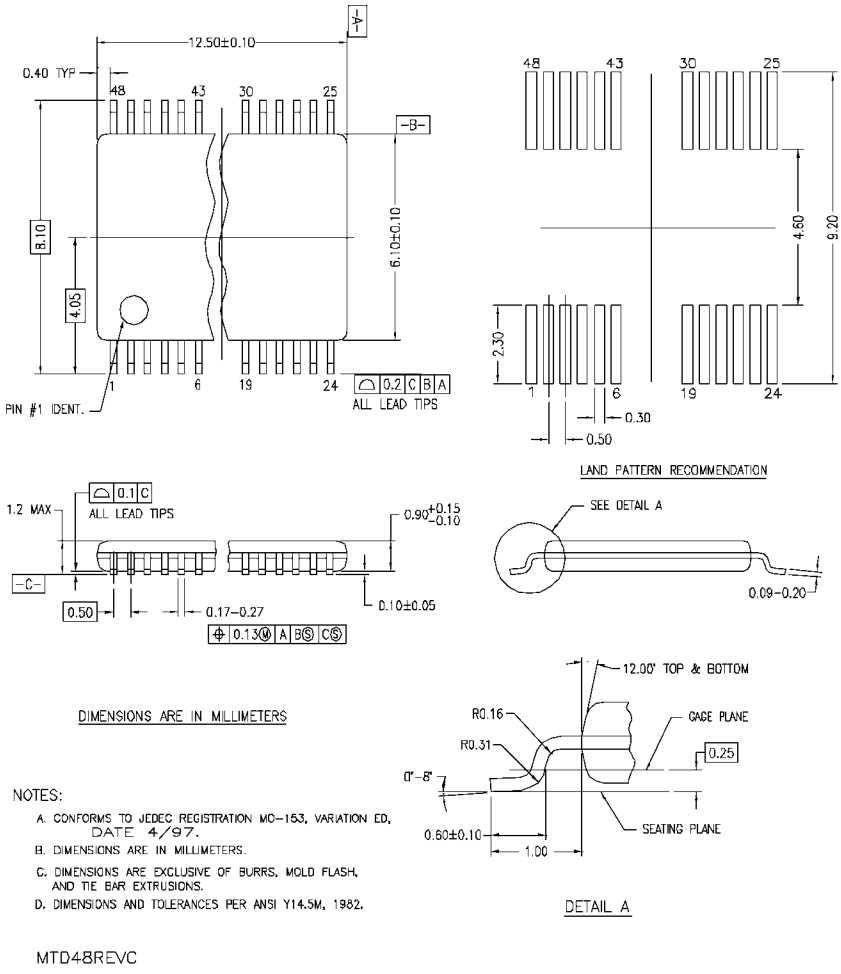
**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide**
**Package Number BGA54A**
**Preliminary**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide**
**Package Number MS48A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD48**



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