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## NTE929 Integrated Circuit General Purpose, High Current, NPN Transistor Array

### Description:

The NTE929 is a versatile array of five high-current (to 100mA) NPN transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistors plus a separate terminal for the substrate permit maximum flexibility in circuit design.

### Features:

- High  $I_C$  100mA max
- Low  $V_{CEsat}$  (at 50mA) 0.7V max.
- Matched pair (Q1 and Q2)
  - $V_{10}$  ( $V_{BE}$  matched):  $\pm 5mV$  max.
  - $I_{10}$  (at 1mA): 2.5 $\mu A$  max.
- 5 independent transistors plus separate substrate connection.

### Applications:

- Signal processing and switching systems operating from DC to VHF
- Lamp and relay driver
- Differential amplifier
- Temperature-compensated amplifier
- Thyristor firing

### Absolute Maximum Ratings: ( $T_A = +25^\circ C$ unless otherwise specified)

Power Dissipation, $P_D$	
Any One Transistor .....	500mW
Total Package .....	750mW
Derate Above $55^\circ C$ .....	Derate Linearly 6.67mW/ $^\circ C$
Operating Ambient Temperature Range, $T_{opr}$ .....	$-55$ to $+125^\circ C$
Storage Temperature range, $T_{stg}$ .....	$-65$ to $+150^\circ C$
Lead Temperature (During Soldering, 1/16" $\pm$ 1/32" from case, 10sec max), $T_L$ .....	$+265^\circ C$

### **The following ratings apply for each transistor in the device:**

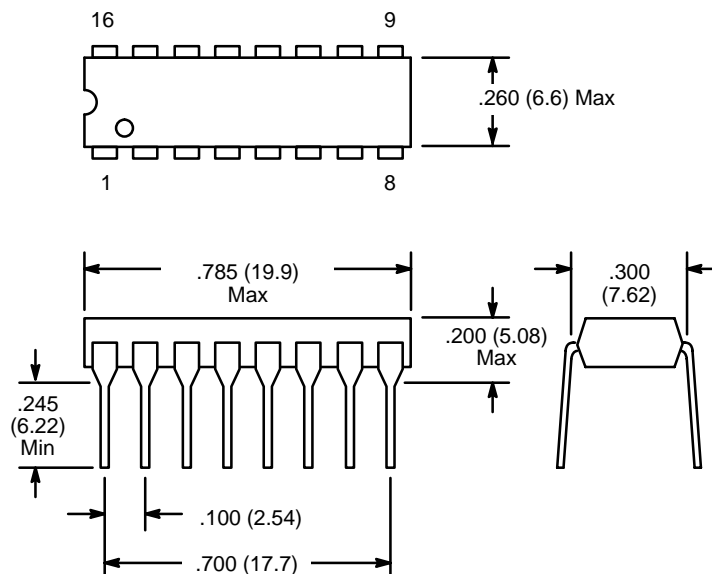
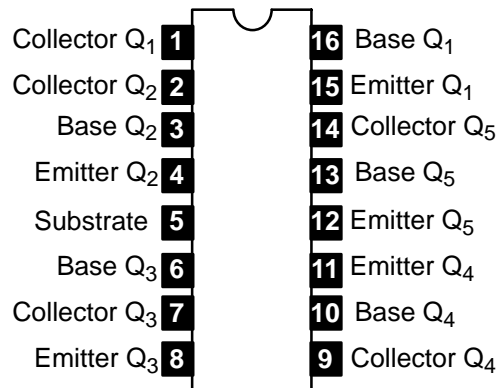
Collector-Emitter Voltage, $V_{CEO}$ .....	15V
Collector-Base Voltage, $V_{CBO}$ .....	20V
Collector-Substrate Voltage, $V_{CIO}$ .....	20V
Emitter-Base Voltage, $V_{EBO}$ .....	5V
Collector Current, $I_C$ .....	20mA
Base Current, $I_B$ .....	20mA

Note 1. The collector of each transistor of the NTE929 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (Pin5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

**Electrical Characteristics:** ( $T_A = +25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>For Each Transistor</b>						
Collector–Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\mu\text{A}, I_E = 0$	20	60	–	V
Collector–Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\text{mA}, I_B = 0$	15	24	–	V
Collector–Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 100\mu\text{A}, I_B = 0, I_E = 0$	20	60	–	V
Emitter–Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 500\mu\text{A}, I_C = 0$	5.0	6.9	–	V
Collector Cutoff Current	$I_{CEO}$	$V_{CE} = 10\text{V}, I_B = 0$	–	–	10	$\mu\text{A}$
	$I_{CBO}$	$V_{CE} = 10\text{V}, I_E = 0$	–	–	1	$\mu\text{A}$
DC Forward Current	$h_{FE}$	$V_{CE} = 3\text{V}, I_C = 10\text{mA}$	40	76	–	
		$V_{CE} = 3\text{V}, I_C = 50\text{mA}$	40	75	–	
Base–Emitter Voltage	$V_{BE}$	$V_{CE} = 3\text{V}, I_C = 10\text{mA}$	0.65	0.74	0.85	V
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 50\text{mA}, I_B = 5\text{mA}$	–	0.4	0.7	V
Gain–Bandwidth Product	$f_T$	$V_{CE} = 3\text{V}, I_C = 10\text{mA}$	–	450	–	MHz
Absolute Input Offset Voltage	$V_{IO}$	$V_{CE} = 3\text{V}, I_C = 1\text{mA}$	–	1.2	5.0	mV
Absolute Input Offset Current	$I_{IO}$	$V_{CE} = 3\text{V}, I_C = 1\text{mA}$	–	0.7	2.5	$\mu\text{A}$

**Pin Connection Diagram**



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