DATA SHEET

TEA1068
Versatile telephone transmission circuit with dialler interface

Product specification
Supersedes data of June 1990
File under Integrated Circuits, IC03

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Philips Semiconductors

PHILIPS

FEATURES

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- Dual-Tone Multi-Frequency (DTMF) signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current-dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility.

GENERAL DESCRIPTION

The TEA1068 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech.

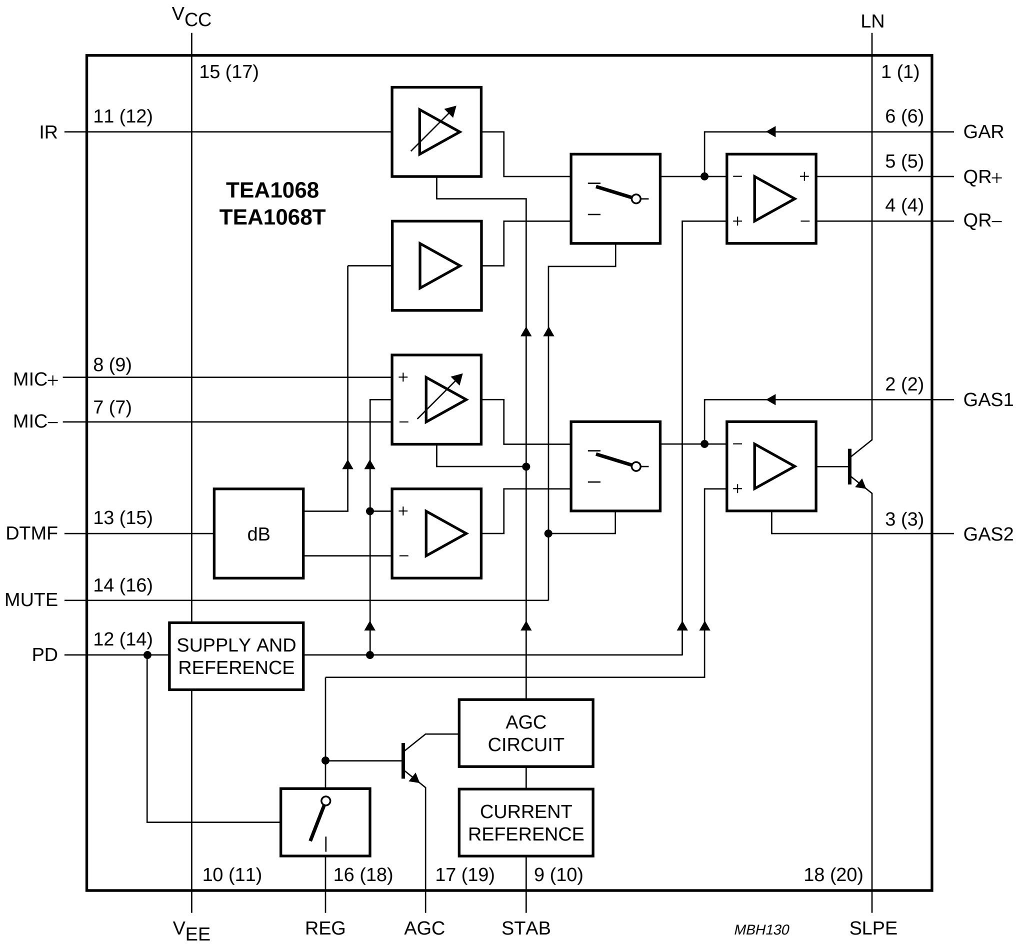
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	4.2	4.45	4.7	V
I_{line}	line current					
	TEA1068	normal operation	10	–	140	mA
	TEA1068T	normal operation	10	–	100	mA
I_{CC}	internal supply current	power down; input LOW	–	0.96	1.3	mA
		power down; input HIGH	–	55	82	μA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; MUTE = HIGH				
		I_p = 1.2 mA	2.8	3.05	–	V
		I_p = 1.7 mA	2.5	–	–	V
G_v	voltage gain					
	microphone amplifier		44	–	60	dB
	receiving amplifier		17	–	39	dB
ΔG_v	line loss compensation gain control range		5.5	5.9	6.3	dB
V_{exch}	exchange supply voltage		24	–	60	V
R_{exch}	exchange feeding bridge resistance range		0.4	–	1	kΩ
T_{amb}	ambient operating temperature		–25		+75	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1068	DIP18	plastic dual in-line package; 18 leads (300 mil)	SOT102-1
TEA1068T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM



The figures in parentheses refer to the TEA1068T.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TEA1068	TEA1068T	
LN	1	1	positive line terminal
GAS1	2	2	gain adjustment transmitting amplifier
GAS2	3	3	gain adjustment transmitting amplifier
QR–	4	4	inverting output receiving amplifier
QR+	5	5	non-inverting output receiving amplifier
GAR	6	6	gain adjustment receiving amplifier
MIC–	7	7	inverting microphone input
n.c.	–	8	not connected
MIC+	8	9	non-inverting microphone input
STAB	9	10	current stabilizer
V_{EE}	10	11	negative line terminal
IR	11	12	receiving amplifier input
n.c.	–	13	not connected
PD	12	14	power-down input
DTMF	13	15	dual-tone multi-frequency input
MUTE	14	16	mute input
V_{CC}	15	17	positive supply decoupling
REG	16	18	voltage regulator decoupling
AGC	17	19	automatic gain control input
SLPE	18	20	slope (DC resistance) adjustment

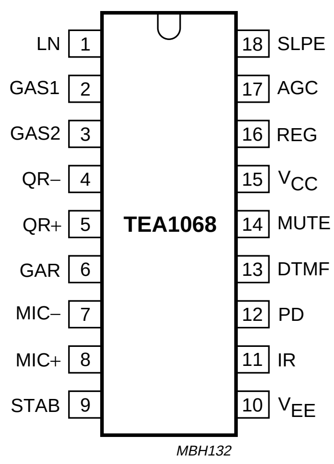


Fig.2 Pin configuration TEA1068.

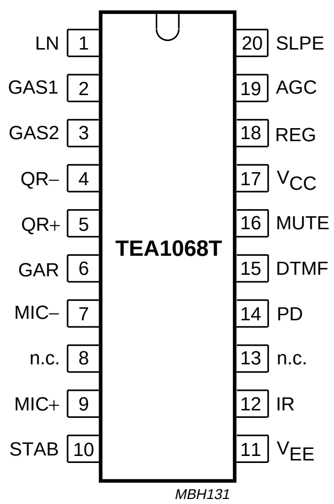


Fig.3 Pin configuration TEA1068T.

FUNCTIONAL DESCRIPTION

Supplies: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1068 and its peripheral circuits is usually obtained from the telephone line. The TEA1068 develops its own supply at V_{CC} and regulates its voltage drop. The supply voltage V may also be used to supply external circuits, e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V ; the internal voltage regulator is decoupled by a capacitor between REG and V .

The DC current flowing into the set is determined by the exchange voltage (V), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

An internal current stabilizer is set by a resistor of 3.6 kΩ between the current stabilizer pin STAB and V_{EE} (see Fig.9).

If the line current I_{line} exceeds the current I + 0.5 mA required by the circuit itself (approximately 1 mA) plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The regulated voltage on the line terminal (V) can be calculated as:

$$V_{LN} = V_{ref} + I \times R9$$

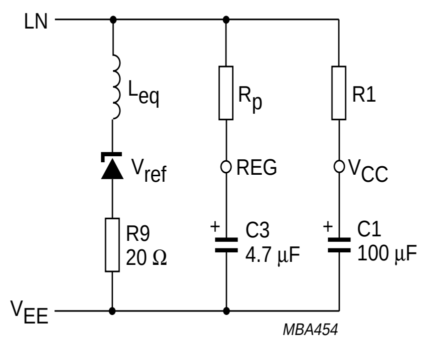
or

$$V = V_{ref} + [(I - I_{CC} - 0.5 \times 10^3) - I\ ] \times R9$$

where V_{ref} is an internally generated temperature compensated reference voltage of 4.2 V and R9 is an external resistor connected between SLPE and V_{EE}. The preferred value for R9 is 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, side-tone level, the maximum output swing on LN and the DC characteristics (especially at lower voltages).

Under normal conditions, when $I_{SLPE} >> I_{CC} + 0.5$ mA + I , the static behaviour of the circuit is that of a 4.2 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range, the dynamic impedance is largely determined by R1 (see Fig.4).

The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor, connected between LN and REG, will decrease the internal reference voltage; when connected between REG and SLPE, it will increase the internal reference voltage. Current (I) available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Figure 10 shows this current for V_{CC} > 2.2 V and for V > 3 V, this being the minimum supply voltage for most CMOS circuits, including voltage drop for an enable diode. If MUTE is LOW, the available current is further reduced when the receiving amplifier is driven.



R_p = 17.5 kΩ
$L_{eq} = C3 \times R9 \times R_p$

Fig.4 Equivalent impedance circuit.

Microphone inputs MIC+ and MIC− and gain adjustment pins GAS1 and GAS2

The TEA1068 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 × 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ; see Fig.14). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used.

The arrangements with the microphone types mentioned are shown in Fig.11.

The gain of the microphone amplifier can be adjusted between 44 dB and 60 dB. The gain is proportional to the value of the external resistor R7 connected between GAS1 and GAS2. An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 × C6.

Mute input (MUTE)

A HIGH level at MUTE enables the DTMF input and inhibits the microphone and the receiving amplifier inputs.

A LOW level or an open circuit has the reverse effect. MUTE switching causes only negligible clicks at the earpiece outputs and on the line.

Dual-Tone Multi Frequency input (DTMF)

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the gain of the microphone amplifier. The signalling tones can be heard in the telephone earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR–. These outputs may be used for single-ended or for differential drive depending on the sensitivity and type of earpiece used (see Fig.12). Gain from IR to QR+ is typically 25 dB (when R4 = 100 kΩ). This is sufficient for low-impedance magnetic or dynamic microphones, which are suited for single-ended drive. By using both outputs (differential drive), the gain is increased by 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω, (high-impedance dynamic or piezoelectric types).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the ratio of peak to RMS value is higher.

The receiving amplifier gain can be adjusted between 17 dB and 33 dB with single-ended drive and between 26 dB and 39 dB with differential drive to suit the sensitivity of the transducer used. The gain is set by the external resistor R4 connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by subtracting the anti-side-tone network attenuation (32 dB) from the amplifier gain. Two external capacitors, C4 = 100 pF and C7 = 10 × C4 = 1 nF, are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The ‘cut-off’ frequency corresponds with the time constant R4 × C4.

Automatic Gain Control input AGC

Automatic line loss compensation is achieved by connecting a resistor R6 between AGC and V_{EE}. This automatic gain control varies the microphone amplifier gain and the receiving amplifier gain in accordance with the DC line current.

The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.13 and Table 1). Different values of R6 give the same ratio of line currents for start and end of the control range. If automatic line loss compensation is not required, AGC may be left open. The amplifiers then all give their maximum gain as specified.

Power-Down input (PD)

During pulse dialling or register recall (timed loop break), the telephone line is interrupted. During these interruptions, the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input, which reduces the typical supply current from 1 mA to 55 µA and switches off the voltage regulator, thus preventing discharge through LN. When PD is HIGH, the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required, PD may be left open-circuit.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3 and Z_{bal} (see Fig.14). Maximum compensation is obtained when the following conditions are fulfilled:

$$R9 \times R2 = R1(R3 + [R8//Z_{bal}]) \qquad (1)$$

$$[Z_{bal} / (Z_{bal} + R8) = Z_{line} / (Z_{line} + R1)] \qquad (2)$$

If fixed values are chosen for R1, R2, R3 and R9, then condition (1) will always be fulfilled, provided that $|R8//Z_{bal}|$ << R3. To obtain optimum side-tone suppression, condition (2) has to be fulfilled, resulting in:

Z_{bal} = (R8/R1) Z_{line} = k × Z_{line}, where k is a scale factor: k = (R8/R1).

Scale factor k (dependent on the value of R8) must be chosen to meet the following criteria:

1. Compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
2. $|Z_{bal}//R8|$ << R3 to fulfil condition (1) and thus ensuring correct anti-side-tone bridge operation
3. $|Z_{bal} + R8|$ >> R9 to avoid influencing the transmitter gain.

In practice, Z_{line} varies greatly with the line length and cable type; consequently, an average value has to be chosen for Z_{bal}, thus giving an optimum setting for short or long lines.

Example: the balanced line impedance (Z_{bal}) at which the optimum suppression is preset can be calculated by:

Assume Z_{line} = 210 Ω + (1265 Ω/140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km). When k = 0.64, then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-side-tone network for the TEA1060 family shown in Fig.5 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier.
The attenuation is almost constant over the whole audio frequency range.

Figure 6 shows a conventional Wheatstone bridge anti-side-tone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

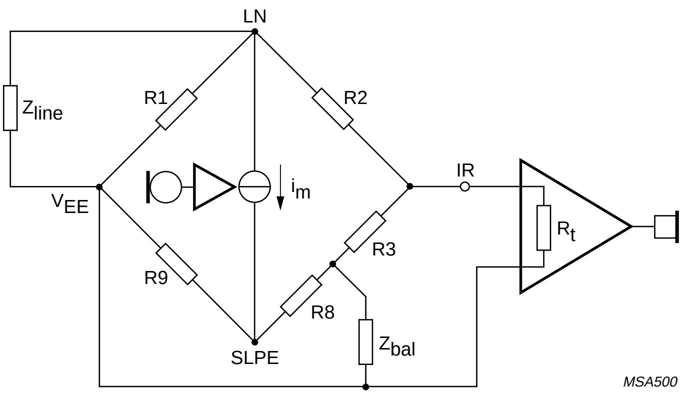


Fig.5 Equivalent circuit of TEA1060 family anti-side-tone bridge.

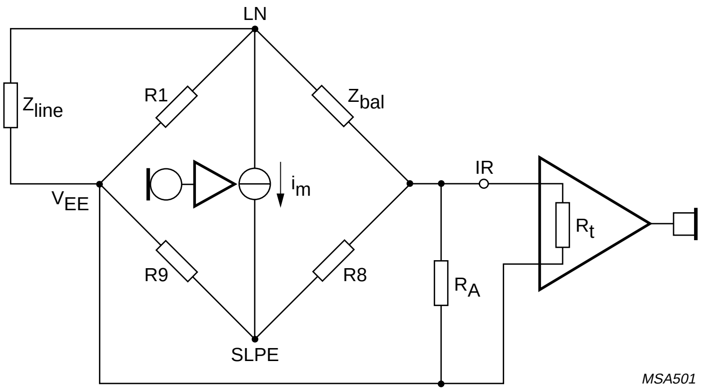


Fig.6 Equivalent circuit of an anti-side-tone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

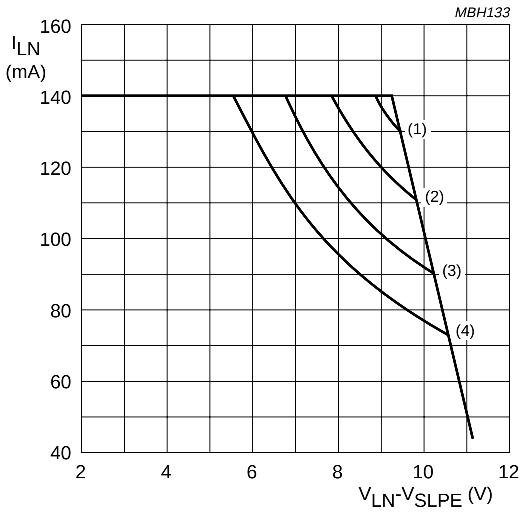
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		–	12	V
$V_{LN(R)}$	repetitive line voltage during switch-on or line interruption		–	13.2	V
$V_{LN(RM)}$	repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; (Fig.15)	–	28	V
I_{line}	line current	R9 = 20 Ω; note 1	–	140	mA
V_n	voltage on any other pin		V_{EE} – 0.7	V_{CC} + 0.7	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1068		–	769	mW
	TEA1068T		–	555	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_j	junction temperature		–	125	°C

Notes

1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 7 and 8 to determine the current as a function of the required voltage and the temperature.
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

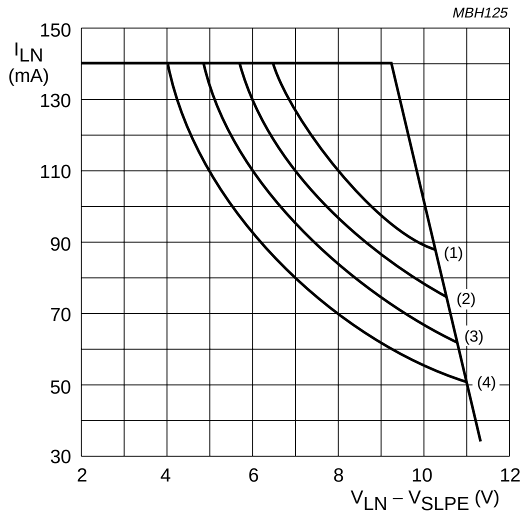
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1068	65	K/W
	TEA1068T	90	K/W



(1) T_{amb} = 45 °C; P_{tot} = 1231 mW.
(2) T_{amb} = 55 °C; P_{tot} = 1077 mW.
(3) T_{amb} = 65 °C; P_{tot} = 923 mW.
(4) T_{amb} = 75 °C; P_{tot} = 769 mW.

Fig.7 Safe operating area TEA1068.



(1) T_{amb} = 45 °C; P_{tot} = 888 mW.
(2) T_{amb} = 55 °C; P_{tot} = 777 mW.
(3) T_{amb} = 65 °C; P_{tot} = 666 mW.
(4) T_{amb} = 75 °C; P_{tot} = 555 mW.

Fig.8 Safe operating area TEA1068T.

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies: LN and V_{CC}						
V_{LN}	voltage drop over circuit between LN and V_{EE}	microphone inputs open				
		I_{line} = 5 mA	3.95	4.25	4.55	V
		I_{line} = 15 mA	4.2	4.45	4.7	V
		I_{line} = 100 mA	5.4	6.1	6.7	V
		I_{line} = 140 mA	–	–	7.5	V
$\Delta V_{LN}/\Delta T$	voltage drop variation with temperature	I_{line} = 15 mA	–4	–2	0	mV/K
V_{LN}	voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA				
		R_{VA} (LN to REG) = 68 kΩ	3.45	3.8	4.1	V
		R_{VA} (REG to SLPE) = 39 kΩ	4.65	5	5.35	V
I_{CC}	supply current	V_{CC} = 2.8 V				
		PD = LOW	–	0.96	1.3	mA
		PD = HIGH	–	55	82	μA
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH				
		I_p = 1.2 mA	2.8	3.05	–	V
		I_p = 0 mA	3.5	3.75	–	V
Microphone inputs MIC+ and MIC–						
$\lvert Z_i \rvert$	input impedance	differential between MIC+ and MIC–	51	64	77	kΩ
		single-ended MIC+ or MIC– to V_{EE}	25.5	32	38.5	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain from MIC+/MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ;	51	52	53	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and f = 3400 Hz	with respect to 800 Hz	–0.5	±0.2	+0.5	dB
ΔG_{vT}	gain variation with temperature at –25 °C and +75 °C	I_{line} = 50 mA; with respect to 25 °C; without R6	–	±0.2	–	dB
Dual-tone multi-frequency input DTMF						
$\lvert Z_i \rvert$	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	24.5	25.5	26.5	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and f = 3400 Hz	with respect to 800 Hz	–0.5	±0.2	+0.5	dB
ΔG_{vT}	gain variation with temperature at T_{amb} = –25 °C and +75 °C	I_{line} = 50 mA; with respect to 25 °C	–	±0.5	–	dB
Gain adjustment connections GAS1 and GAS2						
ΔG_v	gain variation with R7, transmitting amplifier		–8	–	+8	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmitting amplifier output LN						
$V_{LN(rms)}$	output voltage (RMS value)	I_{line} = 15 mA				
		THD = 2%	1.9	2.3	–	V
		THD = 10%	–	2.6	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	–	–72	–	dBmp
Receiving amplifier input IR						
$\|Z_i\|$	input impedance		17	21	25	kΩ
Receiving amplifier outputs QR+ and QR–						
$\|Z_o\|$	output impedance	single ended	–	4	–	Ω
G_v	voltage gain from IR to QR+ or QR–	I_{line} = 15 mA				
		R_L (from QR+ or QR–) = 300 Ω; single-ended	24	25	26	dB
		R_L (from QR+ or QR–) = 600 Ω; differential	30	31	32	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and f = 3400 Hz	with respect to 800 Hz	–0.5	–0.2	0	dB
ΔG_{vT}	gain variation with temperature at T_{amb} = –25 °C and +75 °C	I_{line} = 50 mA; with respect to 25 °C; without R6	–	±0.2	–	dB
$V_{o(rms)}$	output voltage (RMS value)	sine wave drive; I_{line} = 15 mA; I_p = 0 mA; THD = 2%; R4 = 100 kΩ				
		single-ended; R_L = 150 Ω	0.3	0.38	–	V
		single-ended; R_L = 450 Ω	0.4	0.52	–	V
		differential; f = 3400 Hz; R_{series} = 100 Ω; C_L = 47 nF	0.8	1.0	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted (P53 curve)				
		single-ended; R_L = 300 Ω	–	50	–	μV
		differential; R_L = 600 Ω	–	100	–	μV
Gain adjustment GAR						
ΔG_v	gain variation of receiving amplifier achievable by varying R4 between GAR and QR		–8	–	+8	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE input						
V_{IH}	HIGH level input voltage		1.5	–	V_{CC}	V
V_{IL}	LOW level input voltage		–	–	0.3	V
I_{MUTE}	input current		–	8	15	µA
ΔG_v	voltage gain reduction between MIC+ and MIC– to LN	MUTE = HIGH	–	70	–	dB
G_v	voltage gain from DTMF to QR+ or QR–	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	–21	–19	–17	dB
Power-Down input PD						
V_{IH}	HIGH level input voltage		1.5	–	V_{CC}	V
V_{IL}	LOW level input voltage		–	–	0.3	V
I_{pd}	input current in power-down condition		–	5	10	µA
Automatic Gain Control input AGC						
ΔG_v	gain control range from IR to QR+/QR– and from MIC+/MIC– to LN	I_{line} = 70 mA; R6 = 110 kΩ between AGC and V_{EE}	–5.5	–5.9	–6.3	dB
$I_{line(H)}$	highest line current for maximum gain	R6 = 110 kΩ between AGC and V_{EE}	–	23	–	mA
$I_{line(L)}$	lowest line current for minimum gain	R6 = 110 kΩ between AGC and V_{EE}	–	61	–	mA
ΔG_v	voltage gain variation	between I_{line} = 15 mA and I_{line} = 35 mA; R6 = 110 kΩ between AGC and V_{EE}	–1.0	–1.5	–2.0	dB

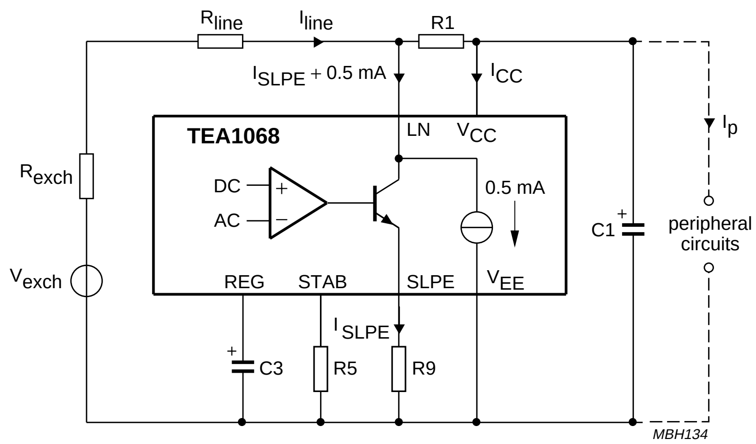
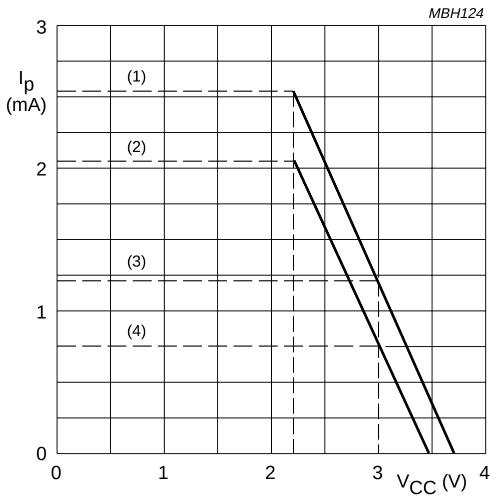


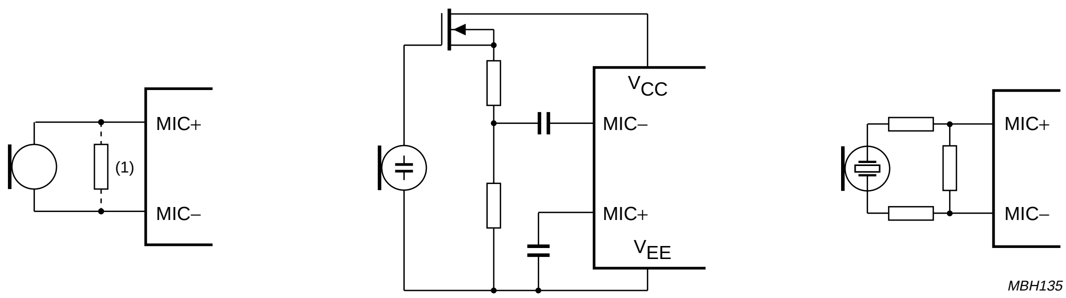
Fig.9 Supply arrangement.



Curve (1) is valid when the receiving amplifier is not driven or when MUTE = HIGH. Curve (2) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)}$ = 150 mV; R_L = 150 Ω asymmetrical.

The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

Fig.10 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} \geq 2.2$ V.



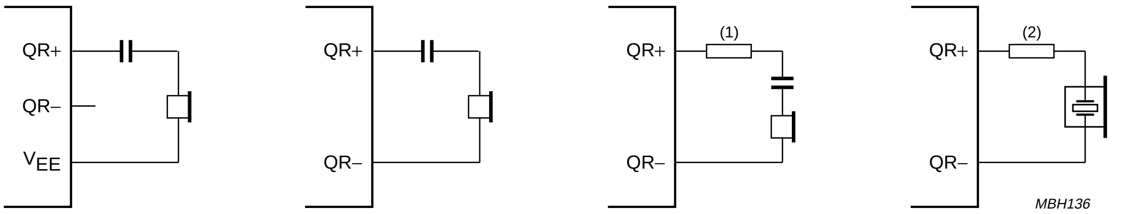
a. Magnetic or dynamic microphone.

b. Electret microphone.

c. Piezoelectric microphone.

(1) May be connected to decrease the terminating impedance.

Fig.11 Alternative microphone arrangements.



a. Dynamic earpiece with less than 450 Ω impedance.

b. Dynamic earpiece with more than 450 Ω impedance.

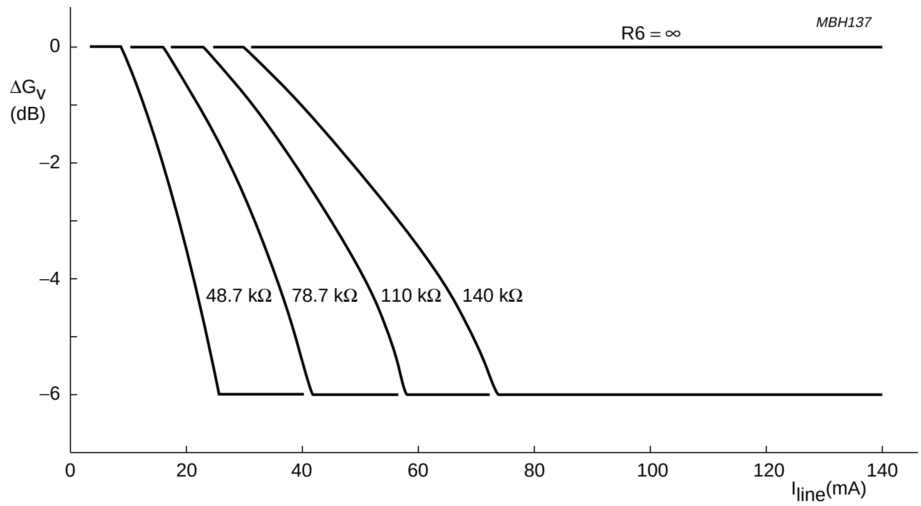
c. Magnetic earpiece with more than 450 Ω impedance.

d. Piezoelectric earpiece.

(1) May be connected to prevent distortion (inductive load).

(2) Required to increase the phase margin (capacitive load).

Fig.12 Alternative receiver arrangements.

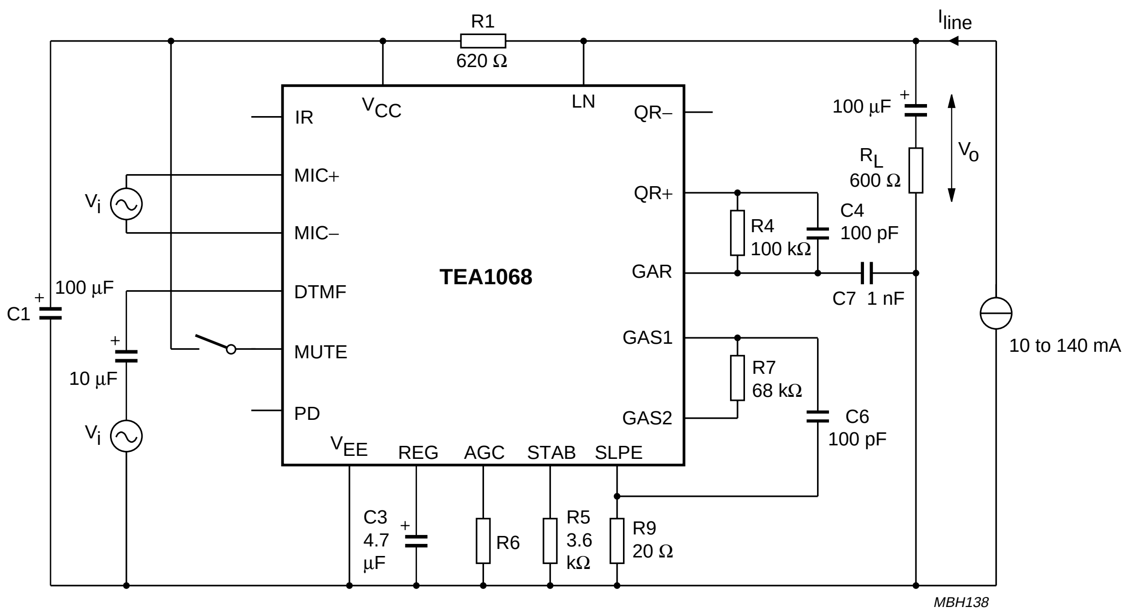


R9 = 20 Ω.

Fig.13 Variation of gain with line current, with R6 as a parameter.

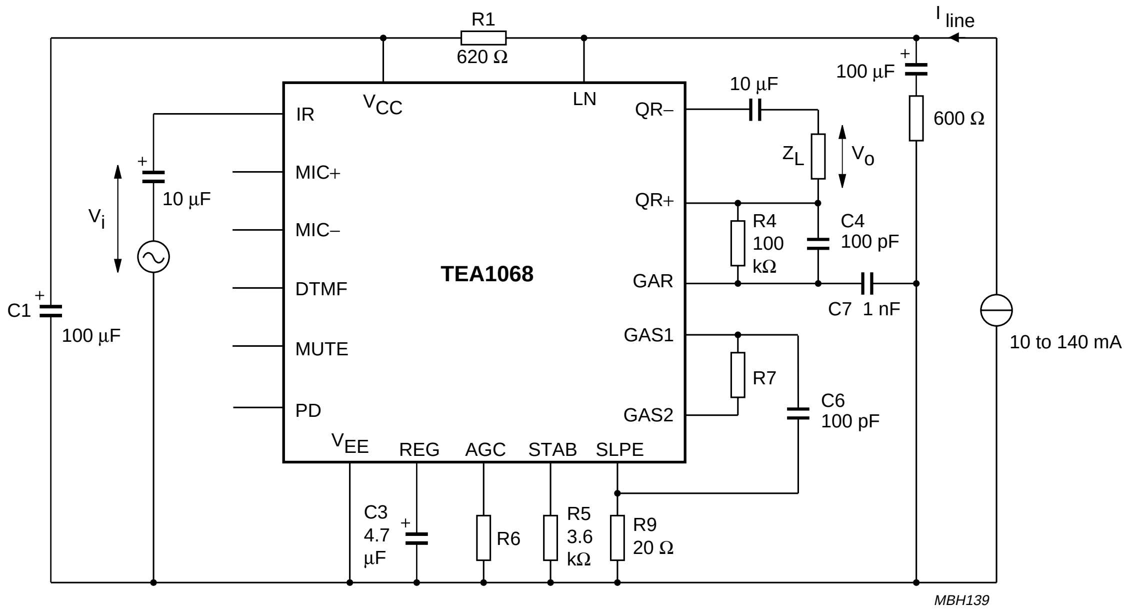
Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω

V_{exch} (V)	R6 (kΩ)			
	R_{exch} = 400 Ω	R_{exch} = 600 Ω	R_{exch} = 800 Ω	R_{exch} = 1000 Ω
24	61.9	48.7	X	X
36	100	78.7	68	60.4
48	140	110	93.1	82
60	X	X	120	102



Voltage gain is defined as; $G_v = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC−, the MUTE input should be LOW or open, for measuring the DTMF input, MUTE should be HIGH. Inputs not under test should be open.

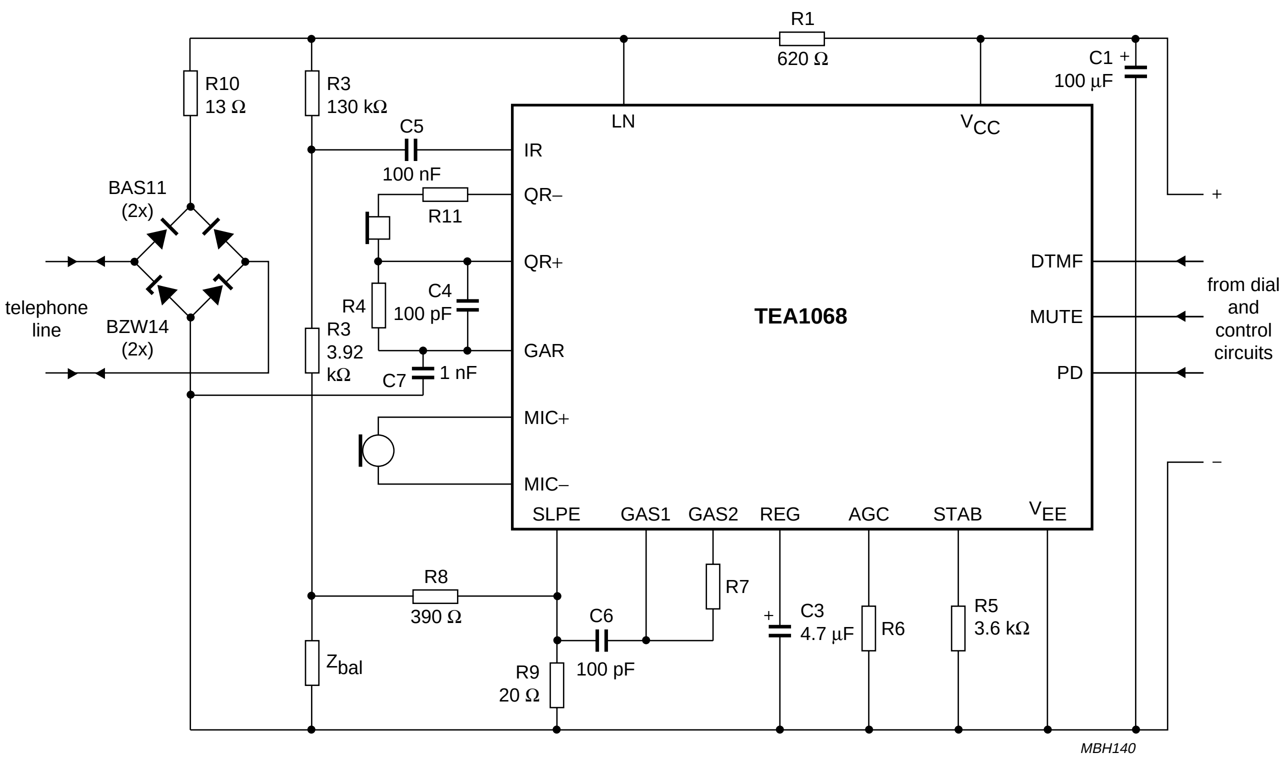
Fig.14 Test circuit for defining voltage gain of MIC+, MIC− and DTMF inputs.



Voltage gain is defined as; $G_v = 20 \log |V_o/V_i|$.

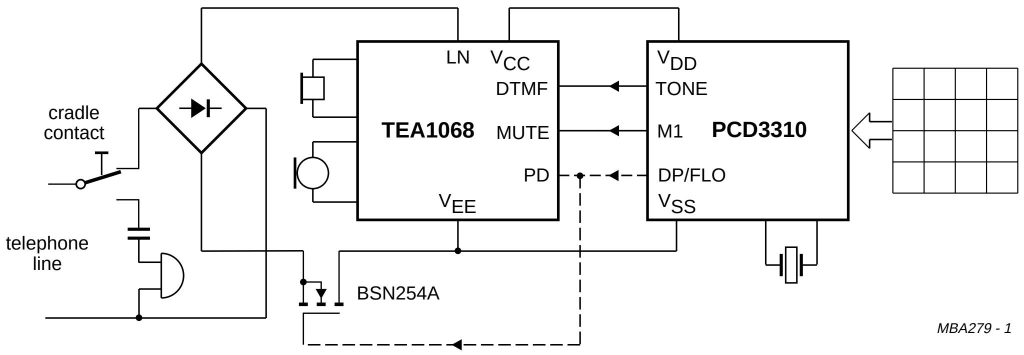
Fig.15 Test circuit for defining voltage gain of the receiving amplifier.

APPLICATION INFORMATION



Typical application of the TEA1068, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

Fig.16 Application diagram.

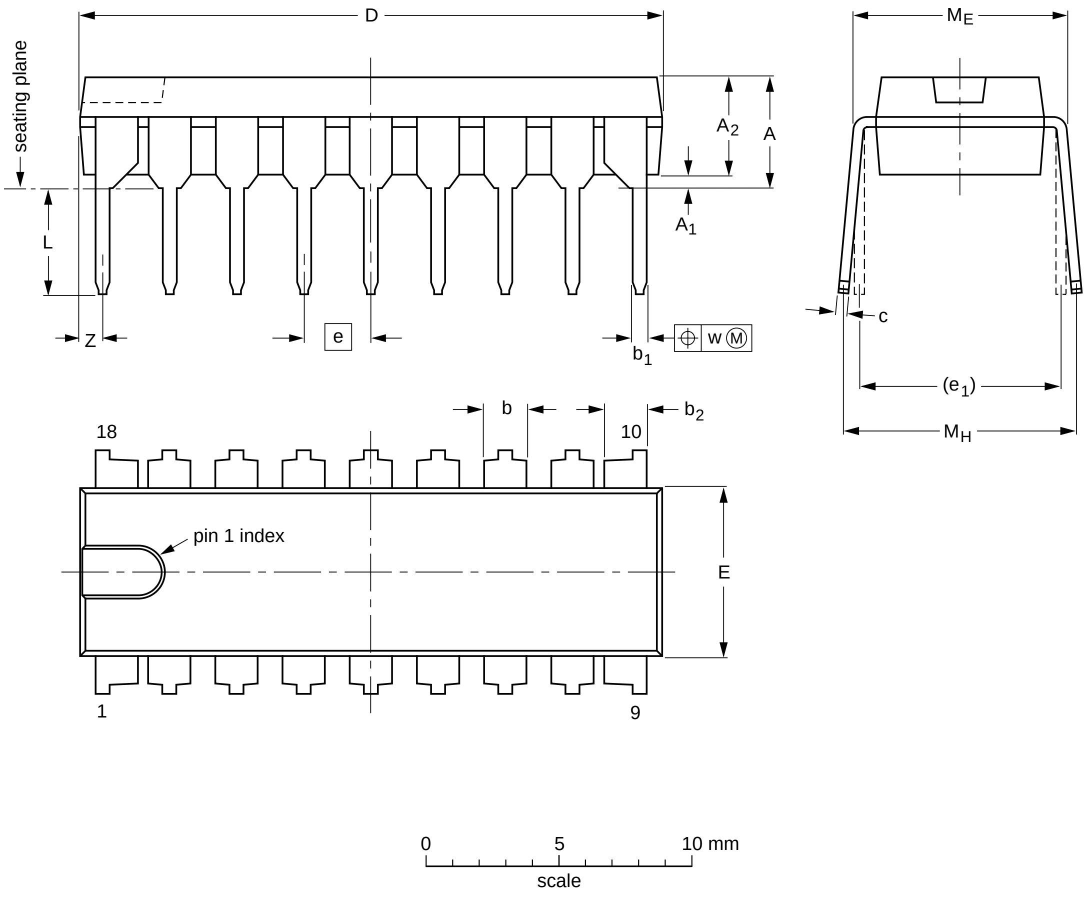


The dashed lines show an optional flash (register recall by timed loop break).

Fig.17 DTMF set with a CMOS DTMF dialling circuit.

PACKAGE OUTLINES

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

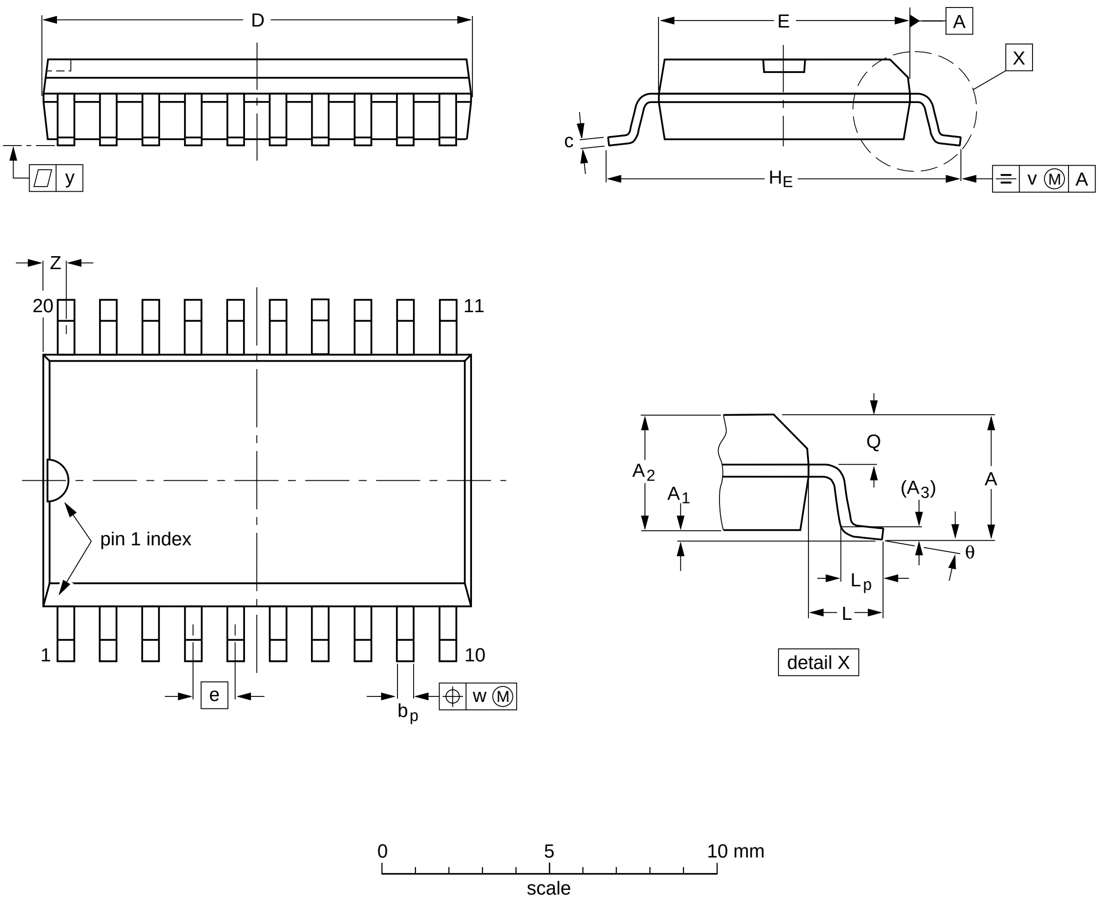
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D [(1)]	E [(1)]	e	e_1	L	M_E	M_H	w	Z [(1)] max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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