SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2028 - TEA2029

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SUMMARY

Page

TEA2028

TEA2029

I - GENERAL DESCRIPTION

As depicted in Figure 1, the TEA2028 combines 3 major functions of a TV set as follows :

- Horizontal (line) and vertical (frame) time base generation for spot deviation. The video signal is used for the synchronization of both time bases.
- On-chip switching power supply controller synchronized on line frequency.

This integrated circuit has been implemented in bipolar I^2L technology, and various functions are digitally processed. In fact, resorting to logic functions has the advantage of working with pure and accurate signals while full benefit is drawn from high integration of logic gates (approx. 110 gates per mm^2).

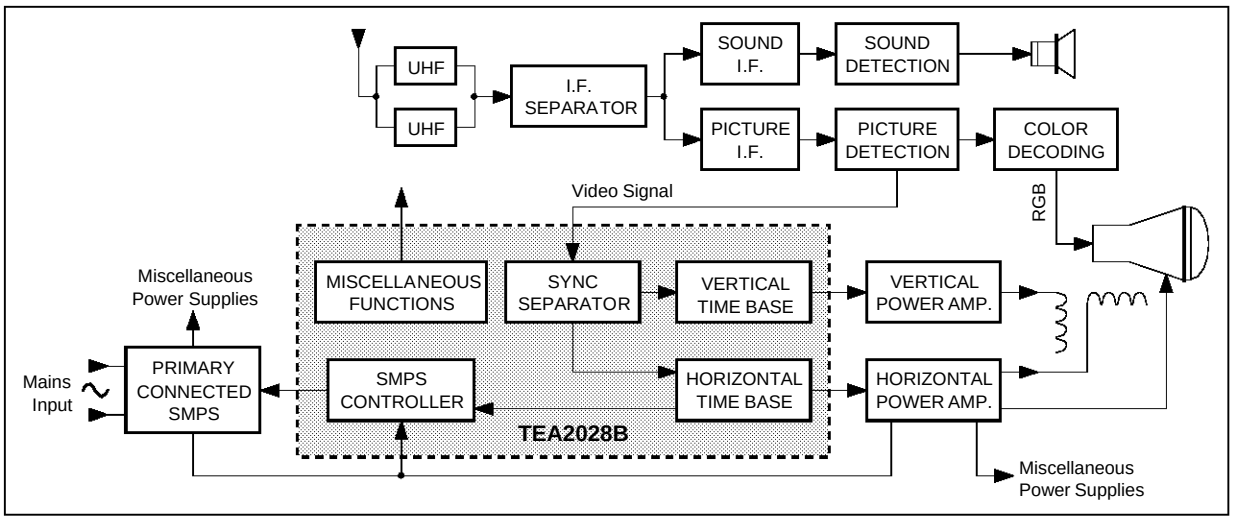
The main objective is to drive all functions using an accurate time base generated by a master 500kHz oscillator.

Also, horizontal and vertical time bases, are obtained by binary division of reference frequency. This has the advantage of eliminating the 2 adjustments which were necessary in former devices.

One section of this integrated circuit is designed to drive a switching power supply of recent implementation called ”master-slave”. Switching takes place on the primary side (i.e., directly on mains) of a transformer. The device ensures **SMPS Control**, **Start-up** and **Protection** functions. Control signals go through a small pulse transformer thereby providing full isolation from mains supply.

This new approach fully eliminates the bulky mains transformers used in the past. In addition, it offers optimized power consumption and reduction of TV cost-price.

Figure 1



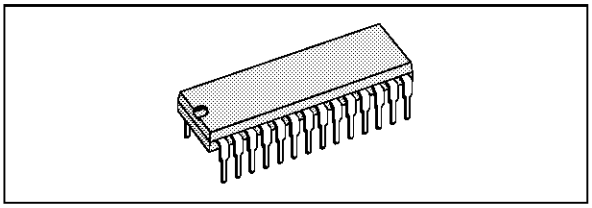
II - MAIN FUNCTIONS

- Detection and extraction of line and frame synchronization pulses from the composite video signal.
- Horizontal scanning control and synchronization by two phase-locked loop devices.
- Video identification.
- 50 or 60Hz standard recognition for vertical scanning.
- Generation of a self-synchronized frame sawtooth for 50/60Hz standards.
- Line time constant switching for VCR operation through an input labeled "VCR" (Video Cassette Recorder).
- Control and regulation of a primary-connected switching power supply by on-chip controller device combining :
  - an error amplifier
  - a pulse width modulator synchronized on line frequency
  - a start-up and protection system
- Overall TV set protection input
- Frame blanking and super sandcastle output signals
- Frame blanking safety input for CRT protection in case of vertical stage failure.

III - PIN CONNECTIONS

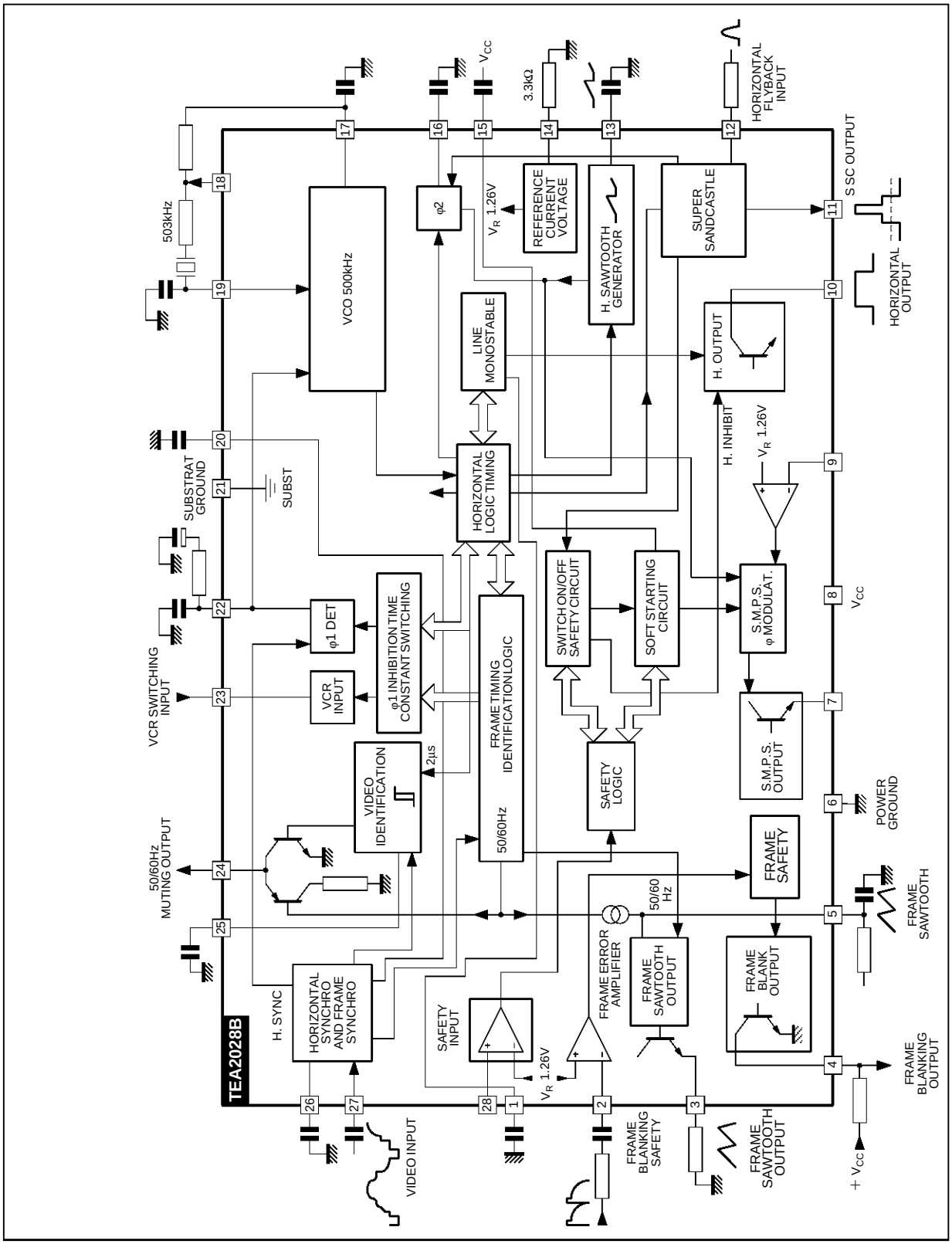
Pin	Description
1	Horizontal output monostable capacitor
2	Frame blanking safety input
3	Frame saw-tooth output
4	Frame blanking output
5	Frame ramp generator
6	Power ground
7	SMPS control output
8	Supply voltage (V_{CC})
9	SMPS regulation input
10	Horizontal output
11	Super-sandcastle output
12	Horizontal flyback input
13	Horizontal saw-tooth generator
14	Current reference
15	SMPS soft-start and safety time constant capacitor
16	ϕ2 phase comparator capacitor (and horizontal phase adjustment)
17	V_{CO} phase shift network
18	V_{CO} output
19	V_{CO} input
20	Frame sync time constant adjustment capacitor
21	Substrate Ground
22	ϕ1 phase comparator capacitor
23	VCR switching input
24	Video and 50/60Hz identification output (Mute)
25	Video identification capacitor
26	Horizontal sync detection capacitor (50% of peak to peak sync level)
27	Video input
28	Safety input

Package : DIP28



IV - INTERNAL BLOCK DIAGRAM

Figure 2



V - FUNCTIONAL DESCRIPTION

Majority of the on-chip analog functions were computer simulated and results such as temperature variation, technological characteristic dispersion and stability, have led to the enhancement and implementation of actually employed structures. A parallel in-depth study of the device implemented in form of integrated sub-sections is provided to analyze the overall performance in a TV set.

V.1 - Internal Voltage and Current References

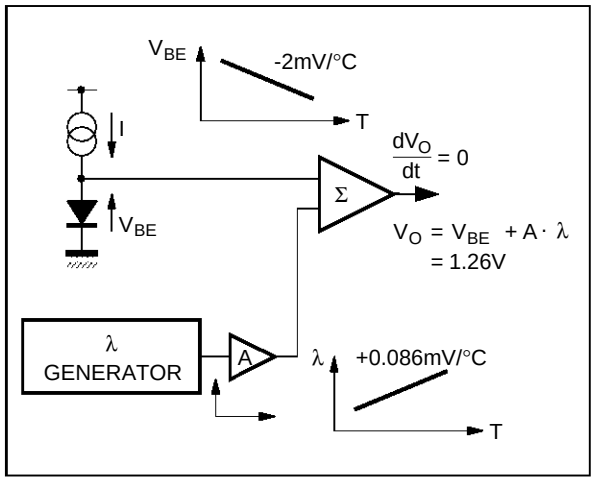
V.1.1 - 1.26V Voltage reference

For optimum operation of the device, an accurate and temperature-stable voltage generator independent from V_{CC} variations is used (Band-gap type generator).

The generated 1.26V is particularly used as reference setting on input comparators.

V.1.1.1 - Generator block diagram

Figure 3



2028B-06.EPS

$$\text{with } \lambda = \frac{K \cdot T}{q} = 25.7\text{mV at } +25^{o}\text{C}$$

$$\frac{d\lambda}{dT} = \frac{K}{q} = +\,0.086\text{mV}/^{o}\text{C}$$

$$\frac{dV_{BE}}{dT} = \frac{V_{BE(25')} - 1.26}{T} = -\,2\text{mV}/^{o}\text{C}$$

if $A\lambda = 1.26 - V_{BE}$

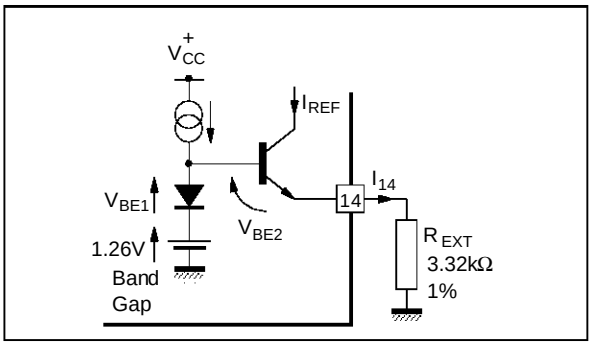
Then : $V_O = 1.26$V (temperature-independant)

In practice, maximum drift due to temperature can be + 0.23mV/°C
i.e., ± 1.5% for a ΔT of 80°C.

V.1.2 - Current reference

This is implemented using the 1.26V generator in combination with an external resistor.

Figure 4



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$$I_{REF} \approx I_{14} = \frac{V_{14}}{R_{EXT}} = \frac{1.26 + V_{BE1} - V_{BE2}}{R_{EXY}}$$

Let's $I_{14} = I$ and $V_{EB1} = V_{BE2}$

then : $I_{REF} = \frac{1.26}{R_{EXT}} = 380\mu\text{A}$

Thus, it follows that I_{REF} is accurate and independent of both V_{CC} and temperature.

A set of current generators proportional to I_{REF} current are used in various circuit blocks.

V.2 - Line Sync. Extraction

Horizontal and vertical time bases should be synchronized with corresponding sync. pulses transmitted inside the infra-black portion of video signal. The duty of this stage is to extract these sync pulses. The output signal, called composite sync, contains the vertical sync which is transmitted by simple inversion of line sync. pulses.

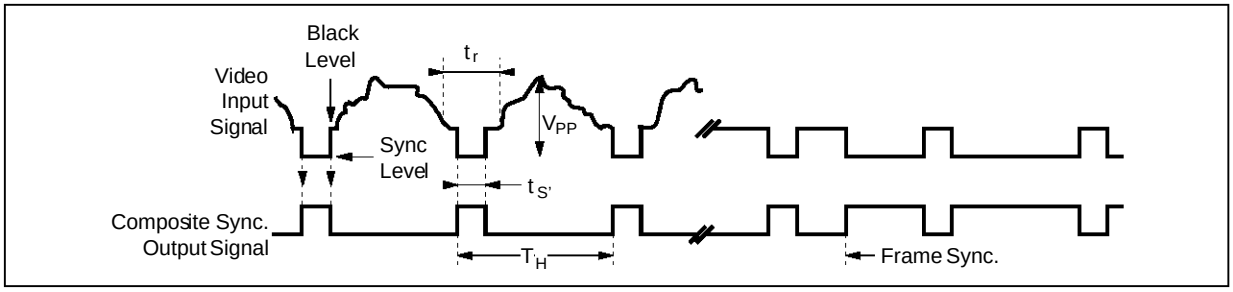
The vertical sync pulse is then extracted from this composite signal.

The main advantage of this arrangement is its ability to operate at video input signal levels falling within 0.2V to 3V peak-to-peak range and at any average value.

The operating principle is to lock the black level of the input signal (Pin 27) onto internaly fixed voltage (V_N) and then memorize the average voltage of the sync pulse by using an integrating capacitor connected to Pin 26.

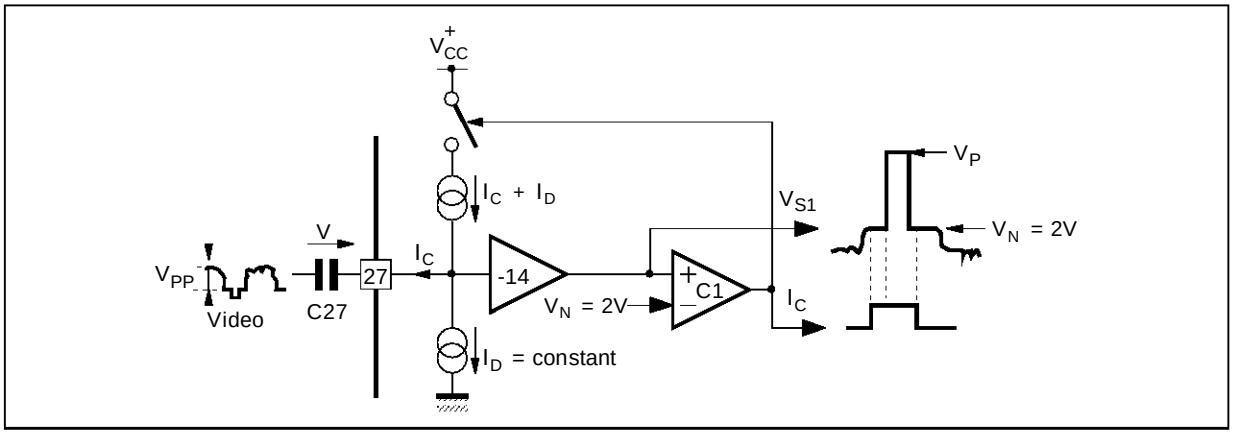
Finally, the composite sync signal is delivered by a comparator the inputs of which are driven by $V_{50\%}$ and video signals.

Figure 5



V.2.1 - Black level locking

Figure 6

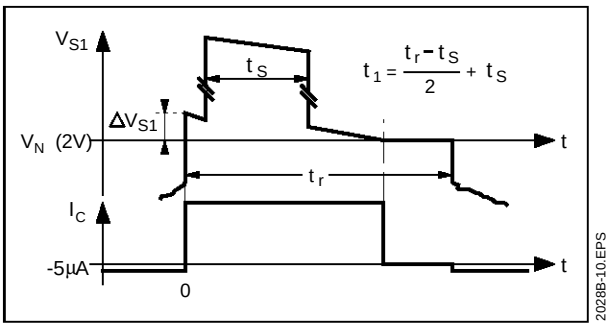


The video signal is applied to Pin 27 through the coupling capacitor "C27". Since the sync pulse amplitude is generally equal to 1/3 of V_{PP} (i.e. 66mV to 1V) and in order to obtain a good precision of the black level, the sync pulse should be amplified by a coefficient of - 14 before being applied to the comparator "C1".

This comparator will charge the "C27" capacitor as long as $V_{S1} > V_N \cdot V_{S1}$ will stabilize at V_N during the line flyback interval "T_r" if the average charge of "C27" capacitor is nil for one T_H period.

I_C/I_D is calculated such that the locking occurs at the middle of the back porch.

Figure 7



The ΔV_{S1} produced by I_D during the line trace which is : $14 \cdot \frac{I_D \cdot t_A}{C27}$

must be equal to ΔV_{S1} during the time interval "t1", i.e. : $14 \cdot \frac{I_C \cdot t_1}{C27}$

It follows that : $\frac{I_C}{I_D} = \frac{t_A}{t_1} = \frac{T_H - t_R}{t_S + \frac{t_R - t_S}{2}}$

substituting $T_H = 64\,\mu s$, $t_r = 12\,\mu s$, $t_S = 4.7\,\mu s$ (which are standard and constant values) into above equation : $\frac{I_C}{I_D} = 6.23V$

V.2.1.1 - Application

At $I_C = 5\mu A \Rightarrow I_D = 31\mu A$

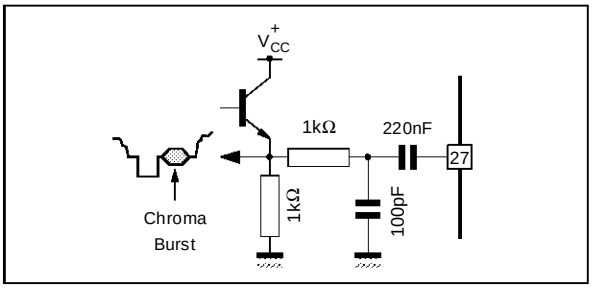
- With C27 = 220nF, ΔV_S will be

$$14 \cdot \frac{5 \cdot 52}{220} = 16mV$$

  which yields 0.8% maximum error in black level with respect to $V_N = 2V$ at the beginning of retrace time
- Due to transposition on amplifier stage, the black level voltage on Pin 27 is equal to 2V.

- In practice, at low amplitude video signals, it is recommended to insert a low-pass filter before the "C27" capacitor so as to attenuate the chrominance sub-carrier and the noise components. The aim is to reduce the phase variations of the detected sync pulse and thus enhance the horizontal scanning stability.

Figure 8



V.2.2 - Memorizing the sync pulse 50% value

The objective is to memorize the voltage corresponding to 50% of the line sync pulse V_{S1} by using an external capacitor connected to Pin 26 (see Figure 9).

The overall arrangement comprises two comparators.

- Comparator C2 : delivers an output voltage "V1" by comparing $V_{S1} + V_D$, V_{26} and the voltage drop across two resistors.
- Comparator C3 : which delivers a constant output current thereby maintaining on capacitor "C26", the voltage $V_{50\%}$ corresponding to 50% of peak to peak sync pulse.

During the line scanning, diode "D" is reverse biased : $V_{S1} + V_D = V_1 < V_{26}$ and C3 will deliver a current I_D which will discharge the capacitor.

During sync pulse interval, $V_{S1} + V_D = V_P + V_D$, diode "D" begins conducting and thus :
$V_1 = (V_P + V_D) - (2\ R\ i_1)$. Since the capacitor has been slightly discharged $\Rightarrow V_1 > V_{26}$, comparator C3 begins charging the capacitor until C2 is brought to equilibrium.

At this time, $I_1 = \frac{i}{2}$ where $i = \frac{V_{26} - V_D - V_N}{R}$

thus $V_1 = V_P + V_D = 2\frac{i}{2} = V_P + V_N + 2\ V_D - V_{26}$

and $V_1 = V_{26} \Leftrightarrow V_{26} = \frac{V_P + V_N}{2} + V_D = V_{50\%}$

A high value C26 capacitor will thus memorize the voltage level corresponding to 50% of the line sync. pulse.

V.2.2.1 - $\frac{I_C}{I_D}$ Ratio calculation

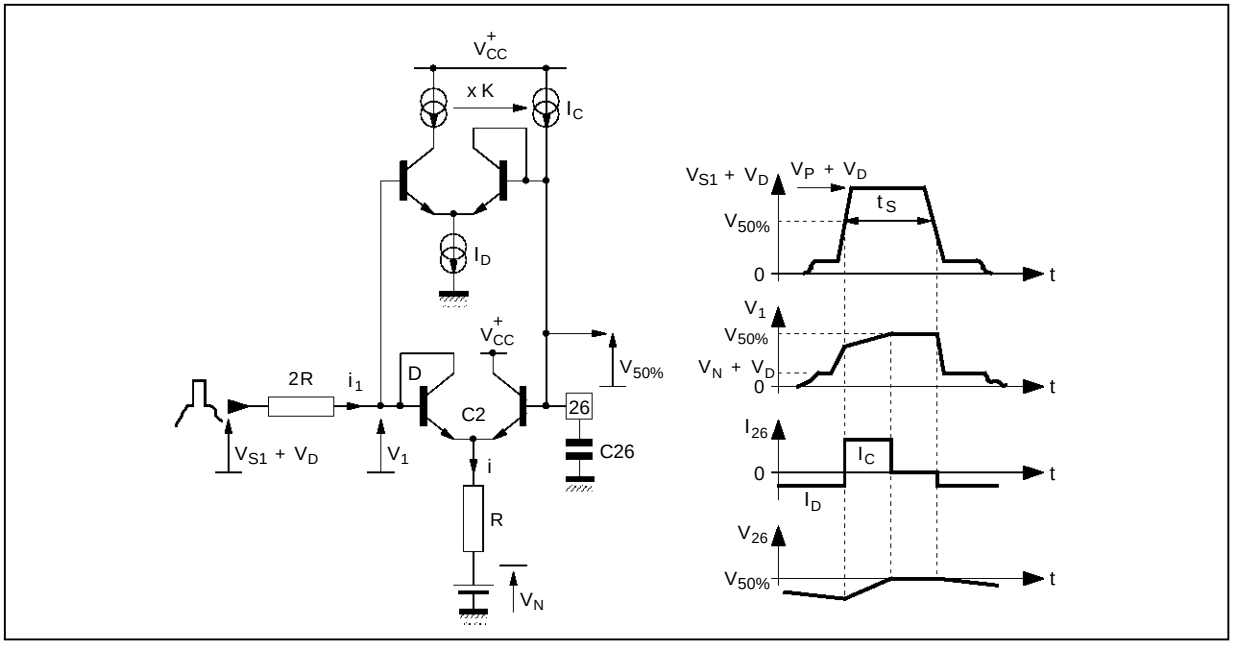
During the line scanning period (T_H - T_S), the capacitor C26 will loose a charge equivalent to : $I_D\ (T_H - T_S)$.

This energy must be recovered before the end of sync pulse such that : $I_C \cdot t_S > I_D\ (T_H - T_S)$

therefore $\frac{I_C}{I_D} > \frac{T_H - t_S}{t_S}$ $\quad \frac{I_C}{I_D} > 12.6$

In practice, for C26 = 100nF, I_D = 25µA and I_C = 800µA.

Figure 9



V.2.3 - Sync pulse detection

This function is fulfilled by comparing the inverted video signal (V_{S1} + V_D) whose black level is constant at 2V, with the sync 50% voltage level on Pin 26 (see Figure 10).

Comparator C4 will deliver the line sync pulse (LS) which will be used for 3 functions :

- Horizontal scanning frequency locking : output to φ1 phase comparator.
- Frame sync extraction for vertical scanning synchronization.
- Detecting the presence of a video signal at circuit input.

The LS signal in two latter functions is filtered for noise by using combination of current generator I and a zener diode equivalent to a capacitor.

Using this extraction technique at a very noisy video signal yields remarkable display stability.

The device also provides for scanning synchronization at aerial signal attenuation of approximately 75dB, i.e. 15 to 20dB better than other sync processors.

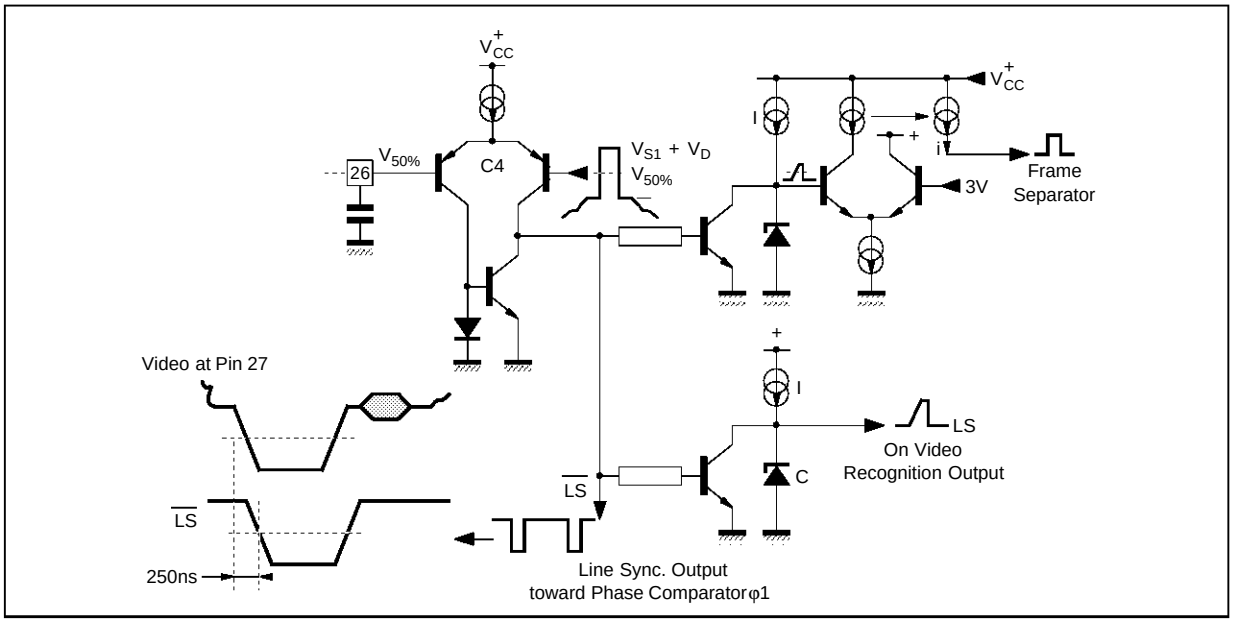
V.3 - First Phase Locked-loop Stage "φ1"

This stage is commonly called the first Phase Locked-Loop "φ1".

Its duty is to lock the frequency and the phase of the horizontal time base with respect to the line sync signal.

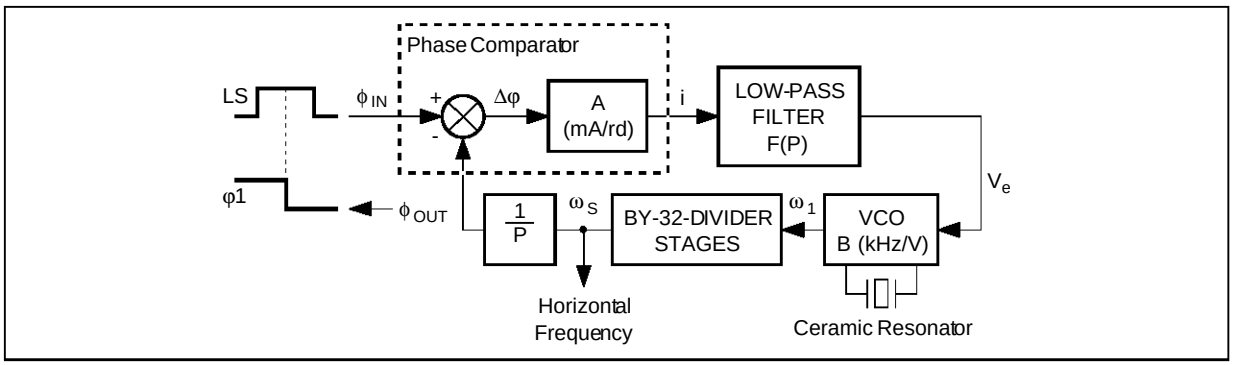
In the absence of transmission (i.e. lack of line sync), the horizontal scanning frequency is obtained by dividing the output frequency of a VCO device. This VCO oscillates at approximately 500kHz and uses a low frequency drift ceramic resonator. This method eliminates the need of horizontal frequency adjustment.

Figure 10



V.3.1 - Phase locked-loop "φ1" block diagram

Figure 11



V.3.2 - Functional duty of individual blocks

V.3.2.1 - Phase comparator

The duty of this comparator is to issue an output current proportional to the phase difference between ϕ_{IN} and ϕ_{OUT}.

V.3.2.2 - Low-pass filter

This filter suppresses the parasitic component containing the sum of phases, smoothens the phase difference component and determines the timing characteristics of the loop.

V.3.2.3 - VCO centered on 500kHz

This is a voltage-controlled oscillator which generates an output frequency proportional to the voltage applied to its input.
This voltage is delivered by low-pass filter.

V.3.2.4 - Divider stage

It is used to divide the VCO frequency (500kHz) by 32 so that it can be compared with the line sync signal frequency of 15625Hz.

V.3.3 - Functional description of building blocks

V.3.3.1 - Phase comparator "ϕ1"

The comparator is functionally equivalent to a signal multiplier (see Figure 12).

Let's assume that :

- $i_{LS} = I \sin(\omega_H t + \phi_{IN})$ and $V_{\phi 1} = k \cos(\omega_H t + \phi_{OUT})$

then :

- $i = \frac{i_{LS} \cdot k}{2} [\sin(\Phi_{IN} - \Phi_{OUT}) + \sin(2\omega_H t + \Phi_{IN} + \Phi_{OUT})]$
  (see Figure 13)
- the low-pass filter will suppress the $2f_H$ frequency component
- $\phi_{IN} - \phi_{OUT}$ difference being low :
  $\sin(\phi_{IN} - \phi_{OUT}) \approx \phi_{IN} - \phi_{OUT}$
- the output current will be therefore proportional to the phase difference between the signals compared.

In other words, the average current over one period is :

$$I_{AV} \cdot T_H = I\left(\frac{t_S}{2} + \Delta t\right) - I\left(\frac{t_S}{2} - \Delta t\right) = 2I\,\Delta t$$

$$I_{AV} = 2I\frac{\Delta t}{T_H} \text{ and } \Delta t = \Delta\Phi\frac{T_H}{2\pi}$$

The comparator conversion gain is thus :

$$A = \frac{i}{\Delta\Phi} = \frac{I}{\pi} \text{ (in A/rd)}$$

Later in our discussion we shall consider the two possible values of the current I.

For the time being, let's define these values as follows :

- I = 500µA for "long time constant" or normal operation
- I = 1.5mA for "short time constant" VCR mode or synchronization search (Mute).

The values of A are therefore :

- A_{LONG} = 0.16mA/rd
- A_{SHORT} = 0.47mA/rd

Use of comparator inhibition signal is quite useful under noisy transmission conditions. It eliminates risk of incorrect comparison during the line scanning phase which would be due to the noise present on LS signal. Horizontal phase and image stability are thus highly enhanced.
Characteristics of this inhibition signal will be discussed at the end of this chapter.

Figure 12

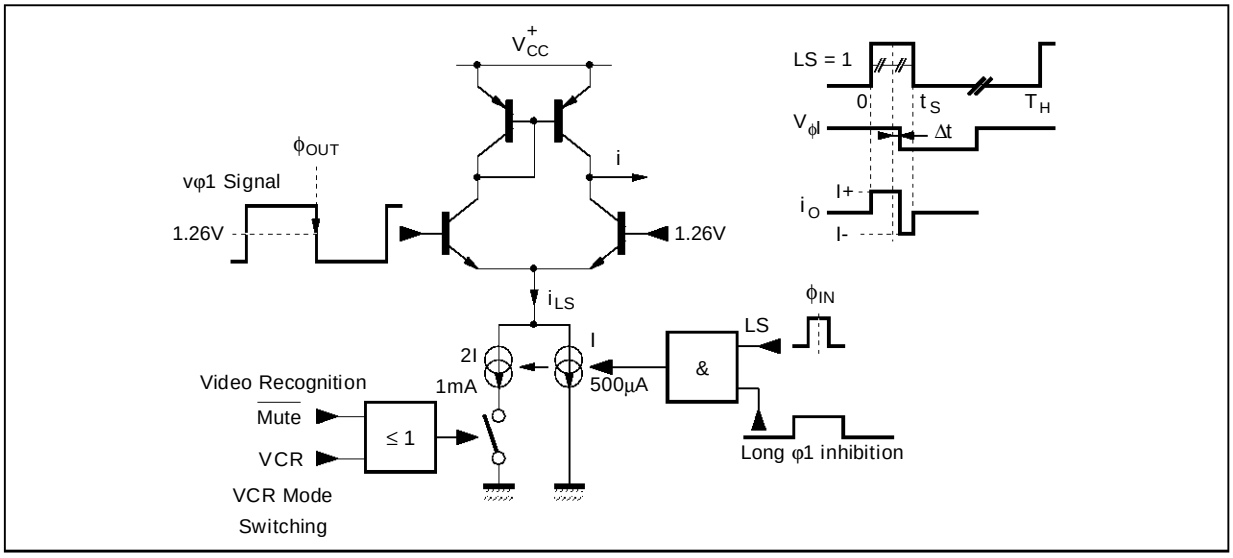
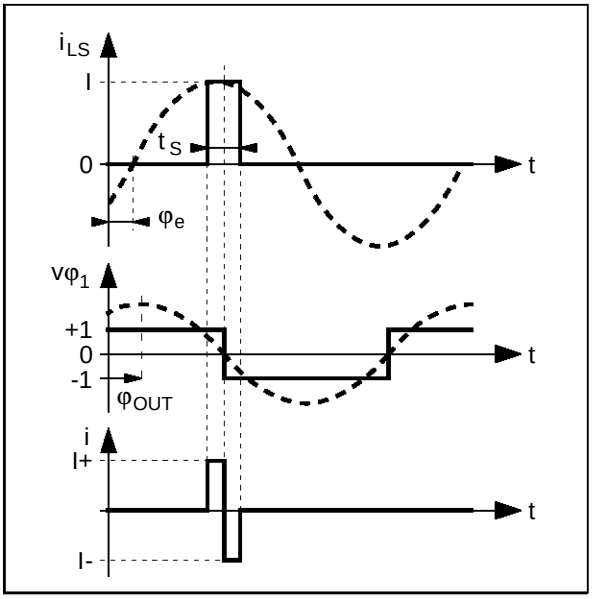


Figure 13



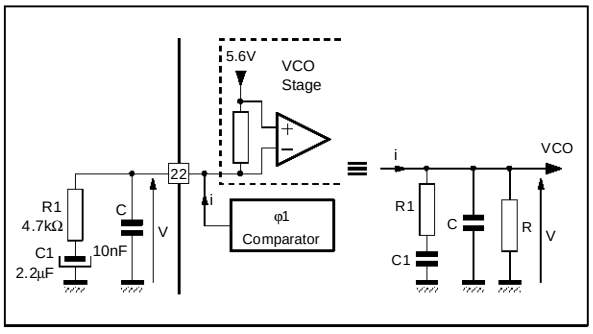
V.3.3.2 - Low-pass filter (see Figure 14)

Its main function is to reject the $2f_H$ (31kHz) frequency component delivered by the phase comparator.

It also defines the characteristics of the loop in transient mode.

The filter is built around two sub-sections which determine the stability and the response time of the loop in the following modes of transmission :
Normal or VCR modes. See section V.3.6 "Dynamic study of ϕ1".

Figure 14



R is the dynamic input resistance of the VCO.

The filter transfer function may be defined as follows :

- $f(p) = \frac{V}{i} = Z(p)$
- $Z(p) = R\frac{1 + R1\,C1\,p}{1 + p\,(R\,C + R1\,C1 + R\,C1) + R\,R1\,C\,C1\,p^2}$

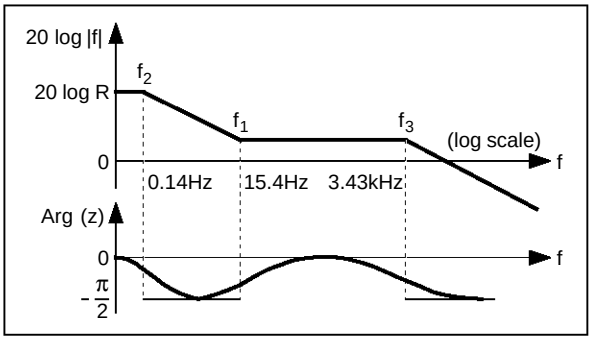
The second order terms of the denominator can be converted to first order products as a function of frequency as follow :

$$f(jf) = R\,\frac{1 + j\frac{f}{f1}}{\left(1 + j\frac{f}{f2}\right)\left(1 + j\frac{f}{f3}\right)}$$

with R1 = 4.7kΩ, R = 500kΩ, C1 = 2.2µF, C = 10nF we obtain :

- $f1 = \frac{1}{2\pi\,R1\,C1} = 15.4Hz$
- $f2 = \frac{1}{2\pi\,(R\,C1 + R\,C + R1\,C1)} = 0.14Hz$
- f3 = 3.43kHz

Figure 15



V.3.3.3 - VCO (Voltage Controlled Oscillator)

Its function is to generate a frequency proportional to a control voltage issued externally, by the low-pass filter in our case.

The period of the output signal is used as timing reference for various functions such as, horizontal and vertical time bases. The frequency range must be short and accurate :

- It must be short since the power dissipated within the horizontal scanning block is inversely proportional to the line frequency.
- The accuracy is required if the adjustment is to be omitted.

The basic arrangement is to employ a ceramic resonator (or ceramic filter) which has quite stable characteristics as a function of frequency.

A filter whose resonating frequency is a multiple of line frequency (15625Hz) is to be selected. An example is 32 · 15625 = 500kHz.

A. 503kHz CERAMIC FILTER

Figure 16

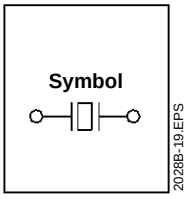
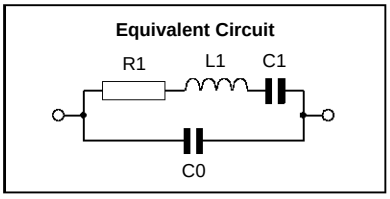


Figure 17



Where :
R1 = 7Ω, L1 = 1.26mH, C1 = 78pF, C0 = 507pF
- Series resonance frequency :

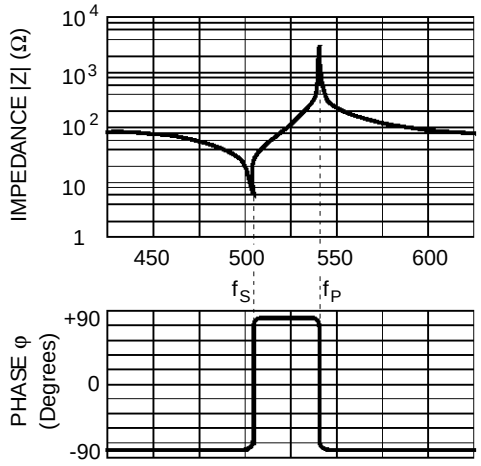
$$f_S = \frac{1}{2\pi\sqrt{L1\,C1}} = 503kHz$$

- Parallel resonance frequency :

$$f_P = f_S \cdot \sqrt{1 + \frac{C1}{C0}} = 540kHz$$

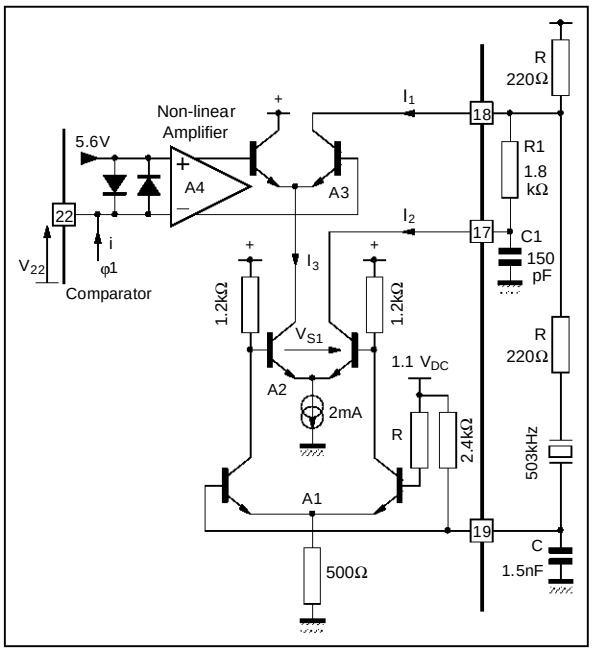
- Tolerance within the resonance area : 503kHz ± 0.3 %
- Temperature stability : ± 0.3% of f_O at $\Delta T = 100^oC$

Figure 18



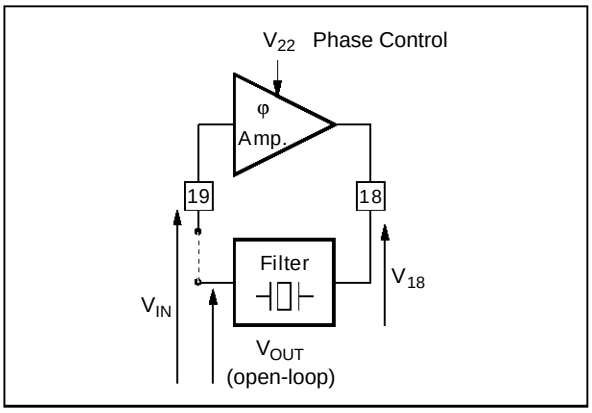
B - SIMPLIFIED BLOCK DIAGRAM OF VCO

Figure 19



The overall arrangement is equivalent to a variable-phase amplifier configured in closed loop with the external passive filter.
The system will oscillate if the open-loop gain is 0dB and if V_{OUT} leads V_{IN}.
In closed-loop oscillating mode, the phase variation of V_{18}/V_{IN} imposed by V_{22} will result in same V_{OUT}/V_{18} variation but of opposite sign.
This phase change will finally correspond to a change in frequency.

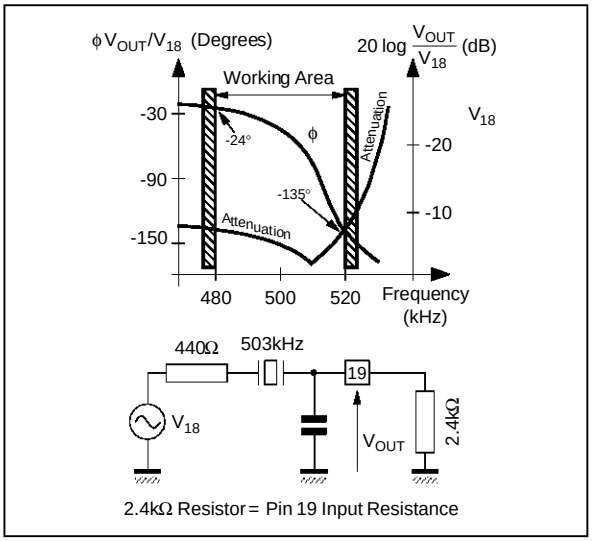
Figure 20



C. - CHARACTERISTICS OF THE EXTERNAL FILTER

The ceramic resonator behaves as a capacitor at $f < f_S$ (f_S : series resonance frequency) and as an inductor at frequencies falling between its two resonance frequencies.
Combined with a "R.C" network to generate a 90° phase lag, the overall arrangement will exhibit the following characteristics : see Figure 21

Figure 21



Thus, a variable (24^o to $+135^o$) phase lead with a gain higher than 10dB, must be implemented on-chip so as to enable the system to enter into oscillation.

The frequency dead points correspond to the maximum internal phase variations. This phase shift is controlled by voltage V_{22} whose value of $5.6V \pm 0.7$ is determined by two diodes.

From the Figure 21, the non-linearity of phase-frequency characteristics is clearly apparent. If linear voltage-frequency response is required for a symmetrical gain of $\phi 1$ loop, it would then be necessary to implement a non-linearity, on the phase control amplifier A4, but in the opposite direction.

D. - STUDY OF THE INTERNAL AMPLIFIER

Let's study the gain and phase response of $\frac{V_{18}}{V_{IN}}$ as a function of V_{22}.

$V_{22} = \frac{V_C}{K}$ where K is a non-linear coefficient

To start with, the "V_C" voltage of comparator "A3" is taken as reference parameter.

The dynamic representation of the output stage can be depicted as below (Figure 22).

with : $I_2' = \frac{i_2}{1 + j\omega\ R1\ C1}$ (at f = 500kHz)

$R1\ C1\ \omega = 1 \Rightarrow i_2' = \frac{i_2}{1+j}$

and $Z = R1 + \frac{1}{j\omega\ C} << R \Leftrightarrow i \approx i_2'$

R1C1 network produces -45^o phase lag of "i" with respect to "i2", around 500kHz.

$$V_{18} \approx - R \cdot (i_1 + I_2')$$

i_1 and i_2 calculation as a function of "V_{IN}" on Pin 19

- A1 Amplifier : $\frac{V_{S1}}{V_{IN}} = \frac{R_C}{dr_1} = \frac{1200}{57} = 21$

  dr : dynamic resistance = $\frac{\lambda}{I}$

- A2 Amplifier :

  $\frac{i_2}{V_{S2}} = \frac{1}{2dr_2} = \frac{1}{54} \Leftrightarrow \frac{i_2}{V_{IN}} = \frac{V_{S1}}{V_{IN}} \cdot \frac{i_2}{V_{S1}} = 0.395$

  $\Rightarrow i_2 = 0.39\ V_{IN}$, i_2 is in phase with V_{IN} therefore : $i_3 = -i_2 = -0.39\ V_{IN}$

- A3 Amplifier :

  $i_1 = i_3 \left(\frac{-V_C}{A\lambda} + \frac{1}{2} \right) = - 0.39\ V_{IN} \left(\frac{-V_C}{A\lambda} + \frac{1}{2} \right)$

"V_{IN}" always leads the "i_1" by 180, only the amplitude of i_1 is a function of V_C (see Figure 23).

- $\frac{V_{OUT}}{V_{IN}} = - R \frac{i_1\ (1 + j\ R_1 C_1 \omega) + i_2}{1 + j\ (R_1 + R)\ C_1 \omega}$

- $i_1 = - 0.39\ V_{IN} \left(\frac{i}{2} - \frac{V_C}{4\lambda} \right)$ and $i_2 = 0.39\ V_{IN}$

The Figure 24 illustrates the characteristics of V_{18}/V_{IN} phase versus V_C.

- Phase variation determined by V_C falls between $+24^o$ and $+135^o$ range
- The gain is higher than 10dB. The Pin 18 output signal of 30 to 40dB has a rectangular component (see Figure 24).

Figure 22

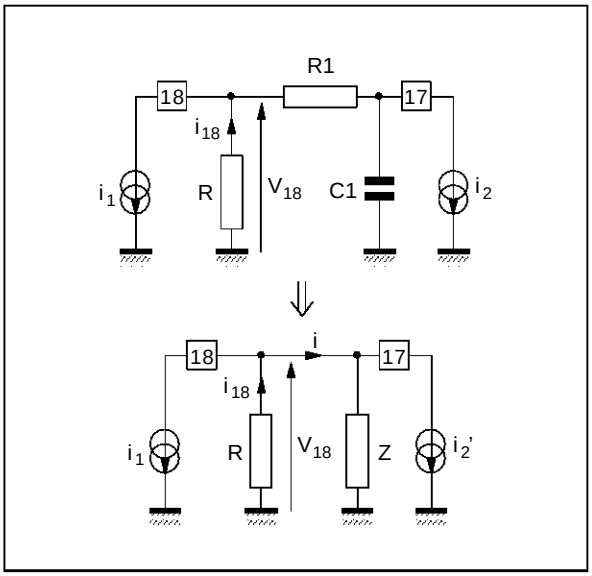


Figure 23 : Vector Representation of V_{18}/V_{IN}

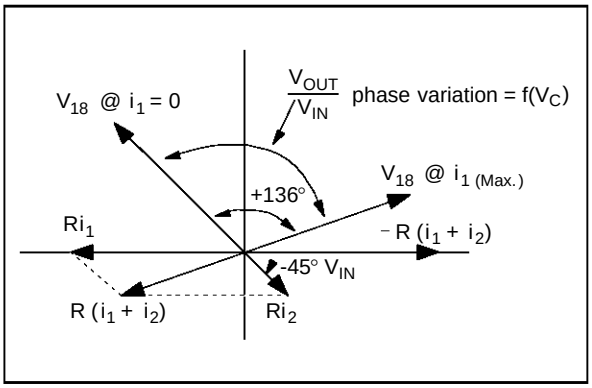
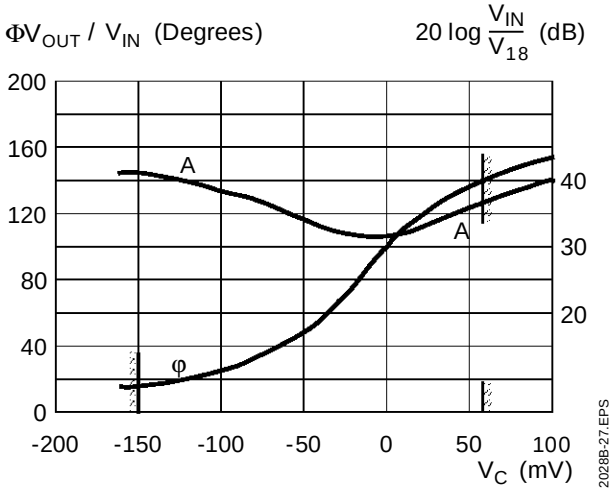


Figure 24



E - CHARACTERISTICS OF THE NON-LINEAR AMPLIFIER "A4" (see Figures 25 and 26)

This is a differential amplifier whose equivalent feed-back resistors of emitters vary as a function of its input voltage.

The maximum output voltage swing is set by two "clamp" diodes connected to "V_{22}" input.

F - VOLTAGE-FREQUENCY TRANSFER CHARACTERISTICS OF V_{CO} (see Figure 27)

The transfer characteristic is linear and centered at 5.6V at 500kHz operating frequency.

$T_{transfer} = \frac{\Delta f}{\Delta V} = 22.4$kH/Vz and once it goes through five divide-by-two stages : $T = \frac{22.4}{32} = 0.7$kHz/V

Figure 25 : $V_C = F(V_{22})$

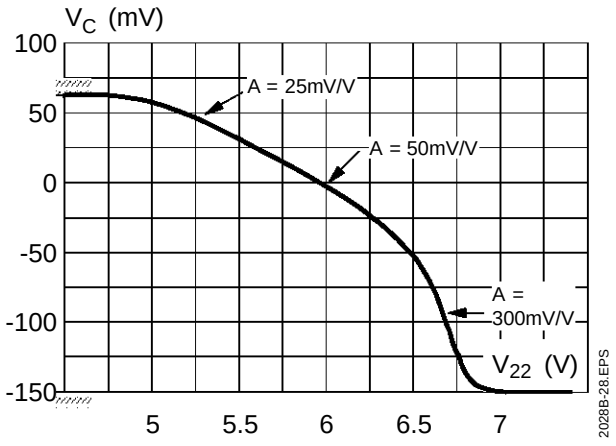


Figure 26 : $I_{22} = F(V_{22})$

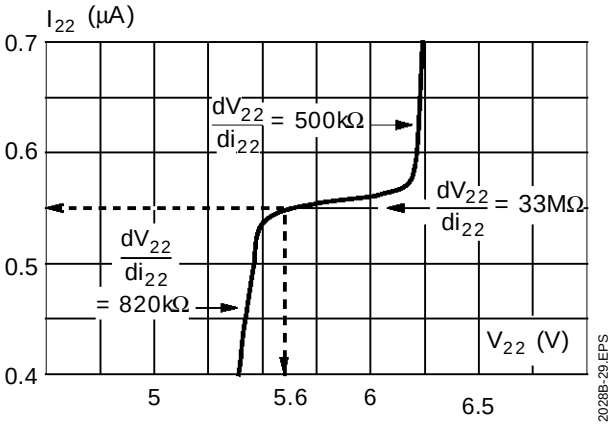
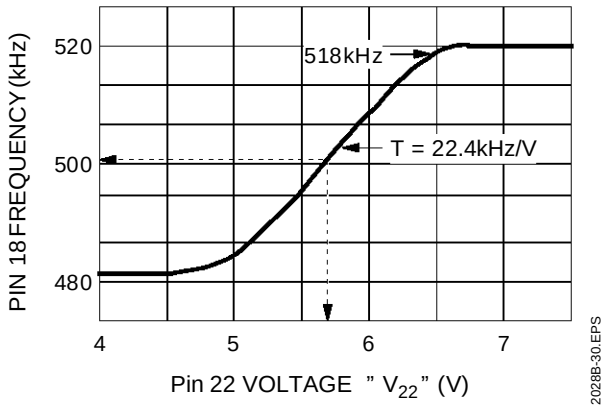


Figure 27



V. 3.4. - "φ1" Time constant switching

When switching between stations or receiving signal via a VCR, the loop locking interval must be as short as possible so as to avoid unwanted visible effect on the picture. In fact, since the synchronization between the VCR motor drive and the playback head is rather imperfect, it will produce frequency and phase fluctuations in the output composite video signal. Under these conditions, phase locking interval must be "short" (VCR Mode).

In the case of broadcast transmission, this loop must also filter all phase variations produced by noisy sync signal. In this case, its locking time constant must be "long" (normal mode).

In other "jungle" circuits, this time constant switching is carried out by capacitor switching within the filter loop. In our case, this function is achieved by changing the current amplitude of the phase comparator.

This amplitude changing modifies the open-loop system gain and therefore the damping coefficient and the locking time constant.

The device will be in short time constant mode under the following two conditions :

- VCR Mode or SCART Connector Mode :
  This mode is enabled by a low state on Pin 23.
  $V_{23} < 2.1V$.
- Transmitter search and tunning.
  In order to accelerate the capture, a "Video Identification" stage will detect the presence or the absence of a video signal on input Pin 27, and deliver accordingly a signal called "Mute".

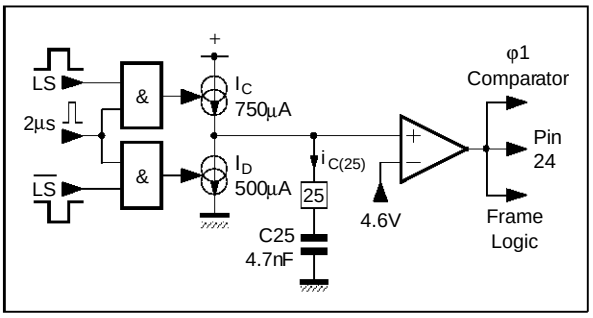
V.3.5 - Video identification stage

This stage will detect the coincidence between the line sync pulse (if present) and a 2µs pulse issued from the logic block. This 2µs pulse at line frequency is positionned at the center of line sync pulse when the first loop "φ1" is locked.

This sampled detection is stored by an external capacitor connected to Pin 25. The video recognition status is also available on Pin 24 so as to enable Sound Muting during station search process and the inhibition of Automatic Frequency Tuning.

V.3.5.1 - Block diagram

Figure 28



The video recognition signal is delivered by a hysteresis comparator.

The recognition time "T_R" is adjustable by an external capacitor, as soon as φ1 is locked :

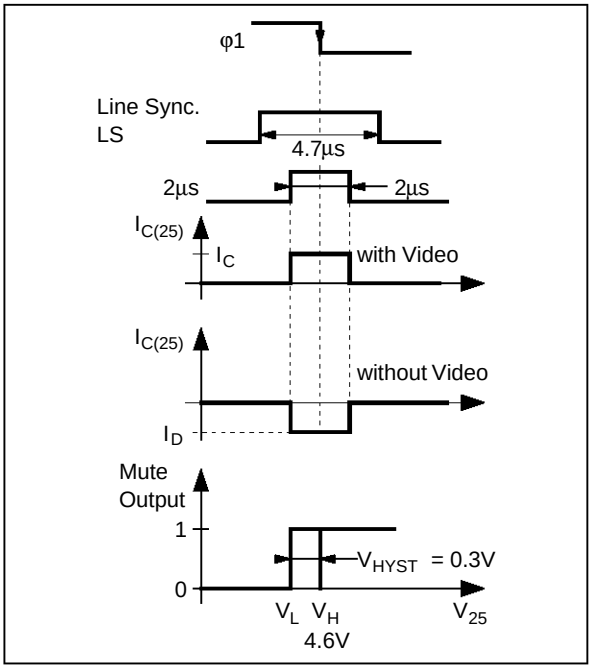
- $I_{C25(AV)} = I_C \cdot \frac{2\mu s}{64\mu s}$

and :

- $T_R = C25 \cdot \frac{V_H}{I_{C25(AV)}} = 1.96 \cdot 10^5 \cdot C25$

  with C25 = 4.7nF $\Rightarrow T_R$ = 1ms
  (which is clearly quite fast)

Figure 29



V.3.6 - Characteristics of loop φ1

V.3.6.1 - Locking accuracy

Let's study the phase error "$\varphi_{OUT} - \varphi_{IN}$" under steady state conditions :

The open-loop gain is :

- $T(p) = \frac{AB\ f(p)}{f}$

  Where :
  A = 0.16mA/rd (long time constant)
  A = 0.47mA/rd (short time constant)
  B = 0.7kHz/V or B = 4.4 10^3rd/s

- $f(p) = R \cdot \frac{1 + \tau_1\ p}{(1 + \tau_2\ p)\ (1 + \tau_3\ p)}$

  Where : R = Dynamic input resistance of VCO.

If a phase step of $\Delta\varphi$ is applied to the input, the following would be obtained as a function of (p) :

$$\Phi_{IN}(p) = \frac{\Delta\Phi}{p}$$

Using the last value theorem : lim f(t) = lim p . f(p)

Let's calculate $\lim_{p\to 0} (\varphi_{IN} - \varphi_{OUT})$

- The closed-loop gain is :

- $H(p) = \frac{T(p)}{1 + T(p)} = \frac{ABf(p)}{p + ABf(p)} = \frac{\Phi_{OUT(p)}}{\Phi_{IN(p)}}$

that is : $\lim_{p\to 0} p\ (\Phi_{IN} - \Phi_{OUT}) = \lim_{p\to 0} \frac{p\Delta\Phi}{p + AB\ f(0)} \to 0$

It is therefore deduced that the system can follow all input phase variations without producing any static error.

In practice, there will be a slight error due to the input bias current "I_B" of VCO, which is 0.55µA at f_O = 500kHz. This DC current is delivered by a phase comparator which will generate a phase error of :

- long time constant :

$$\Delta\Phi_{LONG} = \frac{I_B}{A_{LONG}} = 0.55 \cdot \frac{10^{-3}}{0.16}$$

$= 3.4 \cdot 10^{-3}$ rd or 35ns in Δt

- short time constant : $\Delta\Phi_{SHORT} = \frac{I_B}{A_{SHORT}} = 12ns$

These two errors cause a horizontal picture displacement. On a large screen of 54cm wide, this will be : 64 - 12 = 52µs, which for both modes corresponds to a shift of :

$$\Delta_{LINE} = \frac{\Delta\Phi_{LONG} - \Delta\Phi_{SHORT}}{52} \cdot 520 = 0.24mm$$

It is obvious that such displacement can be fully neglected.

Response to a Frequency Step

- The input phase is : $\Phi_{IN}(t) = \Delta\omega t$

  which as a function of (p) is : $\Phi_{IN}(p) = \frac{\Delta\omega}{p^2}$

- The accuracy is :

$$\lim_{p\to 0} (\Phi_{IN} - \Phi_{OUT}) = \lim_{p\to 0} \frac{\Delta\omega}{p + ABf(o)} = \frac{\Delta\omega}{ABR}$$

  where R = 500kΩ at f(o)

In this case, the phase error depends on both, the magnitude of the frequency step and the static gain ABR.

In general, $\frac{\Delta f}{\Delta f}$ which is the open-loop static gain, is taken into consideration.

$$\frac{\Delta\omega}{\Delta\Phi} = ABR = \frac{2\pi\Delta f}{\Delta t \times 2\pi} = A \cdot 2\pi \cdot B' \cdot R$$

$$\Rightarrow \frac{\Delta f}{\Delta t} = AB'R \cdot \frac{2\pi}{T_H} \text{ (B' in kHz/V)}$$

- In normal mode : A_{LONG} = 0.16 mA/rd

  $\Rightarrow \frac{\Delta f}{\Delta t}$ = 5.5kHz/µs, R = 500kΩ

- In VCR mode : A_{SHORT} = 0.47 mA/rd

  $\Rightarrow \frac{\Delta f}{\Delta t}$ = 16.5kHz/µs

Note : The capture range is specified within ± 500Hz with respect to 15625Hz.

Numerical Example

Let's suppose that in VCR mode there is a frequency variation of ± 100Hz, this will yield a phase variation of 0.1/16.5, i.e. ± 6ns which, on a 54cm wide screen, will produce a horizontal shift of Δ_{LINE} = ± 0.06mm !

It is obvious that an excellent image stability is thus obtained.

V.3.6.2 - Dynamic study

The loop response in transient mode is quite important. It determines the overall system stability and the phase recovery time, which are imposed by the external filter "f(p)".

The close-loop transfer function is equivalent to a second order system. These time constants are in practice displayed on screen by a bar delivered by a special pattern generator representing the phase errors.

The following optimized results were obtained from filter f(p) connected to Pin 22.

Filter component values are :
R1 = 4.7kΩ, C1 = 2.2µF, C = 10nF

A. LONG TIME CONSTANT

- At Δt of 4µs ⇒ N=18 lines, i.e. τ_{LONG} = 1.15ms. System oscillations are perfectly damped. Image stability with a noisy video signal is very satisfactory.

B. SHORT TIME CONSTANT

- At Δt = 4µs ⇒ N = 5 lines, i.e. τ_{SHORT} = 0.32ms
- n = 5 lines

One should notice fast phase recovery, naturally followed by bounced oscillations due to the characteristics of a second order device.

As given in application diagram section 6, an other alternative would be to use the following component values : R1 = 3.9kΩ, C1 = 4.7µF, C = 15nF.

V.3.7 - Phase comparator inhibition

The phase comparator is disabled under two conditions :

- During frame sync pulse (see Figure 30)
  Inverting the line sync pulse contained within the video signal will provide the frame sync pulses required for the synchronization of vertical scanning.
  Since the current supply to comparator $\phi 1$ is controlled by the line sync pulse, the comparator must be inhibited at the time of line sync inversions so as to avoid occurence of phase errors at the beginning of each frame.
  This inhibition is activated during FRI (Frame Retrace Inhibition) issued by frame logic circuitry.
  If $\phi 1$ is locked before the vertical scanning synchronization occurs, (e.g. when switching between channels), and since FRI phase is not yet correctly positioned, the $\varphi 1$ must be further inhibited by FS signal which is the extracted frame sync pulse.
- During line scanning (see Figures 31 and 32)
  This inhibition will eliminate the occurrence of all possible phase errors due to a noisy sync signal or parasitics during the line scanning phase. It yields excellent display stability at noisy video signals.
  - f1 Inhibition in long time constant mode (VCR = 0)
    $S_{INH(LONG)}$ = Mute . (FRI + FS + $\overline{BLK}$. $LINE_{INH}$) and $S_{INH(SHORT)}$ = 1
    Inhibition is activated during, frame sync, FRI and each time line trace interval - except at frame beginning between lines 8 and 21.
  - $\phi 1$ Inhibition in short time constant mode (VCR = 1)
    $S_{INH(SHORT)}$ = Mute . (FRI + FS) = $S_{INH(LONG)}$
    In VCR mode, inhibition is disabled during line trace since phase or frequency variations are not taken into account instantenously.

Figure 30 : On Screen Display of Time Constants

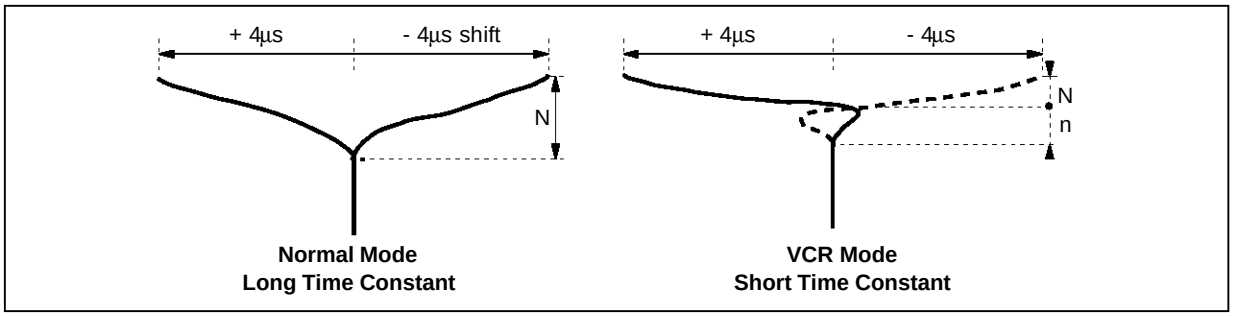


Figure 31

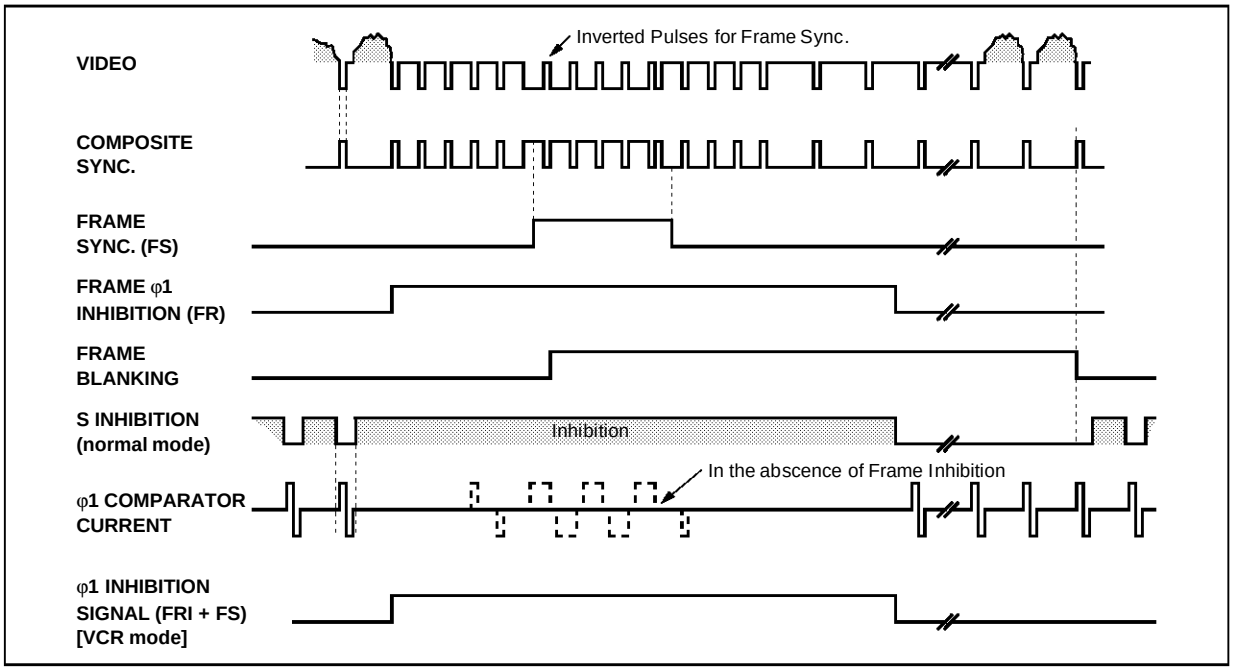


Figure 32

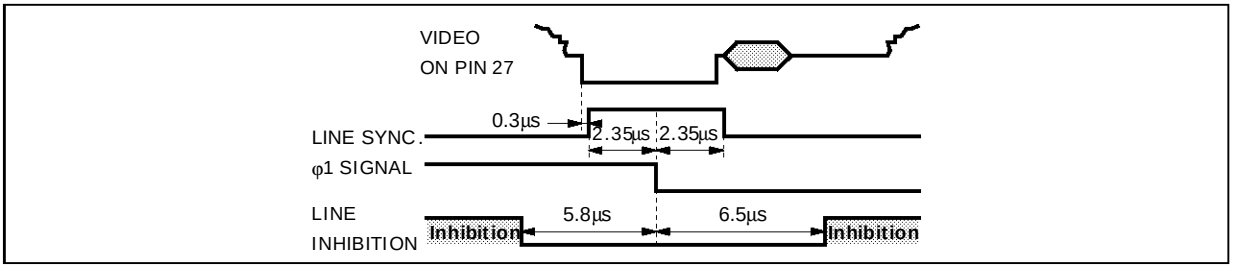
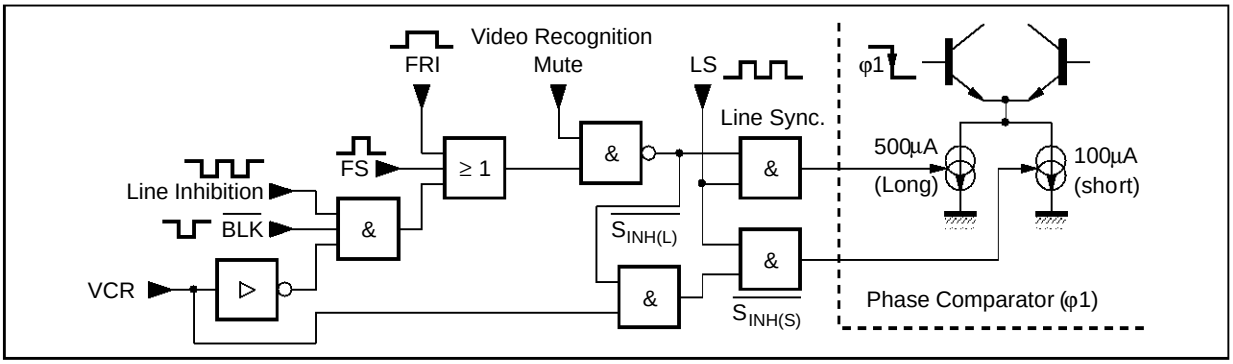


Figure 33 : φ1 Inhibition Logic Block Diagram

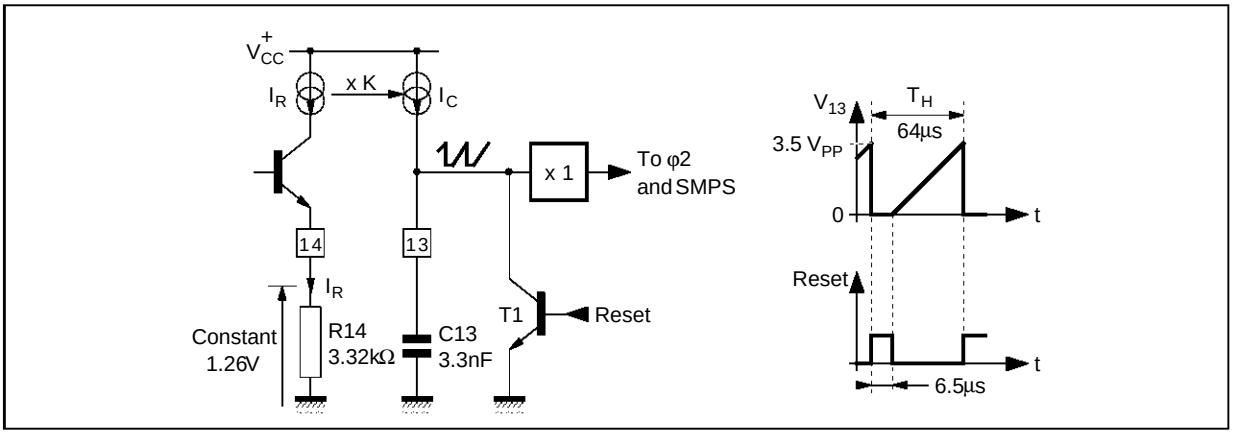


V.4 - Line saw-tooth generator

Before going through a detailed study of the second phase locked loop "ϕ2", let's have an overview of the line saw-tooth generator which has been mainly implemented for ϕ2 phase variations and also the phase modulation of the switching power supply.
It uses the combination of an external capacitor connected to Pin 13 and an internally implemented constant current generator to generate a saw-tooth voltage at line frequency.
Its frequency is determined by the reset frequency of the capacitor "C13". This reset signal is issued by the line logic circuitry at a period multiple of VCO period (×32).

- $I_C = K \cdot I_R = K \cdot \frac{1.26}{R_{14}} = 200\mu A$
- $V_{13PP} = \frac{I_C\,(T_H - t_{reset})}{C13} = \frac{K \cdot 1.26\,(T_H - t_{reset})}{R14 \cdot C13}$
  $= 3.48V$
- $V_{CE(SAT)T1} \approx 20mV \Rightarrow V_{13(MAX)} = 3.5V$
- In sync mode :
  $T_H = 64\mu s$, $t_{RESET} = 6.5\mu s$, $K = 0.527 \pm 2\%$

Figure 34



V.5 - Second Phase Locked Loop "ϕ2"

This stage controls the horizontal deflection of the electron beam i.e., the horizontal picture scanning. The frequency of operation, in the absence of video signal, is a multiple of the VCO frequency, i.e. 15625Hz - 500Hz.

When video signal is present, the scanning frequency is synchronized with the video signal through the first phase locked-loop "ϕ1".

The output rectangular waveform signal drives the line switching transistor. This transistor, when turned-off, generates what is commonly called the "line flyback".

In order to obtain a horizontally centered picture, the line flyback (LF) must coincide with the blanking time on tube cathodes.

The turn-off delay is due to transistor base storage time. This time varies in different TV sets as the transistors employed may have different operating characteristics which are functions of temperature variations, power rating and base drive.

Therefore, it follows that in order to obtain stable image centering, the line flyback must be phase-locked with respect to the video signal.

The second phase-locked loop also offers the possibility of horizontal phase-shift adjustment.

Figure 35

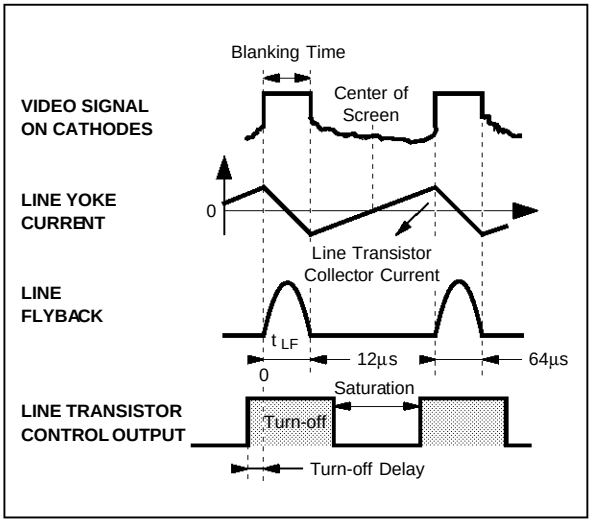
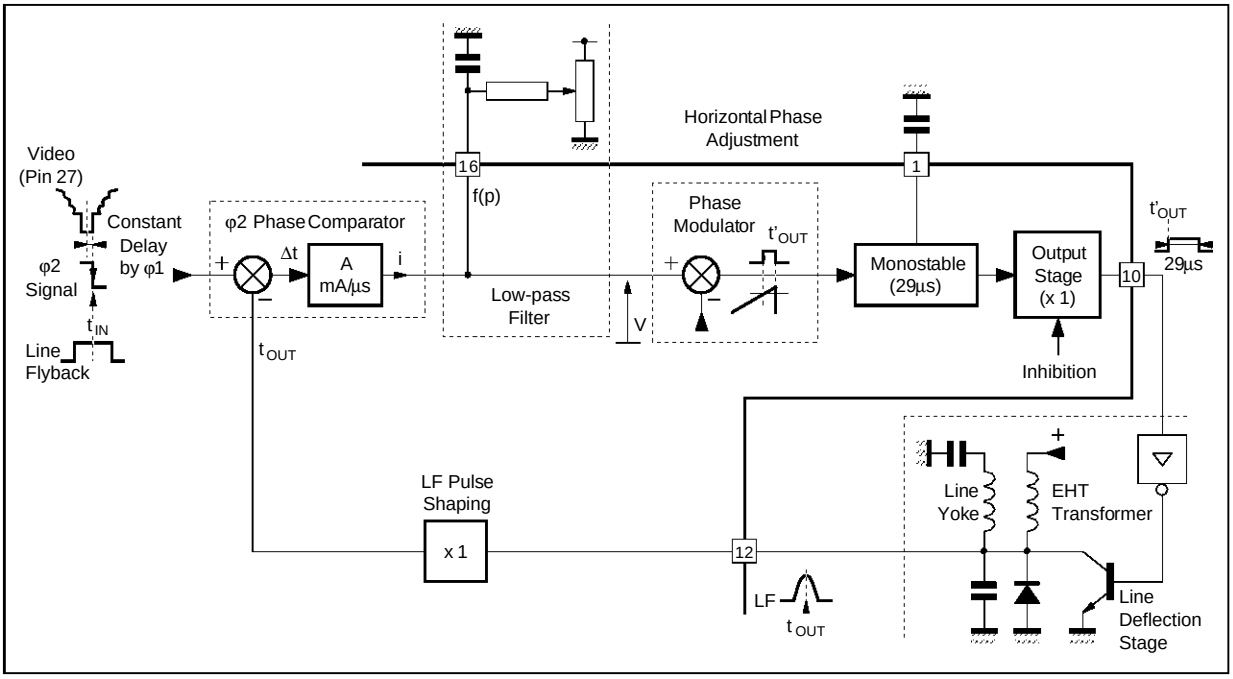


Figure 36 : Second Phase Locked Loop "φ2" Block Diagram



V.5.1 - Duty of different building blocks

V.5.1.1 - "ϕ2" Phase comparator

This block generates a current proportional to the phase difference between the phase reference "ϕ2" and the middle of the line flyback to be phase-locked.

V.5.1.2 - Low-pass filter

- Rejects the parasitic component "sum of phases"
- Smoothens the "phase difference" component
- Allow "phase adjustment" by generating an error within the loop

V.5.1.3 - Phase modulator

Uses the line saw-tooth voltage to convert the voltage delivered by the low-pass filter into a phase corresponding to the line transistor turn-off control signal.

V.5.1.4 - Flip-flop

Generates the turn-off control signal for a constant time (fixed by the external capacitor), the phase of which is set by the modulator.

V.5.1.5 - Output stage

- Delivers the control signal for line transistor driver
- Disables the output during start-up and protection phases

V.5.1.6 - Line deflection stage

- Generates the saw-tooth current for line yoke
- Generates the high voltage required by picture tube and other supply voltages
  The line flyback information is provided by the EHT transformer.

V.5.2 - Operation of building blocks

To provide an easier understanding of the subject, the "ϕ2" loop study will be covered as a function of various time intervals and not as a function of phase.

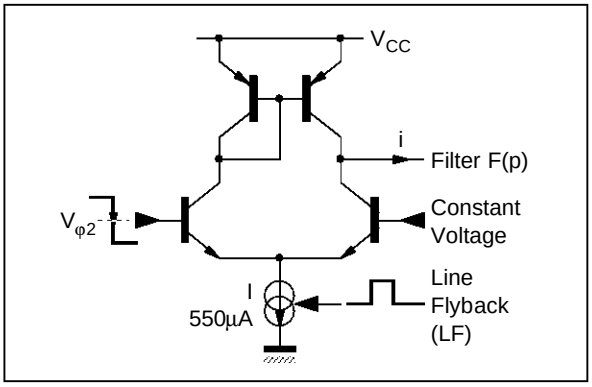
V.5.2.1 - Phase comparator "ϕ2"

The operation is identical to that of "ϕ1" loop.

The $V_{\phi 2}$ signal issued by logic block is phased with respect to the middle of line sync pulse on Pin 27 and delayed by a 2.6µs interval so as to be at the middle of blanking time on video cathodes.

The output current component "$2f_H$" is rejected by the low-pass filter.

Figure 37



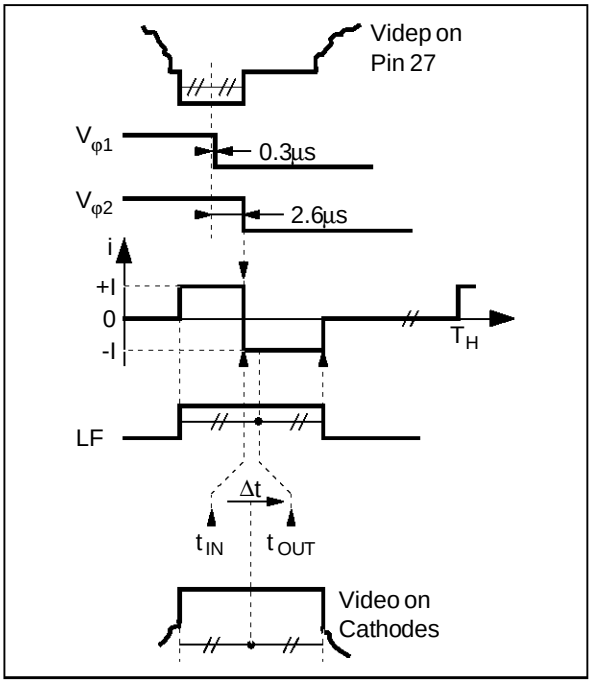
- The average current is $i = 2I \frac{\Delta t}{T_H}$

  Where : $\Delta t = t_{IN} - t_{OUT}$
- The conversion gain is therefore :

  $A = \frac{i}{\Delta t} = \frac{2I}{T_H} = 17\mu A/\mu s$

  At : I = 550µA and T_H = 64µs, "A" will remain constant since "I" is a multiple of "I_{REF}" current on Pin 14.

Figure 38



V.5.2.2 - Low-pass filter f(p)

The horizontal phase-shift adjustment is taken into account : see Figure 39

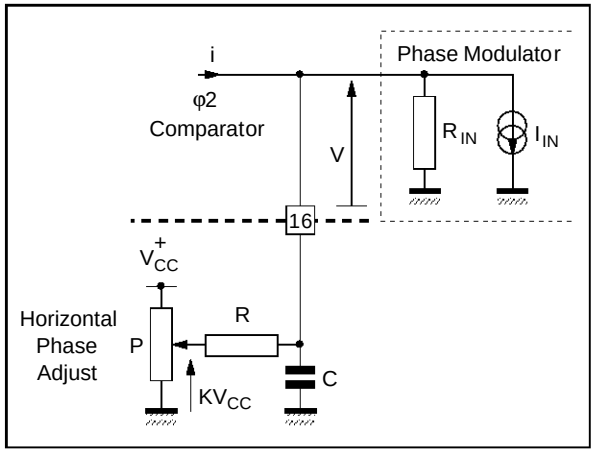
- Filter V = f(i) transfer characteristic is given as :

$$V = Zi + \frac{Z}{R} \cdot K \cdot V_{CC} - Z \cdot I_{IN}$$

Where :

- $Z = R_{IN} // R // \frac{1}{C \cdot p}$
- R_{IN}, I_{IN} : modulator input characteristics

Figure 39



In Dynamic Mode

- $V = Zi \Rightarrow f(p) = \frac{V}{i} = Z(p) = \frac{R'}{1 + \tau p}$

Where :

- $R' = R_{IN} // R$ (R >> Potentiometer P)
- $\tau = R' . C$: Filter time constant

The network behaves as a first order low-pass filter whose cut-off frequency at -3dB is : $f_{-3dB} = \frac{1}{2\pi R'C}$

Filter component values

- R = 470kΩ and C = 22nF
  - In practice, ($K \in [0,1]$) V_{CC} = 12V
- R_{IN} = 25MΩ , I_{IN} = 0.65µA (base input current)
  - F_{-3db} = 15.7Hz with adjustment and 0.3Hz without adjustment

V.5.2.3 - Phase modulator

This is built around a comparator which converts the filter voltage to a rectangular waveform such that its rising edge phase, variable as a function of filter voltage "V", will trigger the line transistor turn-off control circuitry.

The conversion gain is determined by the slope of the line saw-tooth applied to comparator.

Figure 40

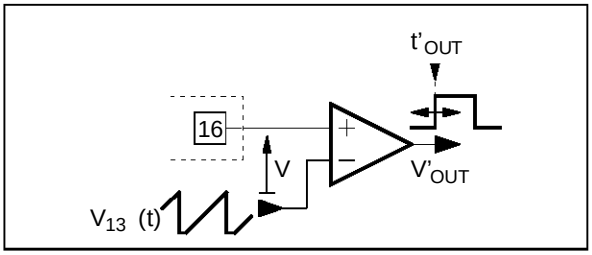
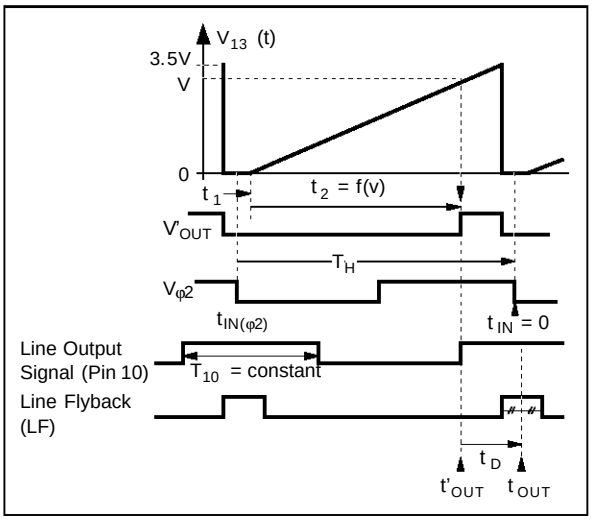


Figure 41



Transfer characteristic is given by :

$$\frac{\Delta t'_{OUT}}{\Delta V} = \frac{\Delta t_{13}}{\Delta V_{13}} = B = 16.4\mu s/V \text{ therefore } t_2 = B.V$$

Let's consider the delay interval between "t_{OUT}" and the reference time "t_{IN}"

where t_{OUT} is the middle of line flyback :

$t_{OUT} - t_{IN} = t_2 + t_d + t_1 - t_H$

Where :

- t1 = 4.3µs
  Reset for V_{13} and $V_{\phi 2}$ are signals coming from line logic block and are synchronized on line sync
- t_d = 2 to 15µs
  Delay between leading edge of output signal - Pin 10 - and the middle of line flyback
- t_H = 64µs
- $t_{OUT} - t_{IN} = B.V + t_d - 59.7\mu s$

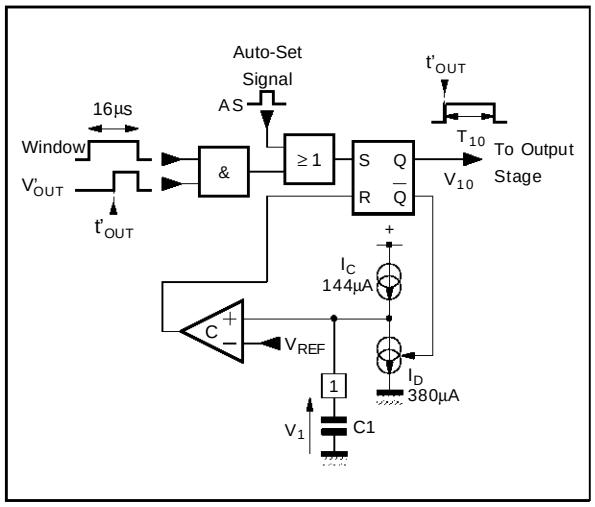
V.5.2.4 - Line flip-flop (TEA2028 only for TEA2029 refer to Section VII.6)

It generates a constant duration rectangular signal used to turn-off the line transistor. It is triggered by the rising-edge of the phase comparator output voltage and reset after capacitor on pin 1 is charged.

A. BLOCK DIAGRAM

"V'$_{OUT}$" will set the flip-flop thereby allowing the capacitor "C1" to be charged by current "I_C" delivered through current generator. The voltage across capacitor begins rising until it reaches "V_{REF}". At this time, comparator "C" is triggered, the output of which will in turn reset the flip-flop. The capacitor "C" is consequently discharged by current I_D - I_C.

Figure 42



B. T10 CALCULATION (see Figure 43)

$$T_{10} = \frac{C1 \cdot \Delta V_1}{I_C} = \frac{C1 \cdot V_{REF}}{I_C}$$

"I_C" is a fraction of "I_{REF}" on pin 14

$$I_C = \frac{I_{REF}}{\alpha} = \frac{V_{REF}}{\alpha \cdot R14} = 144\mu A$$

$\Rightarrow T_{10} = \alpha \cdot R14 \cdot C1 = 2.64 \cdot R14 \cdot C1$
with R14 = 3.32kΩ, C1 = 3.3nF $\Rightarrow T_{10} = 29\mu s$

- T_{10} is independent from temperature and V_{CC}
- α has a maximum dispersion of ± 3% from device to device

C. 16µs WINDOW

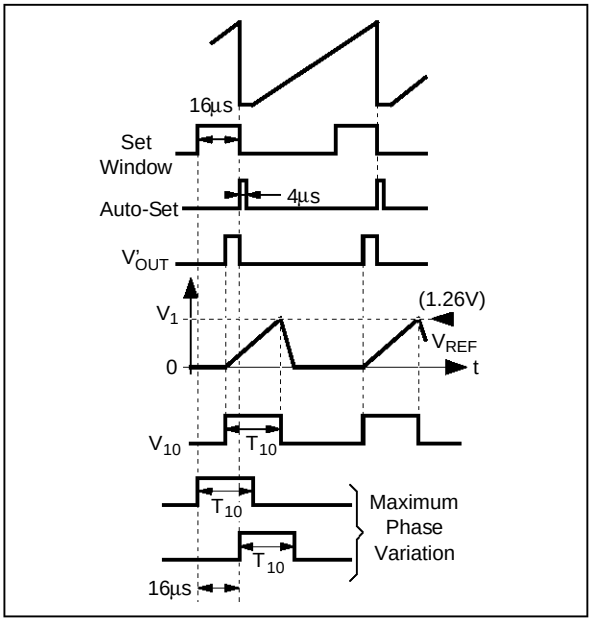
This window is generated by the line logic circuitry and sets the maximum phase variations of the output signal "V_{10}".

Also, for protection purposes, should "V_{16}" voltage equal "0", the output signal will be always present and have a maximum phase shift of 16µs with respect to the falling-edge of the line saw-tooth.

D. AUTO-SET TO "1"

To provide protection, this function will trigger the flip-flop if the modulator is disabled, i.e. $V_{16} > V_{13(MAX)}$.

Figure 43



E. MAXIMUM "T10" VALUE AS A FUNCTION OF "C1"

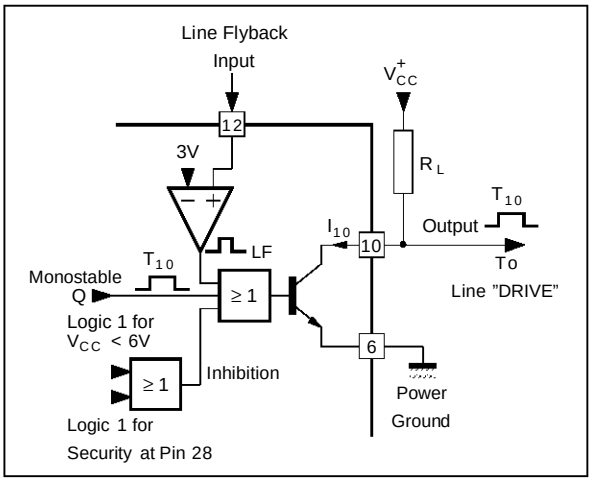
$T_{10\ (Min.)}$: 16µs (window) + 4µs (auto set) = 20µs
$\Rightarrow C1_{(Min.)} = 2.3nF$

$T_{10\ (Max.)}$: for $\frac{C1 \cdot V_{REF}}{I_D - I_C} + \frac{C1 \cdot V_{REF}}{I_C} \leq 64\mu s$
$\Rightarrow T_{10\ (Max.)} = 40\mu s \Rightarrow C1_{(Max.)} = 4.6nF$

For normal operation, C1 value has to be chosen between 2.3nF and 4.6nF.
If Pin 1 is grounded, output signal (Pin 10) is inhibited and goes high.

V.5.2.5 - Line output stage & inhibitions

Figure 44



Open-collector output :
$V_{10(SAT)} < 1.5V$ at $I_{10(MAX)} = 20mA$

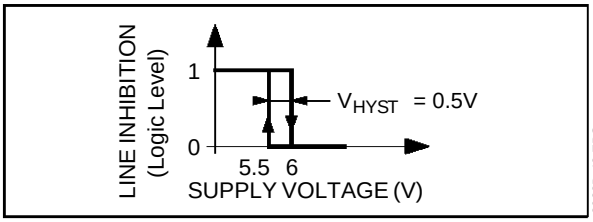
The line output (Pin 10) will go high if either the following three inhibitions is activated :

A. INHIBITION AT START-UP

This is generated by a hysteresis comparator which is driven by "KV_{CC}" and the "1.26V" reference voltage.

This inhibition is mandatory since the device will operate only at $V_{CC} \geq 5V$.

Figure 45



B. INHIBITION DURING LINE FLYBACK

The output signal Pin 10 is high during line transistor turn-off. The leading edge of output signal Pin 10 turns off the line transistor after a delay interval (storage time).

The line transistor turn-off generates an overvoltage on the collector corresponding to the line flyback pulse. During this interval, in order to avoid transistor destruction, the Pin 10 output must absolutely remain high.

This is done internally with the line flyback pulse (Pin 12), which forces Pin 10 output to high level during the line flyback time.

C. SAFETY INHIBITION

The device has a security input terminal "Pin 28". If a signal lower than V_{REF} (1.26V) is applied to this pin, line and power supply outputs are all inhibited.

This function is particularly useful for TV chassis protection. Refer to section V.7.5 for further details.

V.5.2.6 - Line deflection stage

This chapter will cover a general description of the "horizontal deflection stage" employed almost commonly in all recent TV sets.

Deflection of electron beam is proportional to the intensity of magnetic field induced by the line yoke. This yoke is equivalent to an inductor. The deflection is therefore proportional to the current through inductor.

In order to obtain a linear deflection from left to right as a function of time, a saw-tooth current must be generated within the yoke. The approach is to apply a switched DC voltage to the line yoke.

- When K is closed :

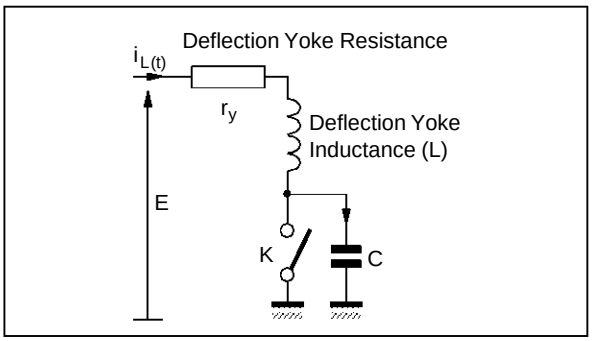
$$i_{L(t)} = \frac{E}{r_y}\left(1 - e^{-\frac{ryt}{L}}\right)$$

- $\frac{L}{r_y}$ is always higher than half of trace time :

$$\frac{t_{trace}}{2} = \frac{T_H - t_{LF}}{2} = \frac{64 - 12}{2} = 26\mu s$$

- "i_L" variations as a function of time :

Figure 46



$$\frac{di_L}{dt} = \frac{E}{L}e^{-\frac{ryt}{L}} \approx \frac{E}{L}\left(\text{for } t << \frac{L}{r_y}\right)$$

The current will therefore be linear as a function of time $i_{L(t)} = \frac{E}{L} \cdot t$ from "t_1" to "t_2" which is the second portion of the line trace interval.

- Current at the end of trace : $I_M = \frac{E}{L} \cdot \frac{t_{TRACE}}{2}$
- Energy stored within inductor : $W = \frac{1}{2} \cdot L \cdot I_M^2$

  If the switch is opened at $t = t_2$, the "L.C" combination will enter into oscillation, the energy stored within inductor is transfered to the capacitor, which will return it to the inductor and so on.

The circuit period is classically given by :
$T = 2\pi \cdot \sqrt{LC}$

If "K" is closed at time "t_3", the inductor will once again have a voltage "E" across its terminals. The current falls linearly until "t_4". This phase corresponds to the first half of line trace interval.

The overvoltage across C is :

$$V_P = E\frac{t_{trace}}{2\sqrt{LC}} + E \text{ during } t_{LF} \approx \pi\sqrt{LC}$$

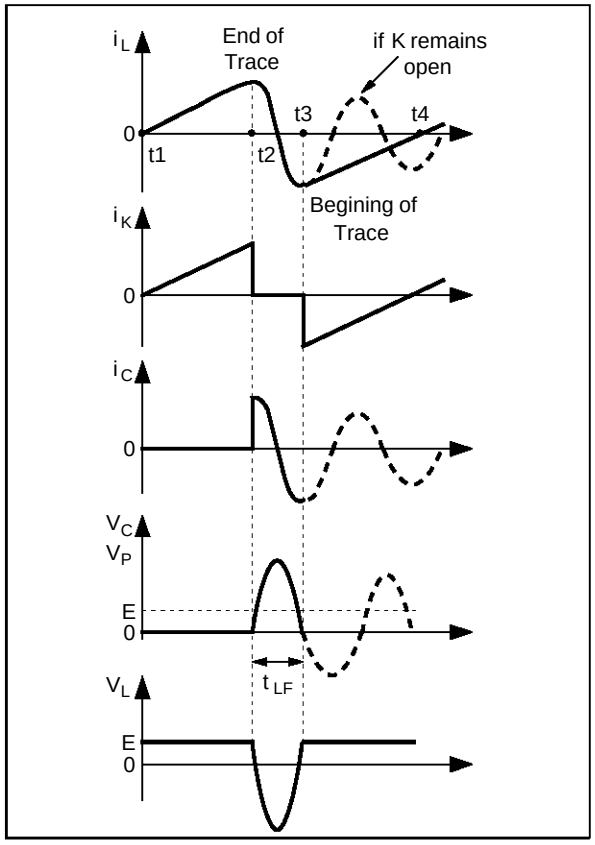
That is : $V_P = E\frac{t_{trace} \cdot \pi}{2t_{LF}} + E$

In practice, E is higher than 100V.
$t_{trace} = 52\mu s$, $t_{LF} = 12\mu s \Rightarrow V_P \geq 780V$

Note that this overvoltage is almost 8 times higher than the source voltage "E". This overvoltage is applied to the primary winding of a "step-up transformer" (EHT Transformer) in order to generate the high voltage required by picture tube anode.

In practice, the power switch "K" is built by a combination of "High Voltage Switching Transistor" and "Fast Recovery Diode".

Figure 47



If considered in average value, it is seen that the voltage across capacitor "CS" is almost equal to the source voltage "E". The saw-tooth current through this capacitor will produce a parabolic ripple around "E", which will thus modify the equivalent source of the line yoke and induce a modified current of "S" shape within the yoke. This "S" current is used to produce a linear picture as a function of the picture tube geometry.

The basic arrangement can be reconstructed by assuming that the equivalent inductor "L" is the transformer "L_P" and line yoke inductors put in parallel (since $VC_{S(AV)} = E$).

The output Pin 10 of TEA2028 is applied to a matching stage called "line driver" the output of which drives the power transistor "T_r". The matching stage is necessary for optimized base drive.

At middle of trace, the transistor enters into saturation and its current rises linearly. V_{10} will then issue a control signal to turn the transistor off. The transistor will be in fact turned-off after a delay interval "t_S" (storage time) varying from 2 to 8 µs depending on application. The system will then enter into oscillation during its half-period thereby generating the line flyback. At the end of flyback time, the line yoke current is negative while the voltage across capacitor "C" has fallen to zero. The energy transfer automatically takes place by the recovery diode during the first portion of trace time.

Also, it is clear that the line scanning phase with respect to video signal is determined by the rising-edge of Pin 10 output signal.

Figure 48 : Simplified Diagram of the Horizontal Deflection Stage

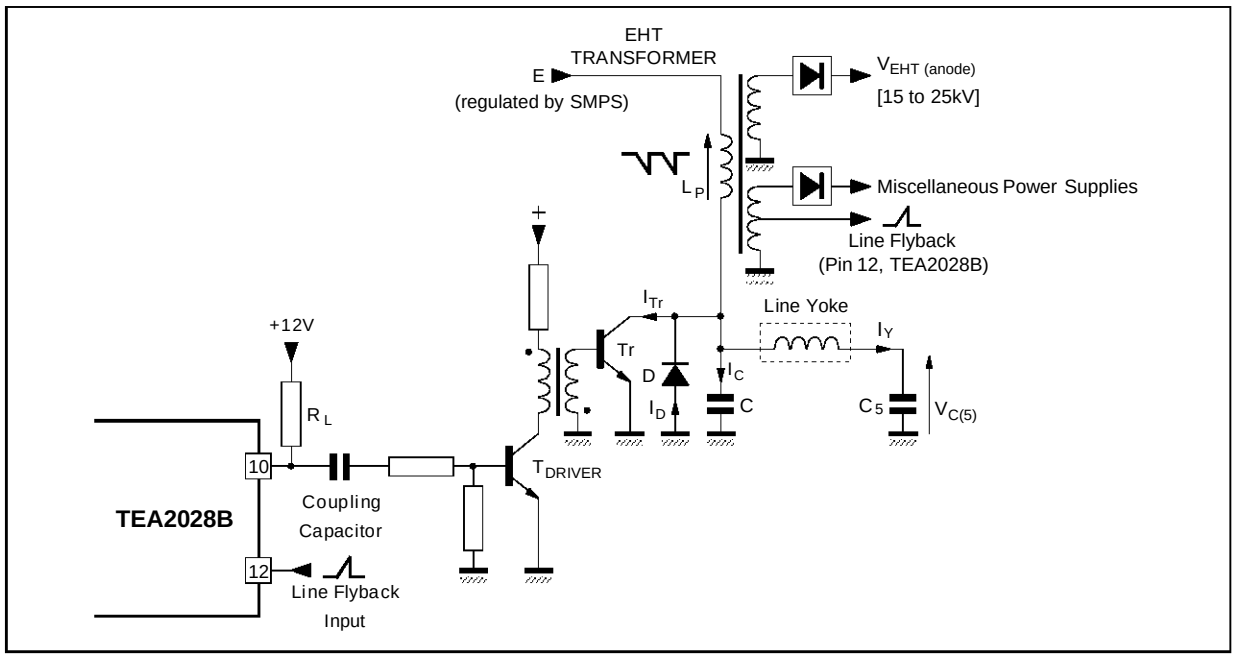
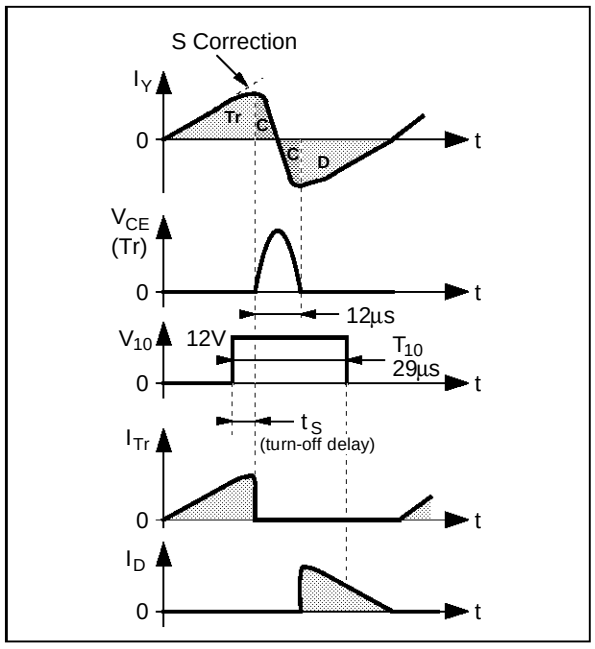


Figure 49



High level duration (T10) of Pin 10 output signal must be higher than the delay interval "$t_{S(MAX)}$" + the flyback time (i.e. 8 + 12 = 20µs) and must turn-off before the end of diode conduction :

$$T_{10} < t_{S(Min.)} + t_{LF} + \frac{t_{trace}}{2} \Rightarrow < 40\mu s$$

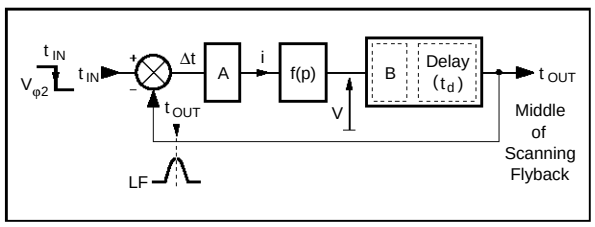
In practice, one will select the pin 1 capacitor C1 = 3.3nF to yield T_{10} = 29µs.

V.5.3 - Characteristics of loop "ϕ_2"

The function to calculate is a time with respect to the origin time set by "$V_{\phi 2}$". In fact, it is an easy task to inter-relate the horizontal displacement (in mm) to a time interval specified in µs.

For a large screen width of 540mm, the horizontal scanning time : 64 - 12 = 52µs, which corresponds to : ≈ 10mm/µs.

Figure 50



- $i = A \cdot (t_{IN} - t_{OUT})$(1)
- $V = Z \cdot i + \frac{Z}{R} \cdot K \cdot V_{CC} - Z \cdot I_{IN}$ (2)
- $t_{OUT} - t_{IN} = B \cdot V + t_d - 59.7\mu s$ (3)
- $Z = \frac{R'}{1 + \tau p}$
- R' = R_{IN} // R
- A = 17µA/µs
- τ = R'C
- B = 16.4µs/V

The open-loop dynamic gain is :

$$T = ABf(p) = ABZ = \frac{ABR'}{1 + \tau p} \quad (4)$$

The system exhibits the characteristics inherent to a first order circuit and is therefore stable.

Combining equations (1), (2), (3) and (4), the t_{OUT} delay is found as follows :

$$t_{OUT} = t_{IN} - \frac{BZI_{IN}}{1+T} + \frac{t_D - 59.7\mu s}{1+T} + \frac{B\frac{Z}{R} \cdot KV_{CC}}{1+T}$$

Dynamic gain = 1 | Error term due to the input current "I_{IN}" | Error term due to delay | Error term due to phase shift adjustment (if applicable)

2028B-97.EPS

It is therefore clear that the second phase-locked loop does not cause any dynamic delay.

This can be explained by the fact that the phase modulator responds instanenously to all variations of "ϕ_2".

V.5.3.1 - Study of the Static Error

t_{IN} = 0 (phase of $V_{\phi 2}$) is taken as timing reference.

The equivalent impedance of F(p) filter is :

- R' = 460kΩ (R // R_{IN}) : if an adjustment is applied to Pin 16, or
- Modulator input resistance RIN = 25MΩ : without adjustment

A. PHASE SHIFT ERROR IN CASE OF NO ADJUSTMENT

Equation (5) becomes :

$$T_{OUT} = \frac{BR_{IN}\, I_{IN}}{1 + T_1} + \frac{t_D - 59.7\mu s}{1 + T_1}$$

with : T1 = ABR_{IN}

Where :

- R_{IN} = 25MΩ
- I_{IN} = 0.65mA
- t_d = 10µs
- $T1 = 6.8 \cdot 10^3 = 76dB$

t_{OUT} = - 46ns which corresponds to a picture shift of 0.46mm !

The error is quite negligible and thanks to rather high open-loop gain, the display accuracy with respect to the phase set by "ϕ_2", is very satisfactory.

B. STUDY OF SHIFT ADJUSTMENT

With R, P network connected to Pin 16, the t_{out} becomes :

$$t_{OUT} = \frac{-BR'I_{IN}}{1+T_2} + \frac{t_D - 59.7\mu s}{1+T_2} + \frac{B\frac{R'}{R}\cdot KV_{CC}}{1+T_2}$$

With : T2 = ABR' (where R' = R // R_{IN}) and K ∈ [0;1]

Substituting the following values into above equation :

- R = 470kΩ
- R' = 470kΩ // 25MΩ = 46kΩ
- A = 17×10^{-6} A/µs
- B = 16µs/V
- t_d = 10µs
- T_2 = 125
- V_{CC} = 12V
- t_{OUT} = - 38ns - 390ns + 1.5µs×K
  therefore t_{out} = 1.5· K - 0.43 (in µs)

If K varies between 0 and 1
⇒ t_{out} [- 0.43ms to 1.07µs]

which corresponds to a picture displacement of : Δ_{LINE} [- 4mm to + 11mm].

Shift variations as a function of V_{CC} (with adjustment)

$$\frac{dt_{OUT}}{dV_{CC}} = \frac{B\frac{R'}{R}\cdot K}{1+T_2} \approx \frac{B\frac{R'}{R}\cdot K}{T_2} \approx \frac{K}{AR}$$

$$= K\cdot 0.12\mu s/V \left[\begin{array}{l} \frac{dL}{dV_{CC}} = 0.34mm/V \\ \text{at } K_{NOMINAL} = 0.28 \end{array}\right.$$

Therefore, a constant V_{CC} must be applied to the potentiometer.

V.6 - Vertical deflection driver stage

This stage must constantly drive the vertical spot deflection. Such deflection will horizontally scan the screen from top to bottom thus generating the displayed image. Similar to horizontal deflection, the vertical deflection is obtained by magnetic field variations of a coil mounted on the picture tube.

A saw-tooth current at frame frequency will go through this coil commonly called "frame yoke". Frame period is the time required for the entire screen to be scanned vertically.

C.C.I.R. and N.T.S.C. TV standards require respectively 50Hz and 60Hz Frame Scanning Frequencies. Also, a full screen display is obtained by two successive vertical scannings such that the second scanning is delayed by a half line period with respect to the first.

This method increases the number of images per second (50 half images/s or 50 frames/s in 50Hz standard). This scanning mode called "Interlaced Scanning" eliminates the fliker which would have been otherwise produced by scanning 25 entire images per second.

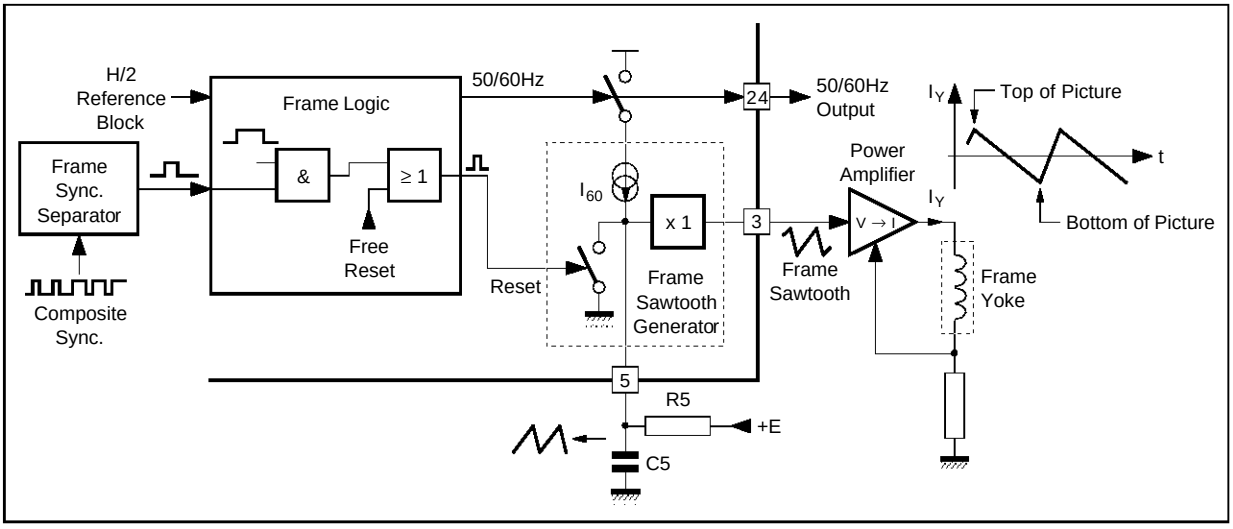
The circuit will generate a saw-tooth voltage which is linear as a function of time and called "frame saw-tooth". A power amplifier will deliver to the "frame yoke" a current proportional to this saw-tooth voltage. It is thus clear that this saw-tooth voltage reflects the function of the vertical spot deflection; which must itself be synchronized with the video signal. Synchronization signals are obtained from an extraction stage which will extract the useful signal during line pulse inversion of the composite sync signal.

Synchronization occurs at the end of scanning, in other words, when the saw-tooth voltage at Pin 5 is reset. This function is accomplished by the "frame logic circuitry" of full digital implementation.

This processing method offers various advantages :

- **Accurate free-running scanning frequency** eliminates the frequency adjustment required by previous devices.
- **Digital synchronization** locked onto half line frequency thereby yielding perfect interlaced display and excellent stability with noisy video signal.
- **Automatic 50/60Hz standard recognition** and switching the corresponding display amplitude.
- **Optimized synchronization in VCR mode.**
- **Generation of various accurate time intervals**, such as narrow "sync windows" thus reducing considerably the vertical image instability in case of for instance, mains interference, superimposed on frame sync pulse.
- **Generation of vertical blanking** signal for spot flyback and to **protect the picture tube in case of scanning failure.**

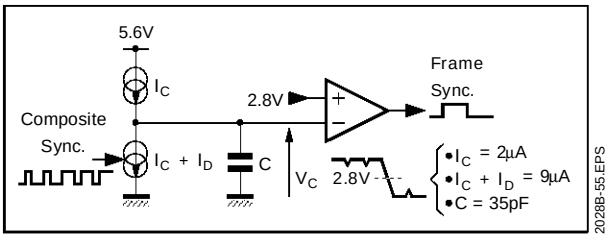
Figure 51 : Block Diagram of the Vertical Deflection Stage



V.6.1 - Frame sync extraction

The main duty of this stage is to extract the frame sync pulses contained in composite sync signal.

Figure 52 : Sync. Extractor Block Diagram



Two current generators are used to charge and discharge the integrated capacitor "C". The discharge generator ($I_C + I_D$) is driven by the composite sync signal.

The ΔV_C across capacitor is : $-\frac{I_D \cdot t_{SYNC}}{C}$

During frame trace, the capacitor is discharged at each line sync pulse thereby generating a ΔV of -0.94V with respect to 5.6V and then recovers the charge by current "I_C". The comparator output remains low.

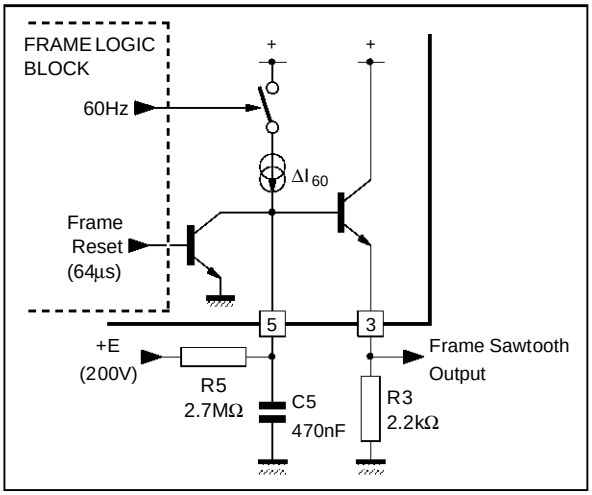
The discharge time is 27µs at the first line sync inversion applied to comparator input. The voltage "V_C" then falls from 5.6V to 0.2V and triggers the comparator "C_0" which will deliver a frame sync pulse when "V_C" crosses the 2.8V level.

The overall arrangement behaves as an integrator and will therefore suppress any noise susceptible to be present on input signal.

An external capacitor Pin 20 can be added to the integrated capacitor C to increase the frame sync time constant.

V.6.2 - Frame saw-tooth generator

Figure 53

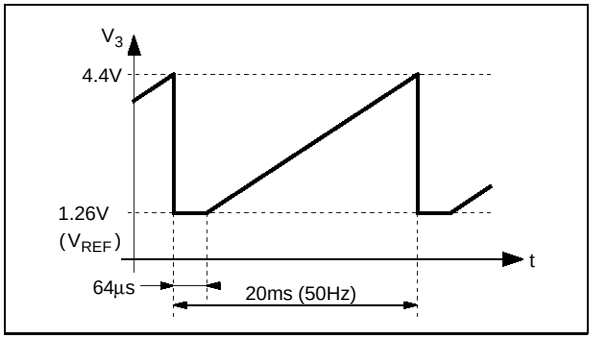


The frame saw-tooth is generated by an external RC network on Pin 5.

The time constant "R5 · C5" is much higher than the frame period. Therefore, the generated saw-tooth is quite linear.

The network is discharged by an internal transistor, controlled by the frame logic block.

Figure 54



V.6.2.1 - 60Hz STANDARD SWITCHING

The NTSC standard requires a vertical picture scanning frequencyof 60Hz, i.e. a saw-tooth period of 16.66ms.

In order to obtain an identical deflection amplitude whatever the standard (50 or 60Hz), the saw-tooth amplitude for both periods must be the same.

60Hz standard recognition is performed automatically by the frame logic block, which will issue a signal to drive a current generator "ΔI_{60}". This current will be summed with the external charge current and will increase the saw-tooth slope, so as to yield same saw-tooth amplitude to that set in 50Hz standard. This current is centered around 14µA and is a fraction of I_{REF} applied to Pin 14.

Employing the recommended component values for network connected to Pin 5, this current will result in identical amplitude in both standards.

$$\Delta V_5 = \frac{I_{60} \times T_{60}}{C_5} = \frac{I_{50} \times T_{50}}{C_5} \Rightarrow I_{60} = I_{50} \times \frac{60}{50} = 1.2 \times I_{50}$$

$$I_{50} = \frac{E}{R_5} = \frac{200V}{2.7M\Omega} = 74\mu A \Rightarrow I_{60} = 88\mu A$$

therefore $\Delta I_{60} = 14\mu A$

V.6.3 - Functions of frame logic block

This section is fully implemented by I^2L logic gates. It is clocked by an accurate "H/2" clock running at half line period (32µs). The required periods and time intervals are obtained by counting the clock pulses.

For the sake of clarity, timing signals so obtained are labeled by the line number corresponding to video signal.

The time corresponding to "x" scanned lines with respect to the beginning of frame saw-tooth (RESET) is therefore :

$$t_x = 64\mu s\ (x - 1) + 32\mu s$$

Figure 55

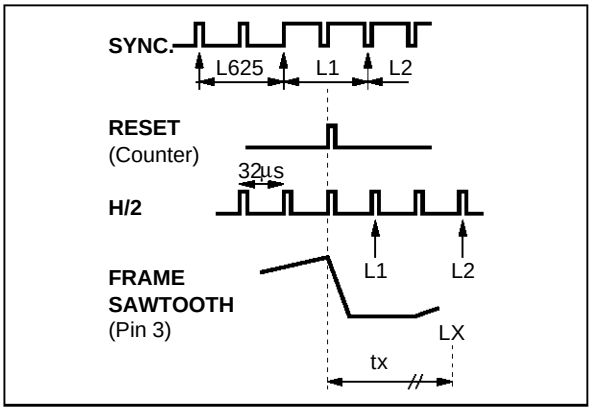
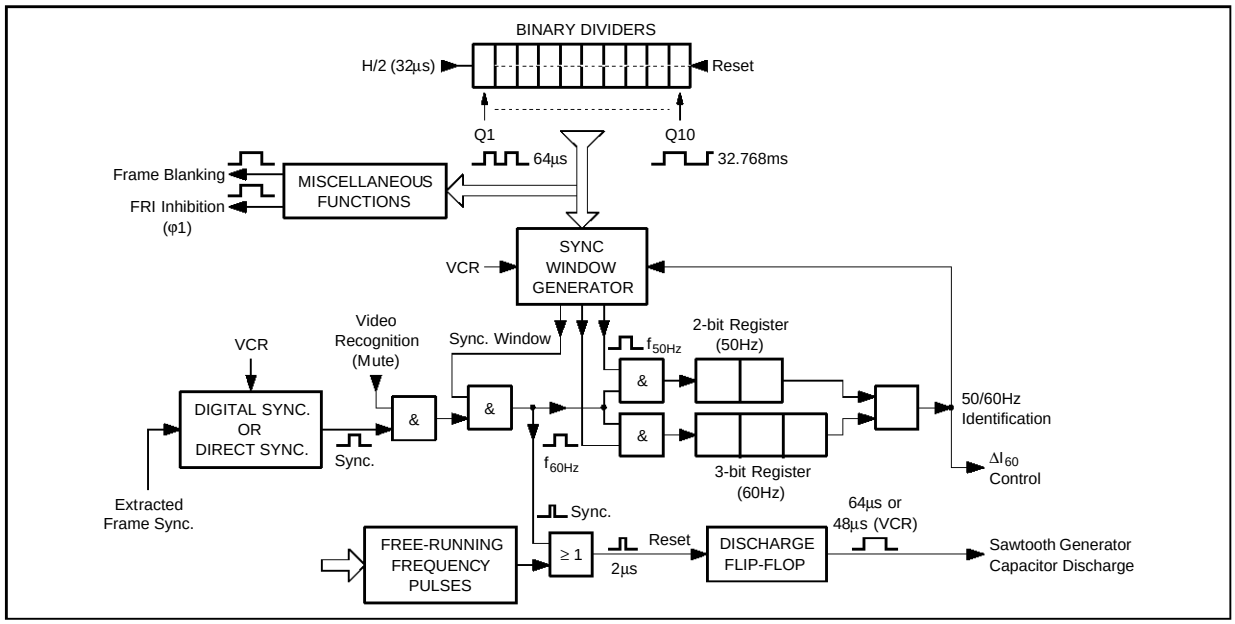


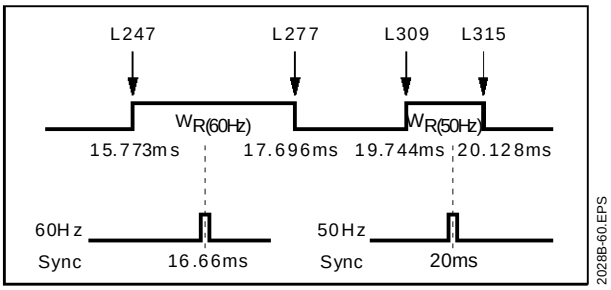
Figure 56 : Block Diagram



V.6.3.1 - 50/60Hz Standard recognition

This function is performed by two shift registers which are loaded by sync pulses (if present) and if these pulses fall within the time interval specific to each standard. These intervals are called "Register Windows" and labeled "$W_R(50)$" and $W_R(60)$.

Figure 57



A. 50Hz STANDARD RECOGNITION

This identification is considered valid if two sucessive sync pulses applied to 50Hz shift register fall within the 50Hz window "$W_R(50)$". At the time of synchronization capture, the first pulse will reset the counters. The second pulse, if present, will then trigger the 50Hz identification 20ms later [$I_D(50) = 1$].

The identification is not valid if two sucessive 50Hz pulses are not detected. Identification signal is also used to reduce the vertical synchronization window in 50Hz standard thereby offering excellent noise immunity against noise susceptible to be present in sync signal and hence good display stability.

B. - 60Hz STANDARD RECOGNITION

This identification is validated after three sucessive sync pulses at 16.6µs period have been detected. Three pulses are necessary to ascertain the identification prior to switching the saw-tooth amplitude. The identification signal [$I_D(60) = 1$] is also used to reduce the synchronization window and, in case of one or two missing pulses close to 60Hz, to set the free-running frequency.

V.6.3.2 - Vertical synchronization window - Free-running period

In the absence of sync pulse various free-running periods are specified. Since vertical scanning must be always active, these free-running periods must be higher than those of 50 and 60Hz standards so as to ensure synchronization.

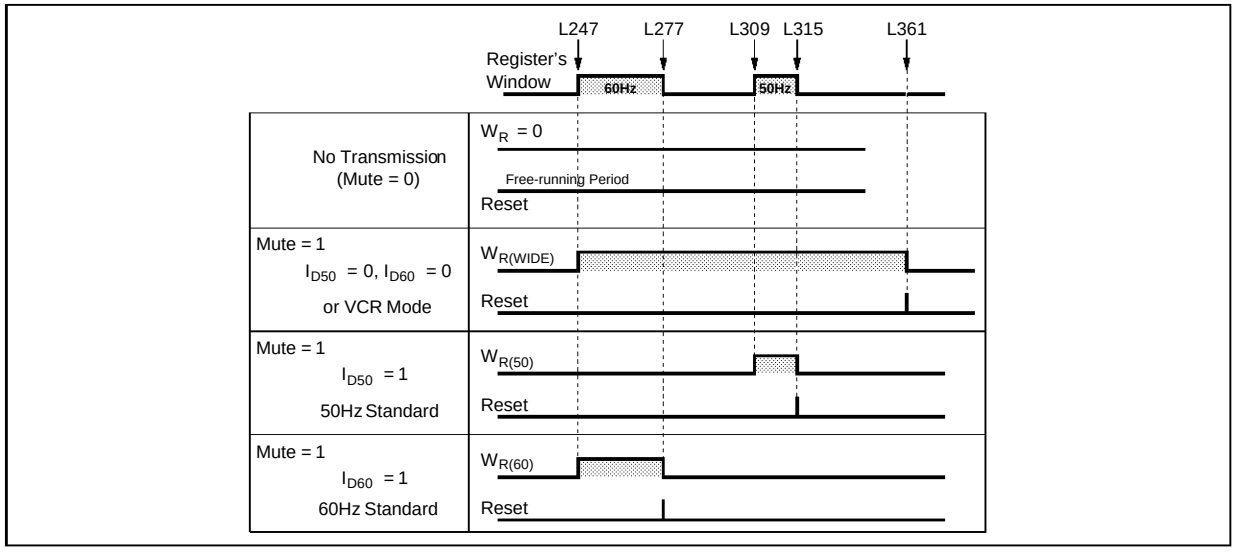
An other window, allowing synchronization only at the end of scanning, is also necessary. Upon synchronization, this window will allow vertical flyback only at the bottom of screen. This window should be narrow for good noise immunity but also wide enough to yield, upon synchronization, a capture time unperceptible on screen.

In our case, as long as no standard identification takes place the window will remain wide, and once one of the standards has been identified, the window will be considerably reduced.

In VCR mode, this window will be always wide since frame frequencies delivered in high-speed search, slow review and picture pause modes are very much variable and must be taken into consideration.

In the absence of transmission (Mute = 0), synchronization is disabled (so as to avoid incorrect synchronization due to noise) and the free-running frequency is around 50Hz. This will eliminate the occurrence of picture overlay at the end of trace at a lower free-running frequency.

Figure 58 : Definition of Synchronization Windows and Free-running Periods



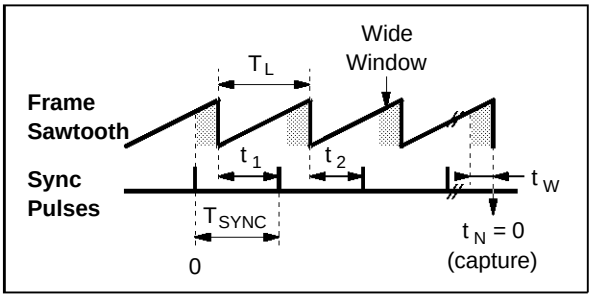
MAXIMUM CAPTURE TIME
The worst case capture time occurs when the first sync pulse just precedes the sync window.

Let's find the number of periods necessary for the capture to occur, i.e. tn = 0.

$\Rightarrow n = \frac{T_L - T_W}{T_L - T_{SYNC}}$, $T_L = 23ms$, $T_W = 7.3ms$

- 50Hz : the number of periods is 6
  $\Rightarrow T_{CAPTURE(MAX)} = 120ms$
- 60Hz : the number of periods is 3
  $\Rightarrow T_{CAPTURE(MAX)} = 50ms$

Figure 59



V.6.3.3 - Frame blanking signal

This signal is necessay to blank the display during each frame flyback. It is triggered at the beginning of frame saw-tooth flyback. The duration of this signal is 1.344ms (or 21 lines).

This "frame blanking" signal is available through Pin 4 (TEA2028 only) which is an open-collector output.

It is also present within the normalized super sandcastle signal on Pin 11 (TEA2028 and TEA2029).

V.6.3.4 - Frame blanking safety (TEA2028 only, for TEA2029 refer to section VII.5)

Its duty is to protect the phosphor coating of picture tube in case of any problem with vertical deflection function such as scanning failure.

A signal to monitor correct scanning is provided by the frame yoke and applied to Pin 2.

In case of any failure, all frame blanking outputs are disabled and go high thereby blanking the entire screen.

During trace phase, the voltage across frame yoke has a parabolical shape due to the coupling capacitor in series with yoke. During frame flyback, the current through frame yoke must be rapidly inverted. Conventionally, a two-fold higher supply voltage is applied across the yoke. This will produce an overvoltage called "flyback".

The safety monitoring status is detected on the falling-edge of flyback, i.e. at the beginning of scanning. A differentiator network is used to transmit only fast voltage variations.

The required pulse is then compared to 1.26V level. Frame blanking goes high in the absence of negative pulse (zero deflection current) or if the pulse does not fall within the first 21 lines (exagerated over-scanning).

Figure 60

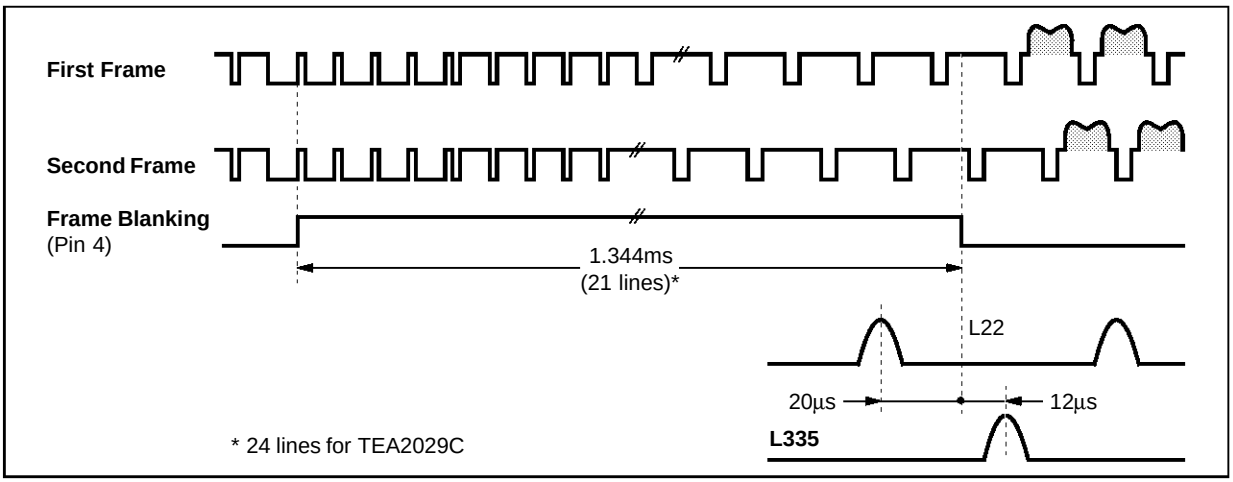
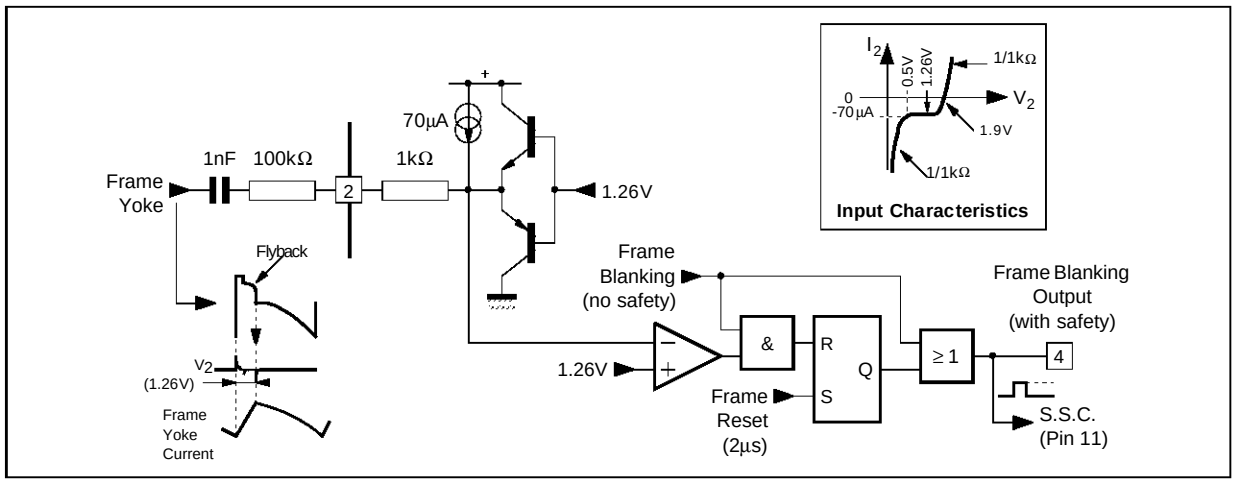


Figure 61 : Block Diagram



V.7 - SWITCHING POWER SUPPLY DRIVER STAGE

Switching takes place on the primary side (mains side) of a transformer by using TEA2164 SMPS Controller manufactured by SGS-THOMSON.

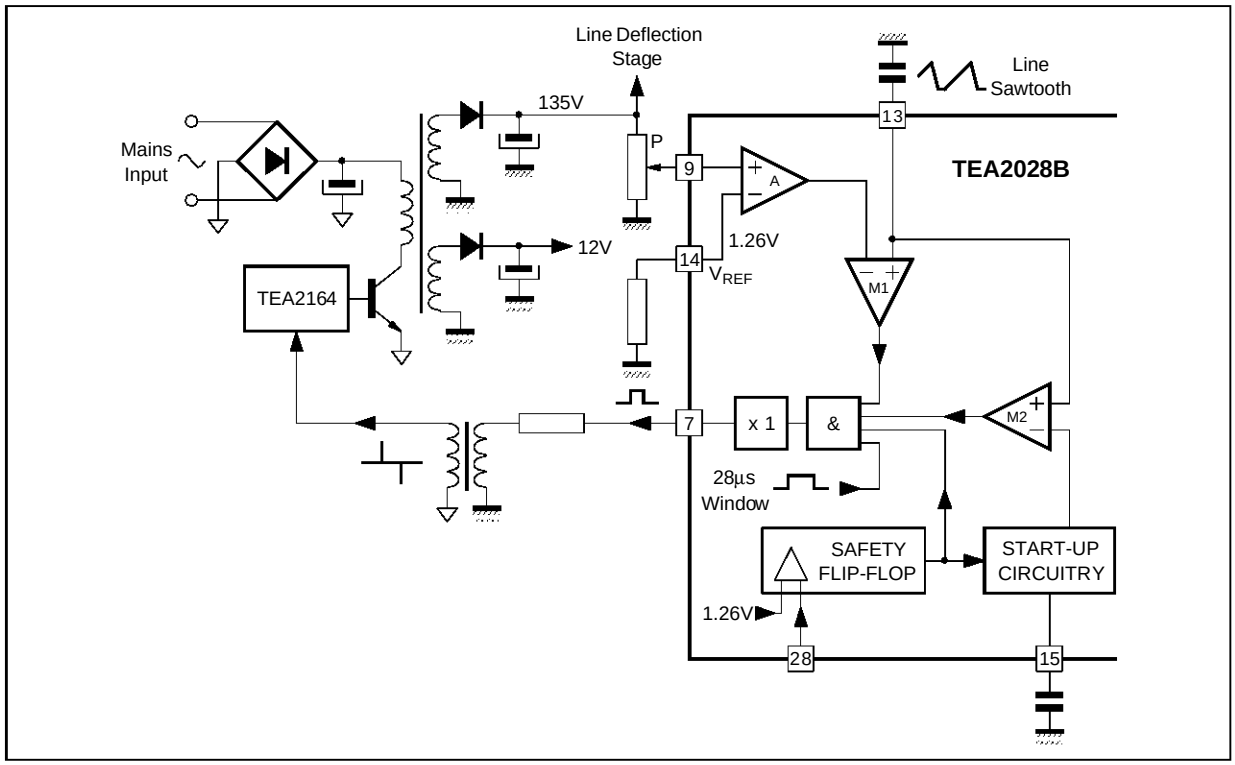
Required voltage values are obtained by rectifying different voltage outputs delivered through secondary windings. The horizontal deflection stage is powered by one of these outputs delivering around hundred volts.

This voltage source must be regulated since any voltage fluctuation will yield variations of the horizontal display amplitude.

The TE2028 monitors this voltage and transmits the regulation signal to the primary controller circuitry via a small pulse transformer. The characteristics of this regulation signal are directly related to the conduction period of switching transistor.

V.7.1 - Power supply block diagram

Figure 62

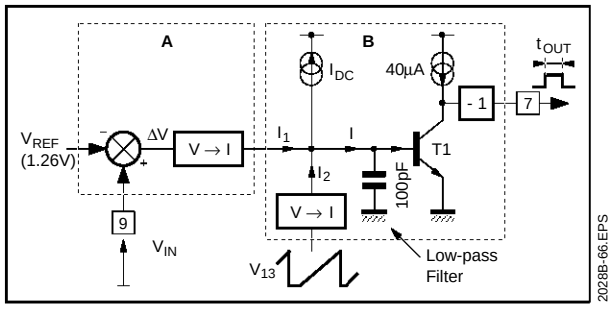


V.7.2 - General operating principles

A fraction of the 135V output voltage to be regulated is compared to the 1.26V reference voltage. Resulting error signal is amplified and then applied to phase modulator "M_1", which will deliver a square waveform at line frequency whose duty cycle depends on the value of input voltage "V_9".
A second phase modulator "M_2" will determine the conduction period as a function of voltage on Pin 15. This function is mandatory for system start-up.
A 28µs window is used to limit the conduction period of the primary-connected transistor.
Supply output (Pin 7) and line output (Pin 10) will be disabled if any information indicating abnormal operation is applied to safety input (Pin 28). Consequently, all power stages are disabled and the TV set is thus protected.

V.7.3 - Electrical characteristics of the internal regulation loop

Figure 63



The phase modulator implemented by a simple transistor "T1" will compare in current mode, the image of amplified input (i_1) with saw-tooth current (i_2) at line frequency. With "i_2" rising, as soon as the sum of "$i_1 + i_2 - I_{DC}$" goes positive, the transistor enters into saturation thus determining the output conduction period.
A low-pass filter implemented by combination of a 100pF capacitor and the input impedance of transistor "T_1", attenuates all frequency variations higher than the line frequency.

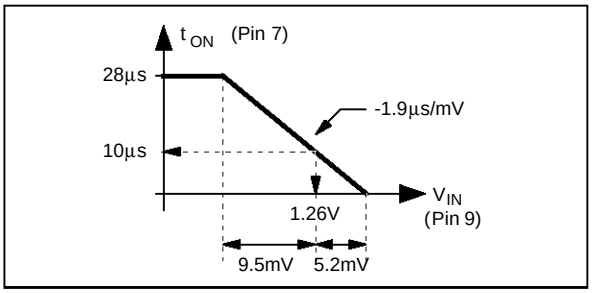
- Input Amplification : $A = \frac{di_1}{dV_{IN}} = 3.3\mu A/mV$
- Modulator conversion gain :

$$B = \frac{dt_{OUT}}{di_1} = -0.558\mu s/\mu A$$

- Overall gain of the internal loop :

$$\frac{dt_{OUT}}{dV_{IN}} = -1.9\mu s/mV \times \frac{1}{1 + j\frac{f}{f_0}} \quad (f_0 = 15kHz)$$

Figure 64 : Conduction Periode (Pin 7) versus Input Voltage (Pin 9)

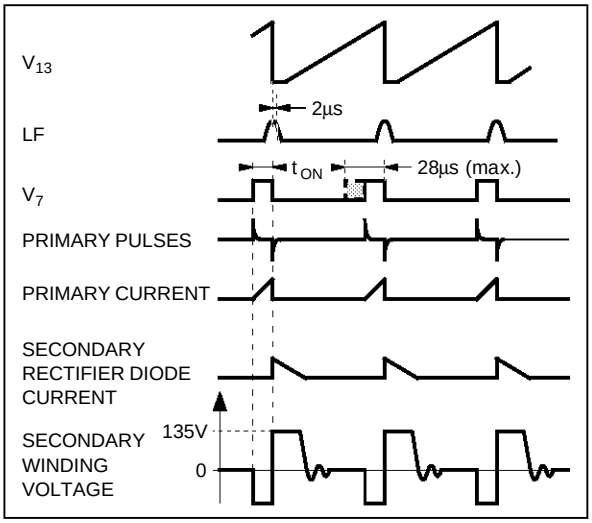


SMPS WAVEFORMS

For discontinous mode "flyback" configuration

The primary-connected transistor is turned-off during the line flyback.
All interference signals due to switching and susceptible to affect the video signal will not therefore be visible on screen.

Figure 65



Regulation Characteristics

The following characteristics have been measured on a large screen and yield excellent results :
- 135V voltage regulation as a function of mains voltage : better than 0.5% for mains voltage variations of $170V_{RMS}$ to $270V_{RMS}$ (P = 60W at 135V)
- 135 V voltage regulation as a function of load : better than 0.5% for a delivered power of 35W to 120W.

This type of power supply offers the following advantages :
- Overall efficiency enhancement : better than 80%
- Reduction of interferences by synchronization on horizontal frequency

- Full protection of the primary-connected transistor in case of short-circuit or open-load on secondary terminals
- Can provide 1W to 7W, for TV standby mode operation (refer to TEA2164 application note).

V.7.4 - Power supply soft-start

When the TV set is initially turned on, control pulses are not yet available and consequently the controller block on primary side will impose a low-power transfer to the secondary winding. This power is produced by an intermittent switching mode called "Burst Mode".

As soon as the V_{CC} supply to TEA2028B exceeds 6V level, line and SMPS outputs are enabled. Since the filtering capactitors on secondary side cannot charge up instantaneously, the voltage to be regulated would not yet be at its nominal value. Without conduction period limitation upon start-up, the device will set a maximum cycle of 28µs which will result in a high current flow through the primary winding and thus through the switching transistor which will in turn activate the protection function implemented on primary side.

Consequently, the primary controller block will be inhibited and the set will not turn-on.

A start-up system has been implemented within TEA2028B to overcome this problem.

This soft start system, will upon initial start-up, use the image of the falling voltage on Pin 15 to increase progressively the conduction cycle. The phase modulator "M2" compares this voltage with line saw-tooth voltage and delivers the corresponding limitation cycle.

During supply voltage rising cycle [V_{CC} (Pin 8) < 6V], the capacitor Pin 15 will charge up rapidly while the voltage across it follows V_{CC}.

At $V_{CC} \geq 6V$, the capacitor is discharged via an internal current generator and the voltage across it decays linearly.

At $V_{15} \leq 3.5V$ (line saw-tooth peak-to-peak voltage), phase comparator "M2" delivers a low conduction period which will gradually increase.

The conduction period (Pin 7) will rise until the secondary voltage reaches the value set by potentiometer "P". When this occurs, the loop is activated.

The Pin 15 discharge current value is 100µA for a duration of 2µs line frequency.

Therefore $I_{D(AV)} = 100 \times \frac{2}{64} = 3.1\mu A$

Conduction period limitation voltage (Pin 15)

$T_{ON(LIM)} = 56\mu s - 16 \times V_{15}$ (in µs)

Figure 66

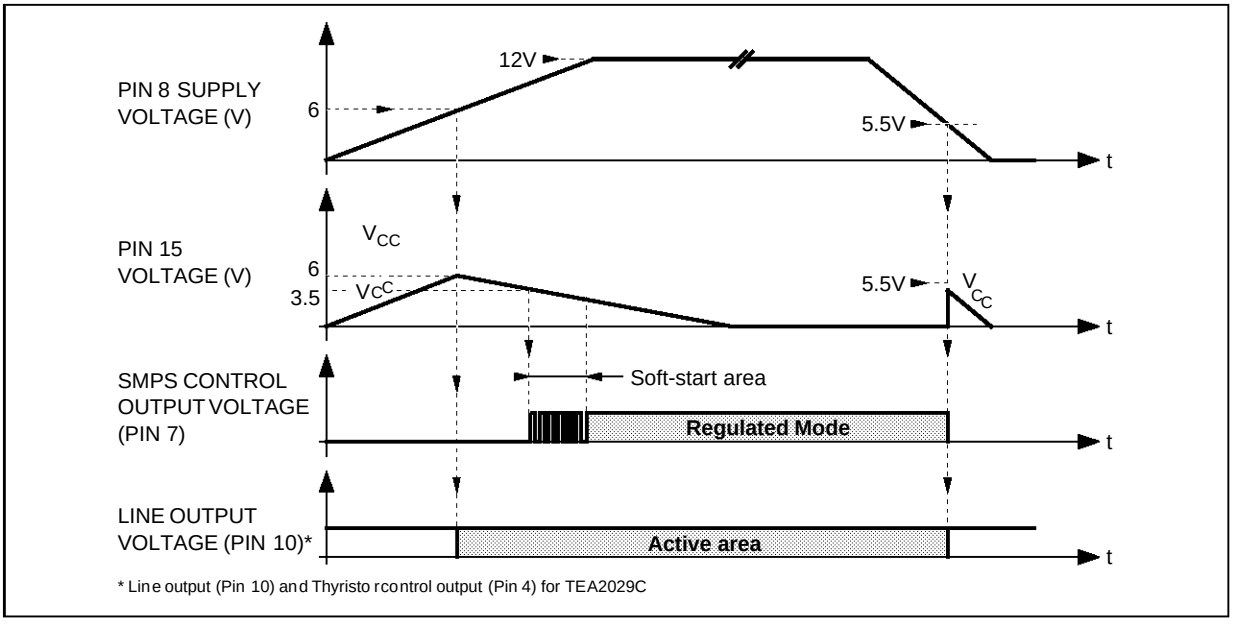
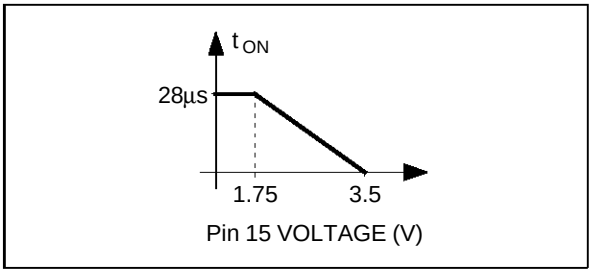


Figure 67



V.7.5 - Protection features

As soon as a safety signal ($V \leq 1.26V$) is applied to Pin 28, line and supply outputs (Pins 10 and 7) are both disabled. Capacitor "C15" begins charging up until the voltage across it reaches 4V ($K \cdot V_{CC}$). Outputs are again enabled and conduction period gradually increases as it occurs upon initial start-up.

The device will be definitively inhibited if the cycle of events is repeated 3 times.

For the device to restart, the internal 3-bit register should be reset which requires the V_{CC} to fall below 4V (see Figure 68).

Pin 15 charging current : $I_{C(AV)} = - I_{D(AV)} = - 3.1\mu A$

V.7.6 - TV Power supply in standby mode

V.7.6.1 - Regulation by primary controller circuit

This mode of regulation called "Burst Mode" is performed only by the primary controller circuit and is activated in the case of missing control pulses or in the absence of power supply to TEA2028B.
In this mode, power available through secondary winding is limited. Refer to TEA2164 Application Note for further details.
Higher powers can be obtained by using the regulation feature offered by TEA2028B. In this case, the horizontal output (Pin 10) must be disabled.

V.7.6.2 - Regulation by TEA2028 (see Figure 69)

In this case, all that is required is to disable the line scanning function thus reducing the overall power by 90%.
The device power supply regulation loop remains active, for minimum conduction period to be 1.5ms the power delivered through secondary must be higher than 3W.

Line Output Inhibition

Two alternatives are possible :
- Grounding flip-flop Pin 1
- Apply a voltage higher than 3V to Pin 12.

Figure 68

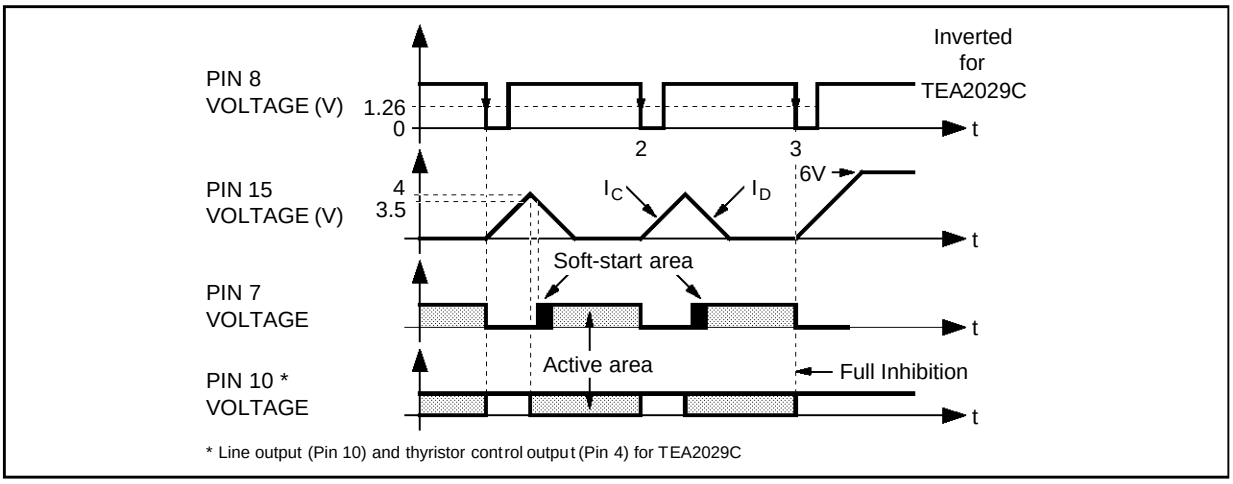
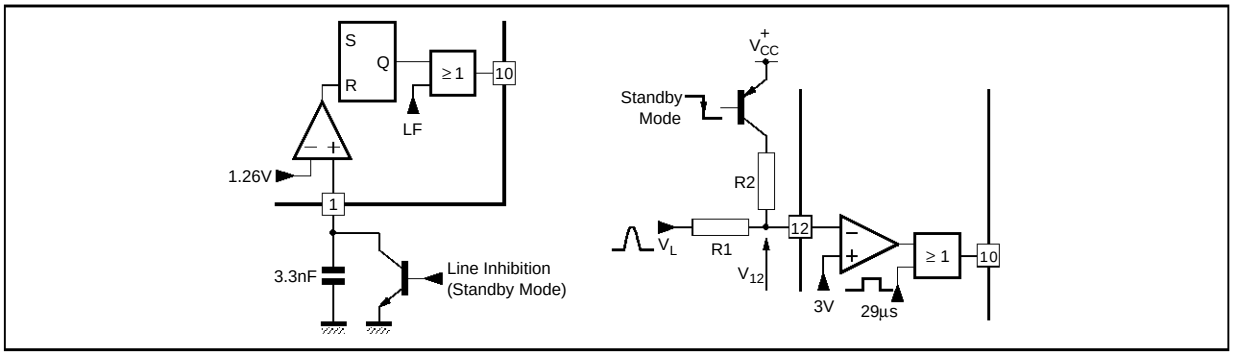


Figure 69



V.8 - Miscellaneous functions

V.8.1 - Super sandcastle signal generator

This signal used in video stage, is available on Pin 11.

It has 3 levels at specified time intervals :

- 2.5V level
  Used for vertical blanking at each frame flyback. Its duration is 21 lines and is generated by the frame logic.
  This level will be maintained if vertical scanning failure is detected on Pin 2.
- 4.5V level
  Used for horizontal blanking, its duration is determined by comparing the line flyback signal on Pin 12 to an internal voltage of 0.25V.
- 10V level
  This signal is used by color decoding stage. Its duration of 4µs is determined by line logic circuitry. With respect to the video signal on Pin 27, this level is positioned such that it is used to sample the burst frequency transmitted just after the sync pulse.

V.8.2 - Video and 50/60Hz standard recognition output

A 3-level signal is available at Pin 24 for video identification (Mute) and for 50 and 60Hz standards recognition.

Figure 70

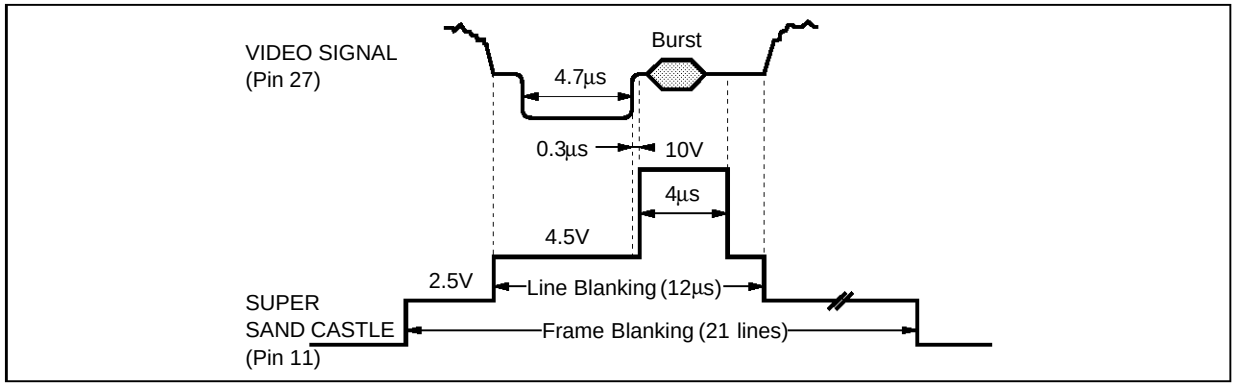
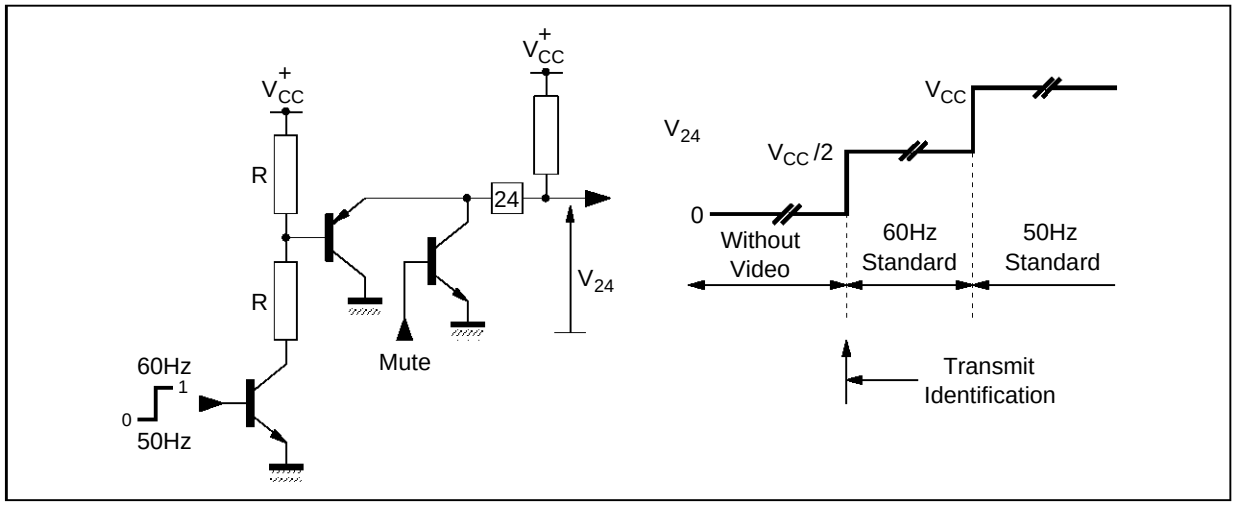
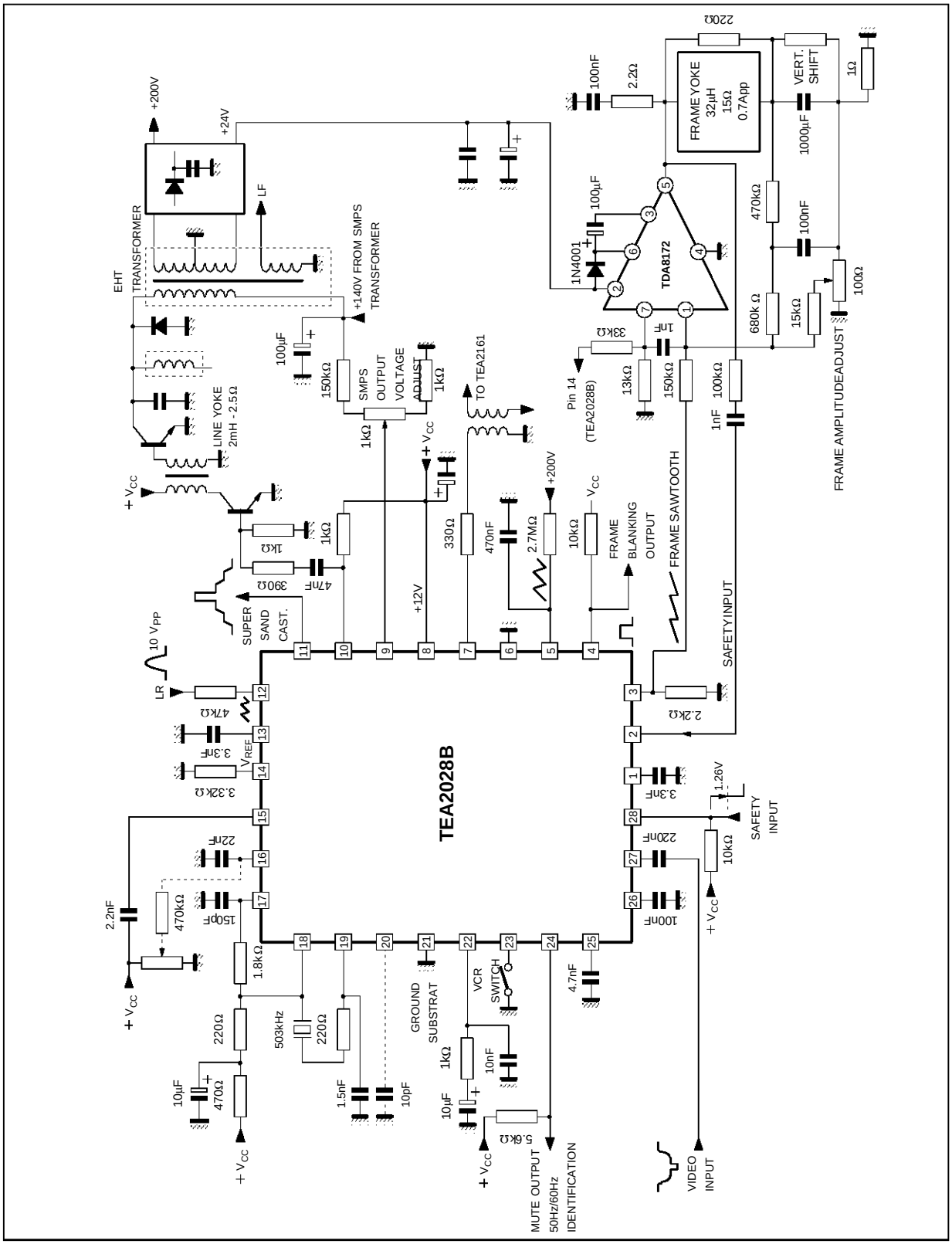


Figure 71



VI - TEA2028 APPLICATION DIAGRAM

Figure 72



VII - TEA2029 : DIFFERENCES WITH TEA2028

VII.1 - General

The TEA2029 has quite the same functions compared to TEA2028.
The main difference is that the TEA2029 incorporates a frame phase modulator intended to work with a switched mode vertical stage using a thyristor.
The TEA2029 can also be used with a linear vertical power amplifier such as the TDA8170.

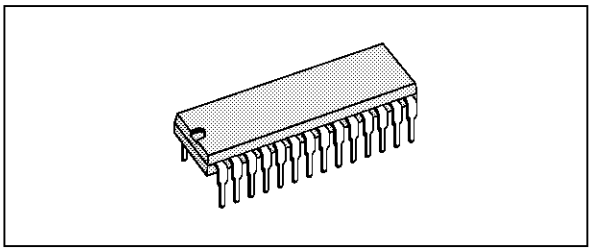
VII.2 - Pin by Pin Differences

Pin	TEA2029C	TEA2028B
1	Dfferential inputs of the frame error amplifier (including frame blanking safety in case of vertical stage failure).	Capacitor for horizontal output duration adjustment (29µs typ. with c1 = 3.3nF)
2		Vertical blanking safety input
4	Frame output for thyristor control	Vertical blanking output (21 lines duration)
10	Horizontal output (26µs typ. duration)	Horizontal output (duration is adjustable)
11	Supersandcastle output (with a frame blanking duration of 24 lines)	Supersandcastle output (with a frame blanking duration of 21 lines)
12	Negative horizontal flyback input (115 V_{PP} through a 47 kΩ resistor)	positive horizontal flyback input ($10V_{pp}$ through a 47kΩ resistor)
20	Positive AGC key pulse output (low level when no video)	Capacitor for frame sync. time constant adjustment
28	Safety input (inhibition of SMPS, Horizontal and Frame outputs when V_{28} > 1.26V)	Safety input (inhibition of SMPS, Horizontal outputs when V_{28} < 1.26V)

VII.3 - TEA2029C Pin Connections

Pin	Description
1	Frame error amplifier non-inverting input
2	Frame error amplifier inverting input
3	Frame saw-tooth output
4	Frame output (for thyristor control)
5	Frame ramp generator
6	Power Ground
7	SMPS control output
8	VCC Supply voltage
9	SMPS regulation input
10	Horizontal output
11	Supersandcastle output
12	Horizontal flyback input
13	Horizontal saw-tooth generator
14	Current reference
15	SMPS soft-start and safety time constant
16	ϕ2 phase comparator capacitor (and horizontal phase adjustment)
17	VCO phase shift network
18	VCO output
19	VCO input
20	AGC key pulse output
21	Substrate Ground
22	ϕ1 phase comparator capacitor
23	VCR switching input
24	Video and 50/60Hz identification output (Mute)
25	Video identification capacitor
26	Horizontal sync detection capacitor (50% of peak to peak sync level)
27	Video input
28	Safety input

Package : DIP28



DIP28.EPS

VII.4 - Frame Phase Modulator

The Tranconductance Amplifier "A1" converts the differential input voltage into two output currents "I_{S1}" and "I_{S3}".

- A1 transconductance = $\frac{I_{S1}}{V_{IN}} = 10\mu A/mV$
- B transconductance = $\frac{I_{S2}}{V_2} = 40\mu A/V$
- Transfer characteristic = $\frac{\Delta t_{OUT}}{\Delta V_{IN}} = 6.4\mu s/V$

The filter time constant is maximum near the operating point when $I_{S1} \cong I_{S2}$

In this case :
- The base current of T_1 = "I_{S2} - I_{S1}"
- The filter band-pass = 15kHz

The maximum conduction period of "40µs" is determined by the horizontal logic circuitry.

The frame frame flyback is detected by transistor "T3".

There is no feed-back during frame flyback and "I_{S3}" is maximum (higher than I_4) which will drive the "T3" into conduction.

Figure 73

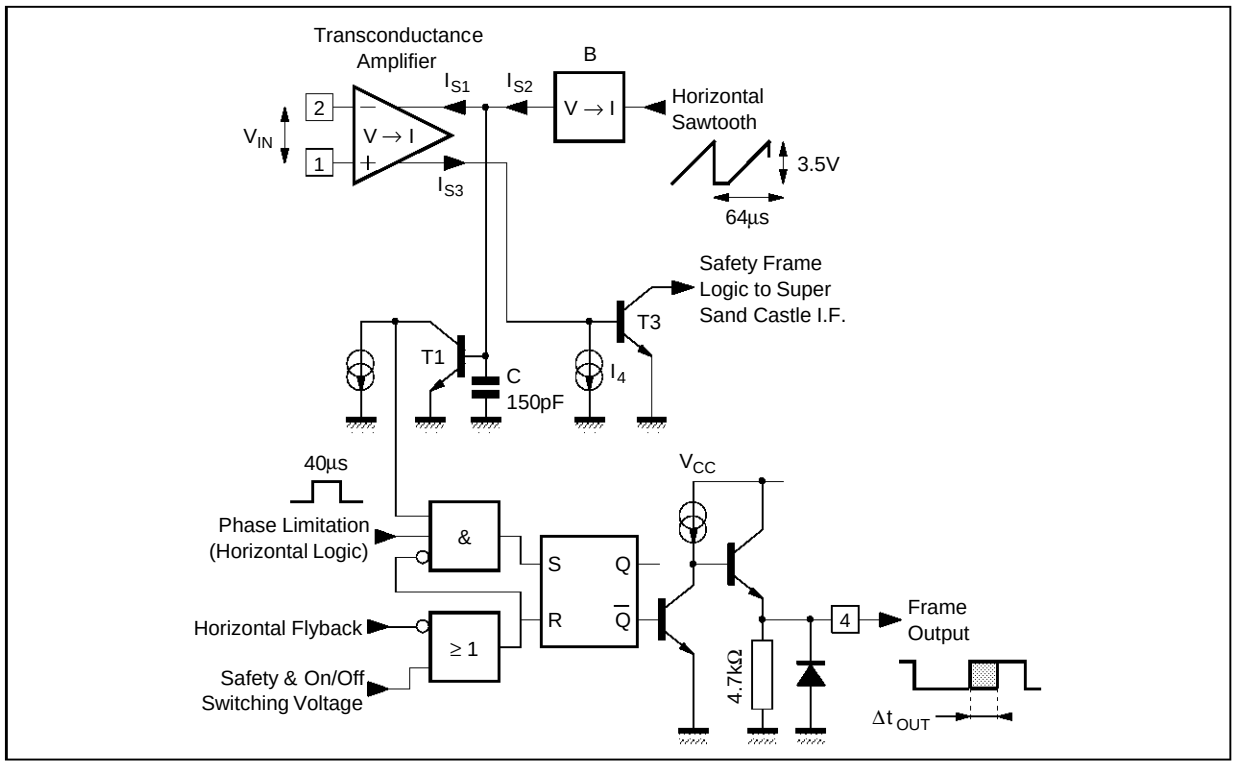
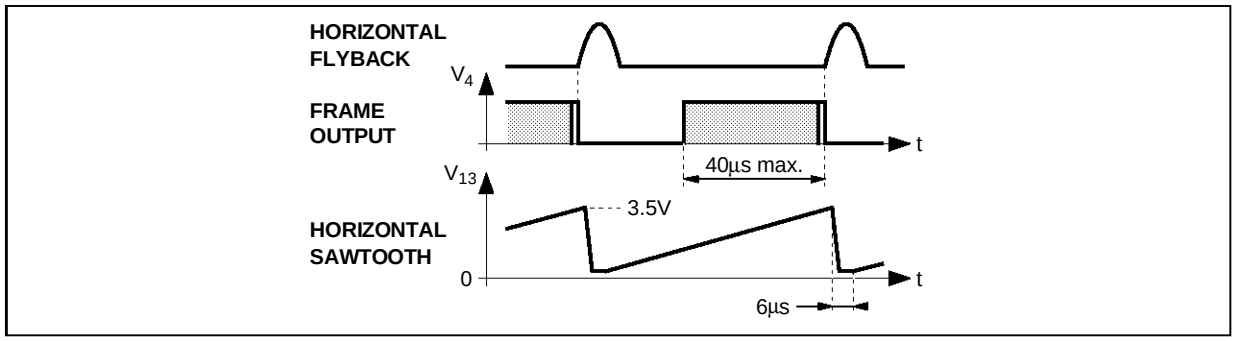


Figure 74



VII.5 - Frame Blanking Safety

- During trace : $I_{S3} < I_4 \Rightarrow$ T3 is blocked.
- During flyback : $I_{S3} > I_4 \Rightarrow$ T3 conducts.

In the absence of flyback detection or if the flyback interval is longer than the blanking time, the sand-castle low level remains constant at 2.5V so as to protect the picture tube in the absence of frame scanning.

- "IF" signal is delivered by Frame Error Amplifier (see Frame phase modulator figure)
- IF is high during the Frame Flyback interval

Figure 75 : Frame Blanking Safety Block Diagram

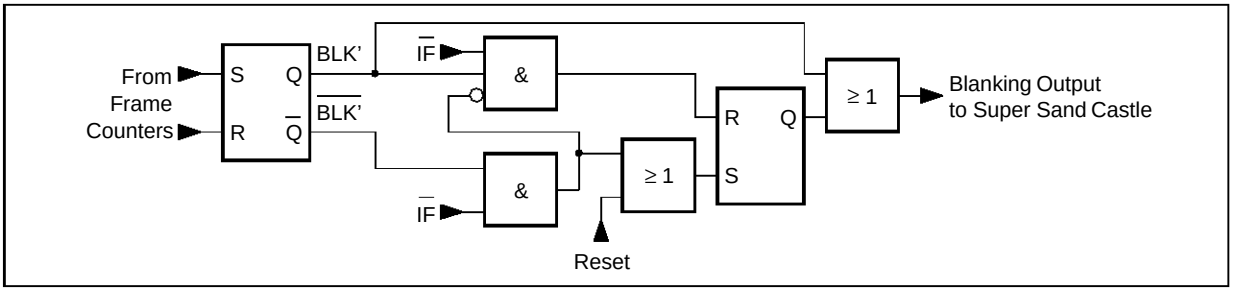
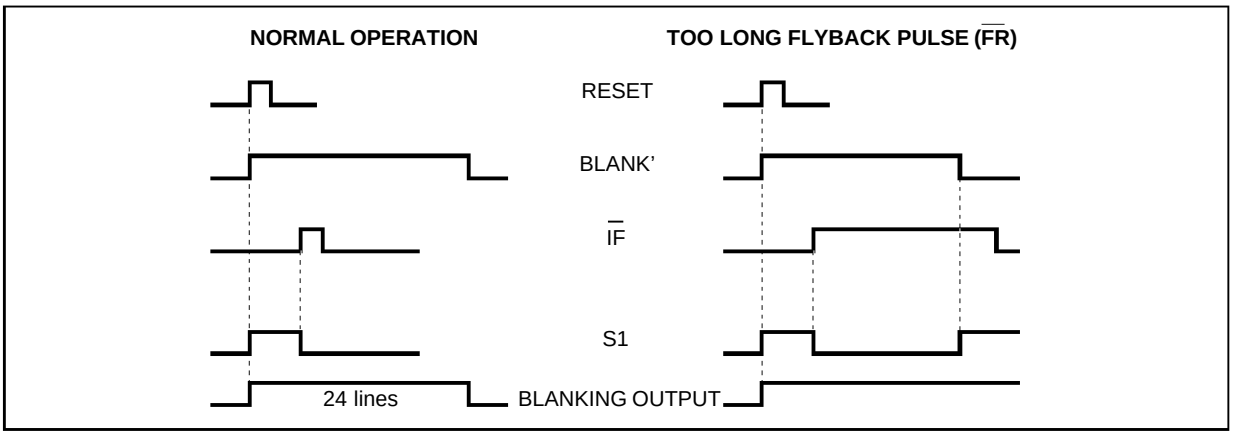


Figure 76



VII.6 - On-chip Line Flip-flop

Figure 77

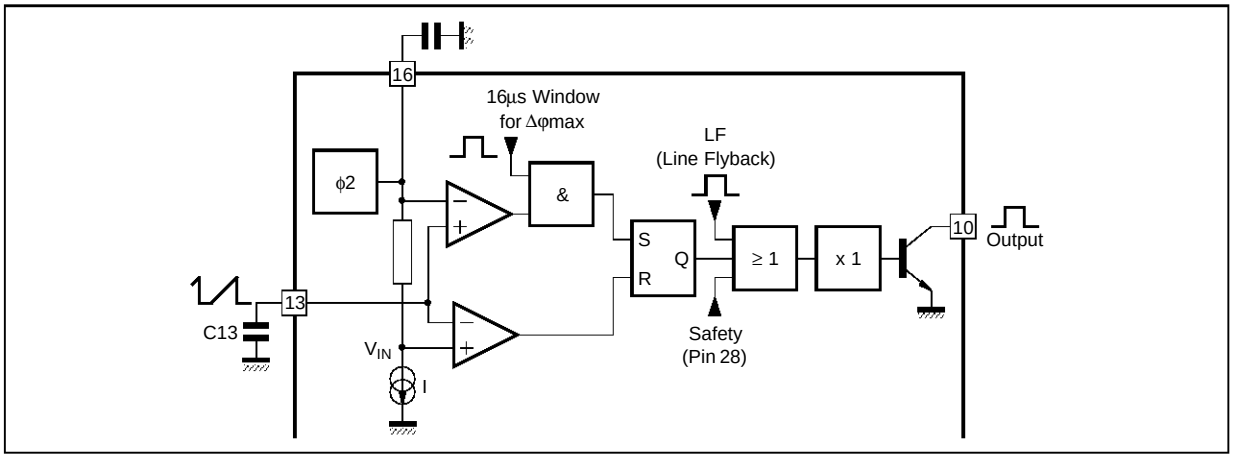
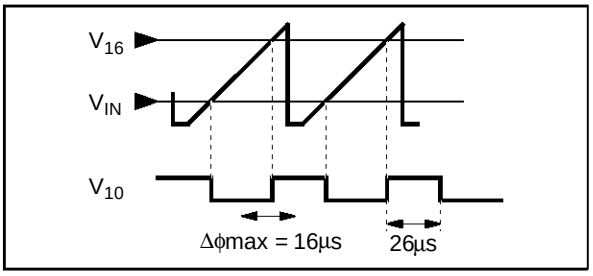


Figure 78



$T_{10} = 35 \cdot T_{VCO} - K \cdot R14 \cdot C13$

$= 70 \cdot 10^{-6} - 4 \cdot R14 \cdot C13$

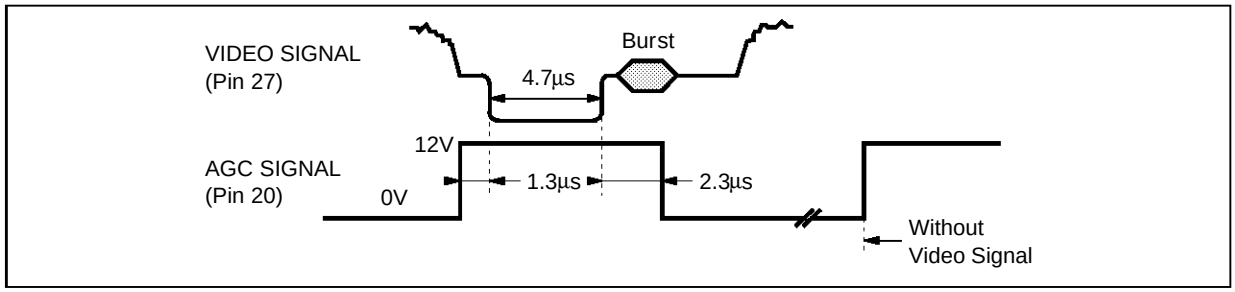
Where T_{VCO} is the V_{CO} period of oscillation on pin 18.

- If in synchronized mode :
  $T_{VCO} = 2\mu s$,
  $R14 = 3.32k\Omega$
  $C13 = 3.3nF$

Therefore $T_{10} = 26\mu s$ (nominal value)

VII.7 - AGC Key Pulse

Figure 79



As illustrated below, this signal is used in some TV sets to perform sampling window for Automatic Gain Control of picture demodulation network.

This system is called "clamped" AGC, and locks the demodulated line sync amplitude and hence sets the video signal amplitude.

This signal generated by line logic circuitry is correctly positioned by the first phase locked loop "ϕ1" and includes the line sync pulse of the video signal. This is an open-collector output.

VIII - APPLICATION INFORMATION ON FRAME SCANNING IN SWITCHED MODE

(TEA2029 ONLY)

VIII.1 - Fundamentals (see Figure 80)

The secondary winding of EHT transformer provides the energy required by frame yoke.

The frame current modulation is achieved by modulating the horizontal saw-tooth current and subsequent integration by a "L.C" network to reject the horizontal frequency component.

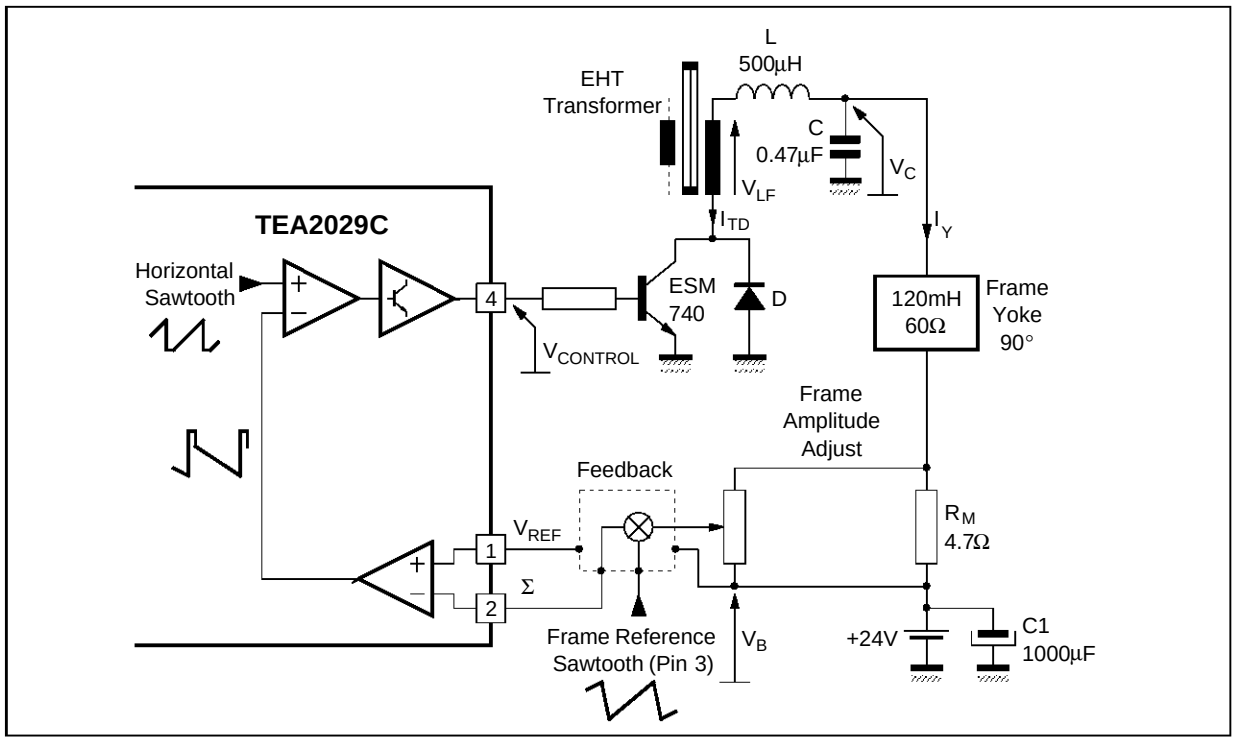
VIII.2 - General Description

The basic circuit is the phase comparator "C_1" which compares the horizontal saw-tooth and the output voltage of Error Amplifier "A".
The comparator output will go "high" when the horizontal saw-tooth voltage is higher than the "A" output voltage. Thus, the Pin 4 output signal is switched in synchronization with the horizontal frequency and the duty cycle is modulated at frame frequency.
A driver stage delivers the current required by the external power switch.
The external thyristor provides for energy transfer between transformer and frame yoke.
The thyristor will conduct during the last portion of horizontal trace phase and for half of the horizontal retrace.
The inverse parallel-connected diode "D" conducts during the second portion of horizontal retrace and at the beginning of horizontal trace phase.

Main advantages of this system are :

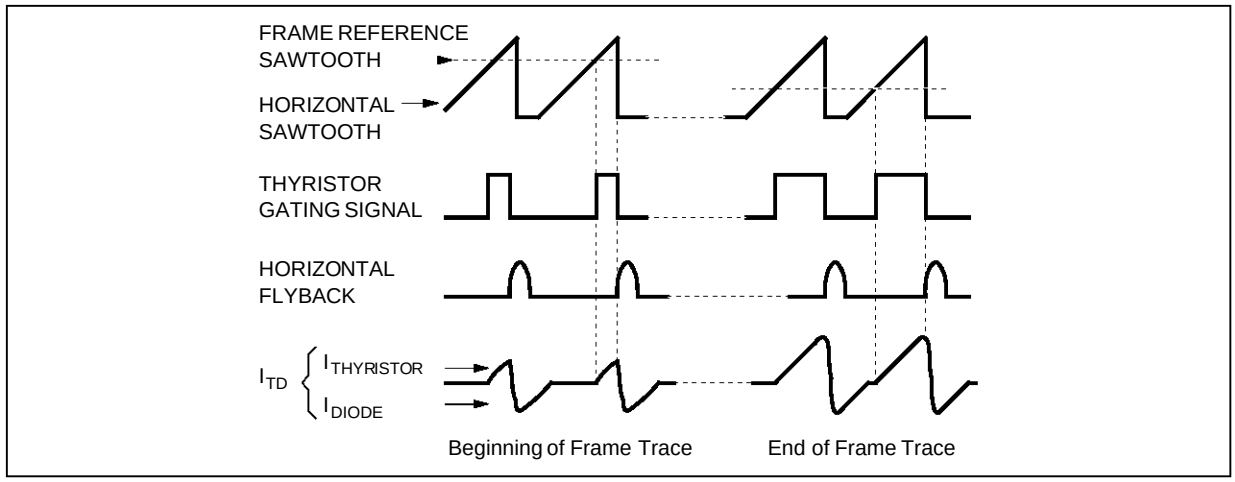
- **Power thyristor soft "turn-on"**
  Once the thyristor has been triggered, the current gradually rises from 0 to IP, where IP will reach the maximum value at the end of horizontal trace. The slope current is determined by, the current available through the secondary winding, the yoke impedance and the "L.C." filter characteristics.
- **Power thyristor soft "turn-off"**
  The secondary output current begins decreasing and falls to 0 at the middle of retrace. The thyristor is thus automatically "turned-off".
- **Excellent efficiency of power stage** due to very low "turn-on" and "turn-off" switching losses.

Figure 80 : Block Diagram



VIII.3 - Typical Frame Modulator and Frame Output Waveforms

Figure 81



VIII.4 - Frame Power Stage Waveforms

Figure 82

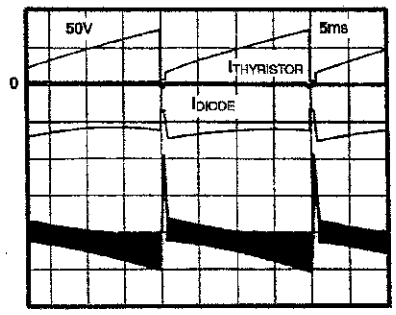


Figure 83

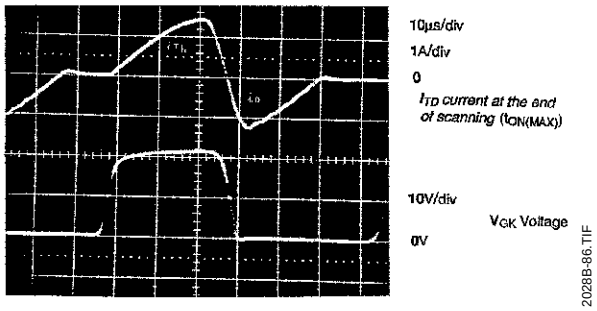


Figure 84

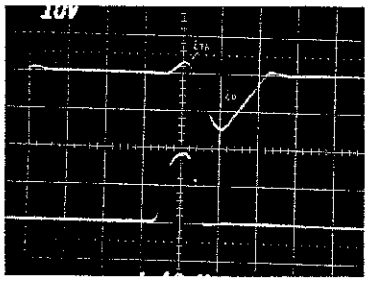


Figure 85 : Different Horizontal Conducting Times during Frame

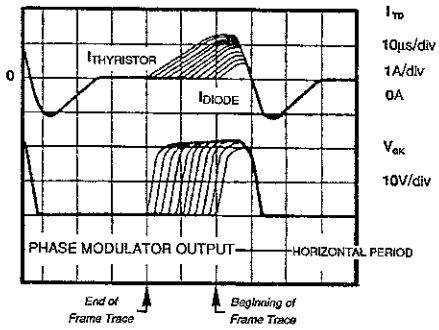


Figure 86

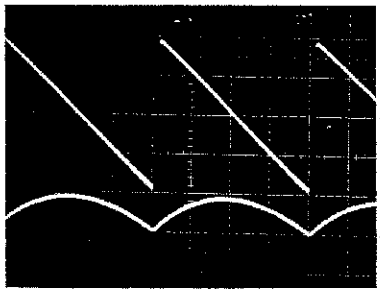
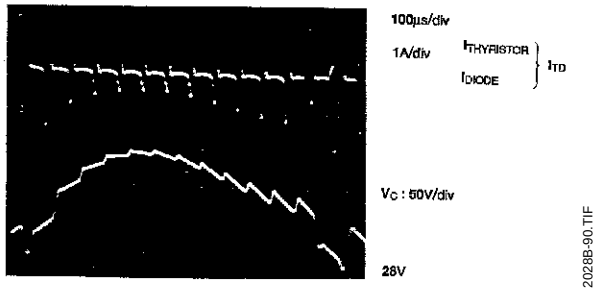


Figure 87



The bias voltage "V_B" is supplied by the secondary winding of EHT transformer. The parabolic effect is due to the integration of frame saw-tooth by the filtering capacitor "C1".

$$DVB = \frac{I_Y \cdot T}{8 \cdot C1} = 0.95V$$

Where :
- I_Y : Peak-to-peak yoke current = 380mA$_{pp}$
- T : 20ms
- C1 = 1000µF

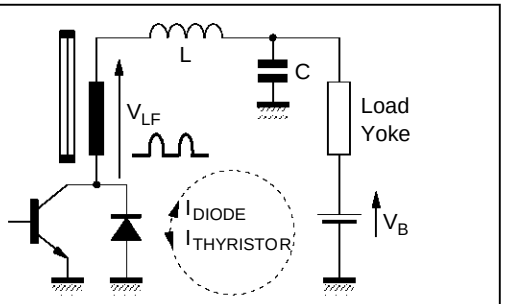
VIII.5 - Frame Flyback

During flyback, due to the loop time constant, the frame yoke current cannot be locked onto the reference saw-tooth. Thus the output of amplifier "A" will remain high and the thyristor is blocked.

The scanning current will begin flowing through diode "D". As a consequence, the capacitor "C" starts charging up to the flyback voltage. The thyristor is triggered as soon as the yoke current reaches the maximum positive value.

EHT transformer winding (see Figure 88)
(for 90° tube : Yoke ⇒ L = 120mH, r_Y = 60Ω)

Figure 88



- V_{LF} = 210V$_{PP}$
- C = 0.47µF
- I_{YOKE} = 380mA$_{PP}$
- $V_{LF} \approx 9.2\ I_{Y(PP)} \cdot r_Y$
- L = 500µH
- Flyback duration = 1ms

2028B-91.EPS

VIII.6 - Feed-back Circuit

VIII.6.1 - Frame power in quasi-bridge configuration (see Figure 89)

This stage measures the frame scanning current in differential mode and compares it to the reference saw-tooth on Pin 3.

The overall configuration is built around two symmetrical networks :
- "R_1, R_2, R_3" network : determines the dynamic saw-tooth voltage
- "R'_1, R'_2, R'_3" network : sets the bias voltage and the d.c. shift control.

$$\text{A.C. gain : } G = \frac{R_2}{R_1} = \frac{I_Y}{V_{IN}} \cdot \alpha \cdot R_M$$

where :
- I_Y : Peak-to-peak Yoke Current
- V_{IN} : Peak-to-peak saw-tooth voltage (Pin 3)
- $\alpha \in [0,1]$: amplitude adjustment

VIII.6.1.1 - Choice of "R" value

The saw-tooth generator output is an emitter follower stage. Pin 3 output current must therefore be always negative.

$$R << R1 \frac{V_{IN(Min.)}}{V_{BIAS} - V_{IN(Min.)}}$$

Where :
- V_{BIAS} : Bias voltage for Pins 1 and 2
- $V_{IN(MIN)}$: Saw-tooth voltage low level

Example :
- R1 = 22kΩ
- V_{BIAS} = 5V
- $V_{IN(Min.)}$ = 1.26V

$$\Rightarrow R \approx \frac{R_1}{10}$$

VIII.6.1.2 - Influence of R3 value

R_3 sets the bias voltage for Pins 1 and 2. This voltage should be lower than 5.5V so as to enable the frame to function upon initial start-up at V_{CC} = 6V.
If the bias voltage is higher than this 5.5V level, the d.c. open-loop gain will fall thereby rendering the system more sensitive to d.c. drift.

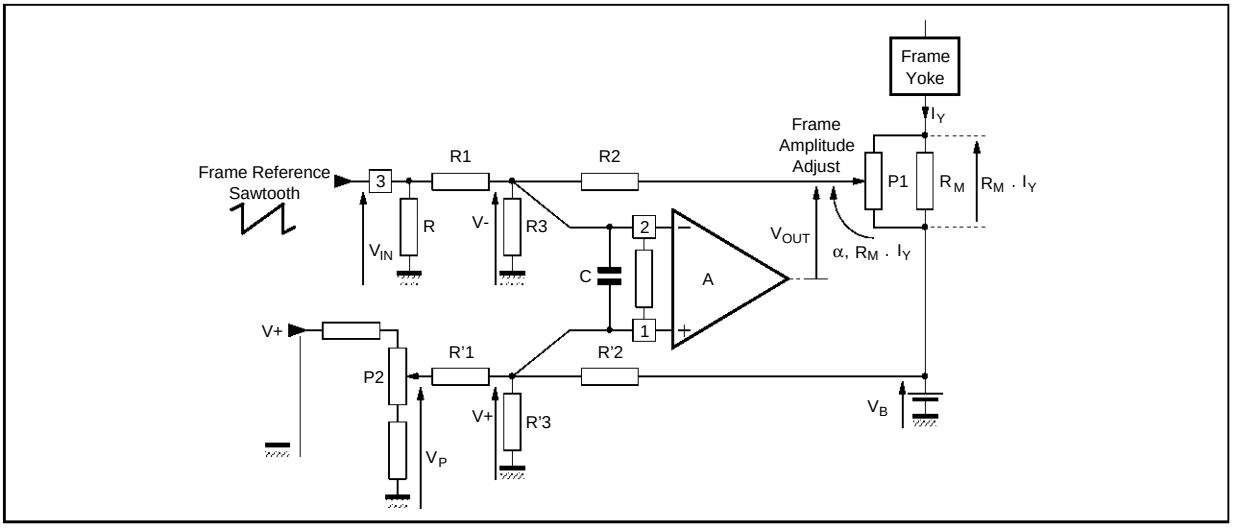
Satisfactory results are obtained at V_{BIAS} values falling within 4V to 5V range.

$$R3 = R2 \frac{V_{BIAS}}{V_B\,[V_{IN(MEAN)} \cdot G] - V_{BIAS}\,[1 - G]}$$

Where : $V_{IN(MEAN)}$: saw-tooth mean value (Pin 3)

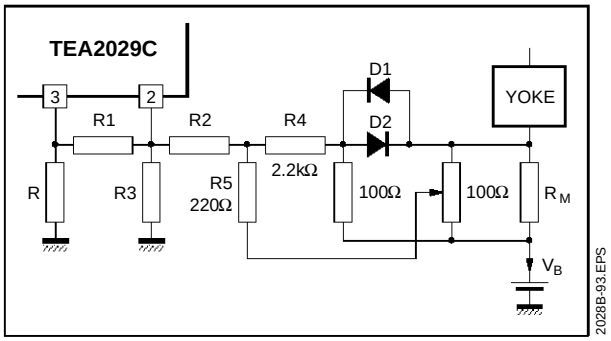
Capacitor "C" connected between Pins 1 and 2 determines the system stability. Its value must be appropriately calculated as a function of "R_1, R_2 and R_3" values so as to reject the line frequency component.

Figure 89



VIII.6.1.3 - "S" Correction circuit in quasi-bridge configuration

Figure 90



The "S" correction waveform is obtained using the non-linear "V_{DIODE}" versus "I_{DIODE}" characteristics of "D1" and "D2" diodes.

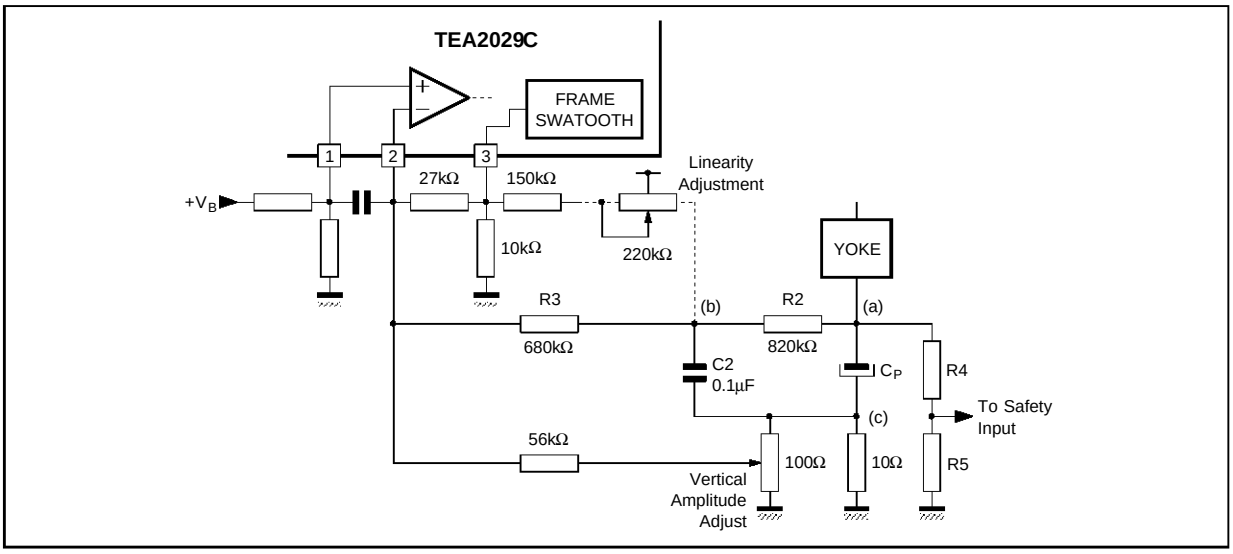
The signal pre-corrected by "D1", "D2" diodes and the feed-back signal through "R5", are summed at "A". The "S" correction level is determined by the ratio between "R4" and "R5" resistors.

VIII.6.2 - Frame scanning in switched mode using coupling capacitor (see Figure 91)

The parabolic voltage at (a) is integrated by "R2, C2" network and used for "S" correction.

The "S" waveform voltage at (b) is added to the saw-tooth voltage at (c). The "S" level is determined by "C2, R2, R3" network.

Figure 91



VIII.6.3 - Frame safety

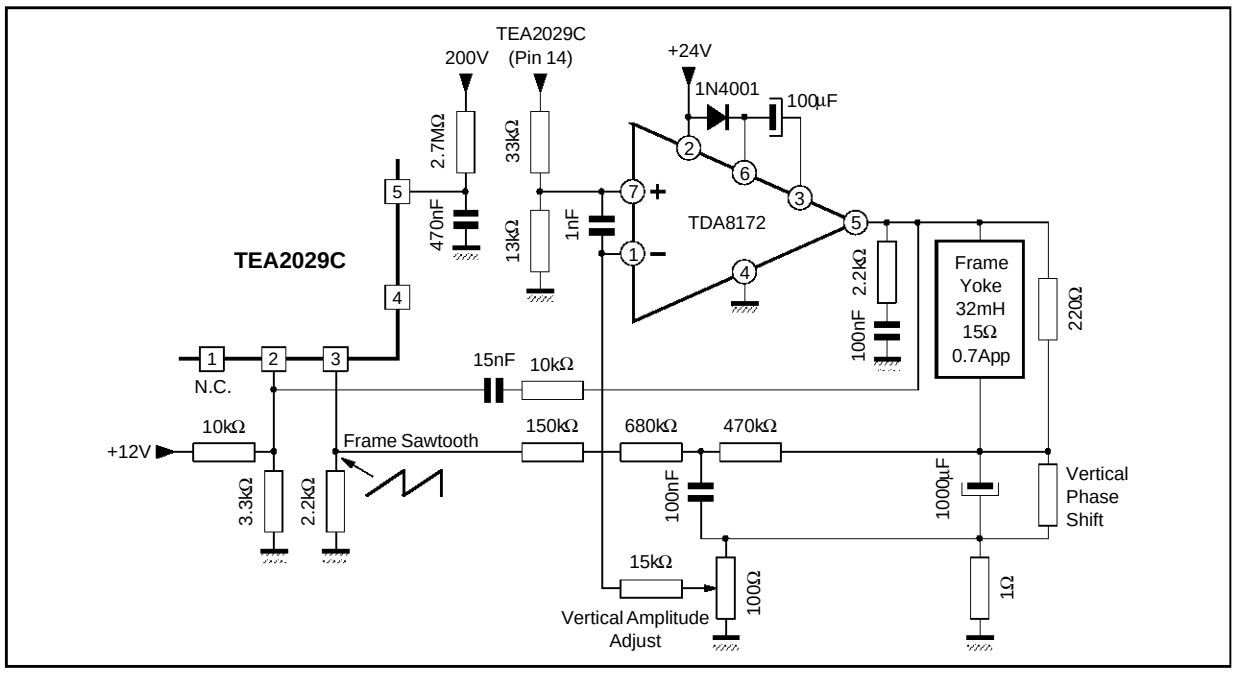
In case of failure in the loop, the thyristor may remain turned-off while the inverse parallel-connected diode conducts. This will result in a hazardeous situation where the voltage across the coupling capacitor "C_P" will reach an excessively high value.

To avoid such situation, the voltage at point (a) should be applied to the "Safety" input Pin 28 after it has gone through the matching network "R4, R5".

VIII.7 - Frame Scanning in Class B with Flyback Generator

VIII.7.1 - Application diagram

Figure 92



IX - TEA2029 APPLICATION DIAGRAM

Complete application with TEA2164

Figure 93