TFP510
TI *PanelBus*™ DIGITAL TRANSMITTER

SLDS146B – JANUARY 2002 – REVISED DECEMBER 2002

- Digital Visual Interface (DVI) Compliant[1]
- Supports Resolutions From VGA to UXGA (25-MHz–165-MHz Pixel Rates)
- Universal Graphics Controller Interface
  - 12-Bit, Dual-Edge and 24-Bit, Single-Edge Input Modes
  - Adjustable 1.1-V to 1.8-V and Standard 3.3-V CMOS Input Signal Levels
  - Fully Differential and Single-Ended Input Clocking Modes
  - Standard Intel 12-Bit Digital Video Port Compatible as on Intel™ 81x Chipsets
- Enhanced PLL Noise Immunity
  - On-Chip Regulators and Bypass Capacitors for Reducing Systems Costs
- Enhanced Jitter Performance
  - No HSYNC Jitter Anomaly
  - Negligible Data-Dependent Jitter
- Programmable Using I²C Serial Interface
- Monitor Detection Through Hot-Plug and Receiver Detection
- Single 3.3-V Supply Operation
- 64-Pin TQFP Using TI's PowerPAD™ Package
- TI's Advanced 0.18 µm EPIC-5™ CMOS Process Technology
- Pin Compatible With Sil164 and Sil168 DVI Transmitters
- High-Bandwidth Digital Content Protection (HDCP) Specifications Compliant[2]

description

The TFP510 is a Texas Instruments *PanelBus* flat panel display product, part of a comprehensive family of end-to-end DVI 1.0 compliant solutions, targeted at the PC and consumer electronics industry.

The TFP510 provides a universal interface to allow a glueless connection to most commonly available graphics controllers. Some of the advantages of this universal interface include selectable bus widths, adjustable signal levels, and differential and single-ended clocking. The adjustable 1.1-V to 1.8-V digital interface provides a low-EMI, high-speed bus that connects seamlessly with 12-bit or 24-bit interfaces. The DVI interface supports flat panel display resolutions up to UXGA at 165 MHz in 24-bit true color pixel format.

The TFP510 combines *PanelBus* circuit innovation with TI's advanced 0.18 µm EPIC-5 CMOS process technology and TI's ultralow ground inductance PowerPAD package. The result is a compact 64-pin TQFP package providing a reliable, low-noise, high-speed digital interface solution.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Footnotes:

1. The digital visual interface (DVI) specification is an industry standard developed by the digital display working group (DDWG) for high-speed digital connection to digital displays. The TFP510 is compliant to the digital visual interface (DVI) Revision 1.0 specification. The DVI 1.0 specification has been adopted by the industry leading PC and consumer electronics manufacturers.
2. .The high–bandwidth digital content protection system (HDCP) is an industry standard for protecting DVI outputs from being copied. HDCP was developed by Intel Corporation and is licensed by the Digital Content Protection, LLC. The TFP510 is compliant to the HDCP Rev. 1.0 specification.

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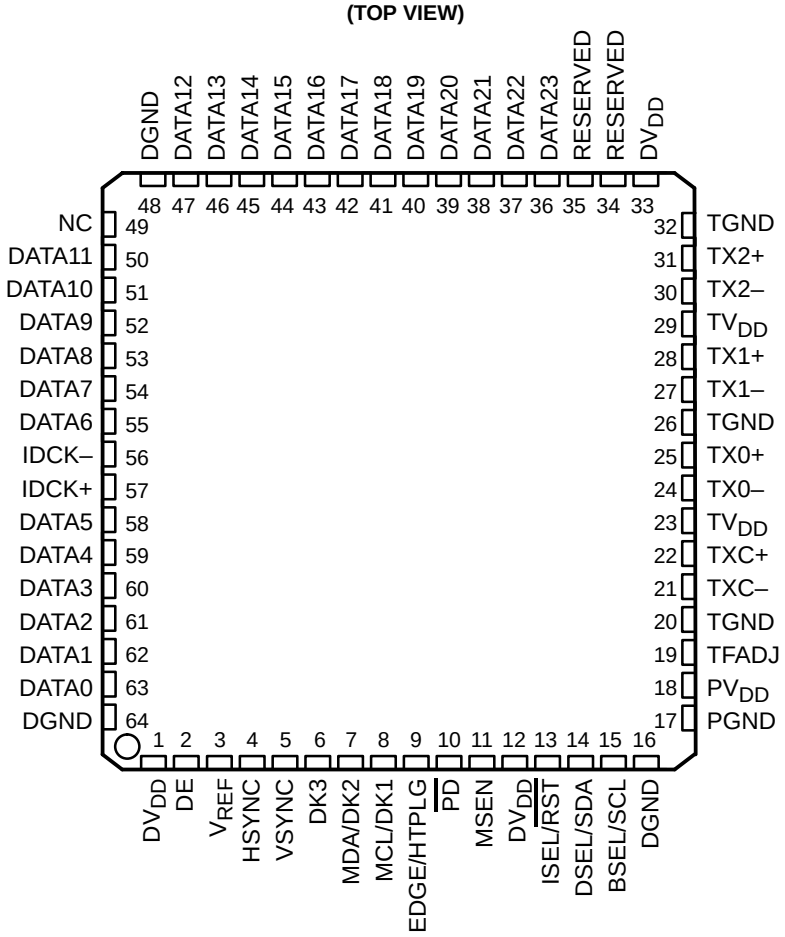
Intel is a trademark of Intel Corporation.

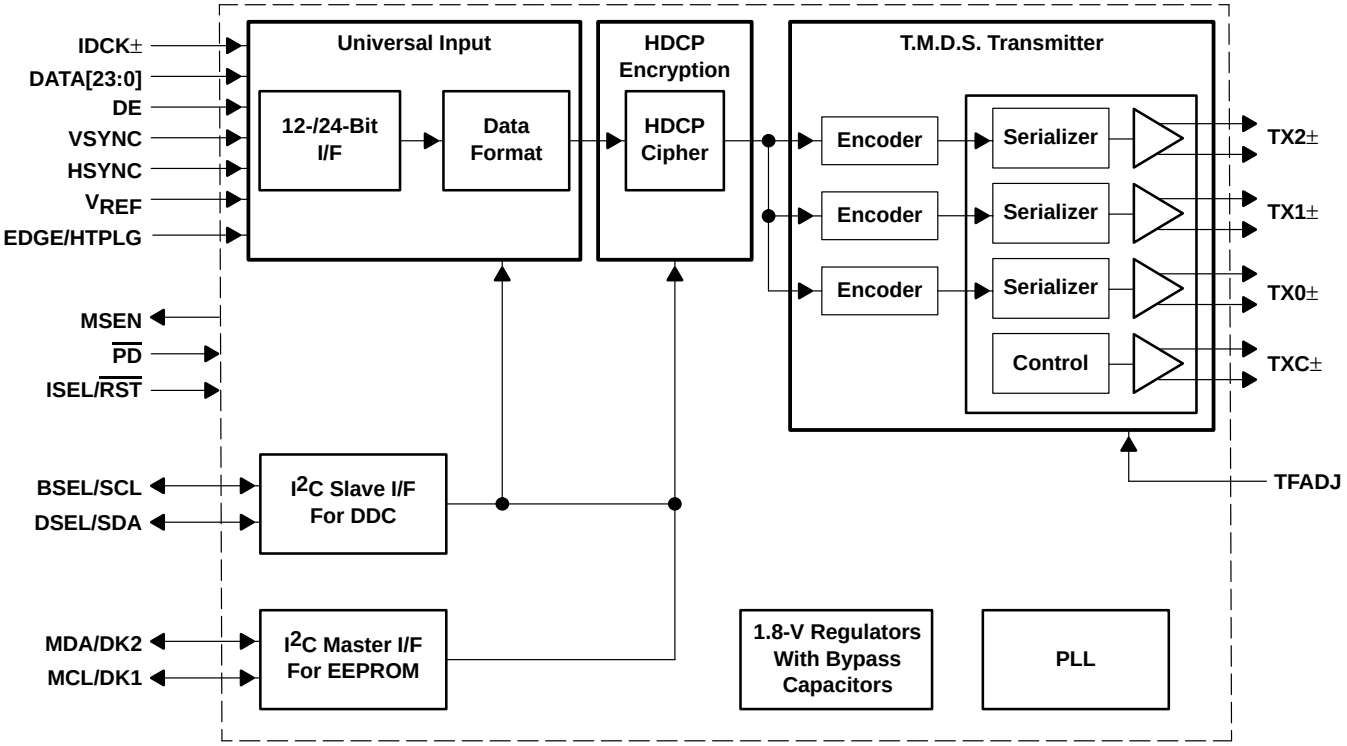
This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

pin assignments

PAP PACKAGE
(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Input Pins			
DATA[23:12]	36–47	I	The upper 12 bits of the 24-bit pixel bus. In 24-bit, single-edge input mode (BSEL = high), this bus inputs the top half of the 24-bit pixel bus. In 12-bit, dual-edge input mode (BSEL = low), these bits are not used to input pixel data. In this mode, the state of DATA[23:16] is input to the I^2C register CFG. This allows 8 bits of user configuration data to be read by the graphics controller through the I^2C interface (see the I^2C *register descriptions* section). Note: All unused data inputs should be tied to GND or V_{DD}.
DATA[11:0]	50–55, 58–63	I	The lower 12 bits of the 24-bit pixel bus/12-bit pixel bus input. In 24-bit, single-edge input mode (BSEL = high), this bus inputs the bottom half of the 24-bit pixel bus. In 12-bit, dual-edge input mode (BSEL = low), this bus inputs 1/2 a pixel (12 bits) at every latch edge (both rising and falling) of the clock.
DE	2	I	Data enable. As defined in the DVI 1.0 specification, the DE signal allows the transmitter to encode pixel data or control data on any given input clock cycle. During active video (DE = high), the transmitter encodes pixel data, DATA[23:0]. During the blanking interval (DE = low), the transmitter encodes HSYNC, VSYNC, and CTL[3:1].

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Input Pins (Continued)			
DK3 MDA/DK2 MCL/DK1	6 7 8	I/O	The operation of these three multifunction inputs depends on the setting of the ISEL (pin 13) input. All three inputs support 3.3-V CMOS signal levels and contain weak pulldown resistors so that if left unconnected they default to all low. When the I^2C bus is disabled (ISEL = low), then these three inputs become the de-skew inputs, DK[3:1], used to adjust the setup and hold times of the pixel data inputs, DATA[23:0], relative to the clock input, IDCK±. When the I^2C bus is enabled (ISEL = high), MDA and MCL are open-drain I/O pins used for the I^2C interface to the key EEPROM, which can be used by the HDCP. In this case, MCL is the memory clock signal, while MDA is the memory data signal. The DK3 pin is not used in this mode. Pins 7–8 require a 5-kΩ resistor connected to V_{DD} when used for EEPROM I^2C interface.
HSYNC	4	I	Horizontal sync input
IDCK– IDCK+	56 57	I	Differential clock input. The TFP510 supports both single-ended and fully differential clock input modes. In the single-ended clock input mode, the IDCK+ input (pin 57) should be connected to the single-ended clock source and the IDCK input (pin 56) should be tied to GND. In the differential clock input mode, the TFP510 uses the crossover point between the IDCK+ and IDCK– signals as the timing reference for latching incoming data DATA[23:0], DE, HSYNC, and VSYNC. The differential clock input mode is only available in the low-signal-swing mode.
VSYNC	5	I	Vertical sync input
Configuration/Programming Pins			
BSEL/SCL	15	I/O	Input bus select / I^2C clock input. The operation of this pin depends on whether the I^2C interface is enabled or disabled. This pin is only 3.3-V tolerant. When I^2C is disabled (ISEL = low), a high level selects 24-bit input, single-edge input mode. A low level selects 12-bit input, dual-edge input mode. When I^2C is enabled (ISEL = high), this pin functions as the I^2C clock input (see the I^2C *register descriptions* section). In this configuration, this pin has an open-drain output that requires an external 5-kΩ pullup resistor connected to V_{DD}.
DSEL/SDA	14	I/O	DSEL/I^2C data. The operation of this pin depends on whether the I^2C interface is enabled or disabled. This pin is only 3.3-V tolerant. When I^2C is disabled (ISEL = low), this pin is used with BSEL and V_{REF} to select the single-ended or differential input clock mode (see the *universal graphics controller interface modes* section). When I^2C is enabled (ISEL = high), this pin functions as the I^2C bidirectional data line. In this configuration, this pin has an open-drain output that requires an external 5-kΩ pullup resistor connected to V_{DD}.
EDGE/HTPLG	9	I	Edge select/hot plug input. The operation of this pin depends on whether the I^2C interface is enabled or disabled. This input is 3.3-V tolerant only. When I^2C is disabled (ISEL = low), a high level selects the primary latch to occur on the rising edge of the input clock IDCK+. A low level selects the primary latch to occur on the falling edge of the input clock IDCK+. This is the case for both single-ended and differential input clock modes. When I^2C is enabled (ISEL = high), this pin is used to monitor the hot plug detect signal (see the DVI or VESA™ P&D and DFP standards). When used for hot-plug detection, this pin requires a series 1-kΩ resistor.
ISEL/$\overline{\text{RST}}$	13	I	I^2C interface select / I^2C RESET (active low, asynchronous). If ISEL is high, then the I^2C interface is active. Default values for the I^2C registers can be found in the I^2C *register descriptions* section. If ISEL is low, then I^2C is disabled and the chip configuration is specified by the configuration pins (BSEL, DSEL, EDGE, V_{REF}) and state pins ($\overline{\text{PD}}$, DKEN). If ISEL is brought low and then back high, the I^2C state machine is reset. The register values are changed to their default values and are not preserved from before the reset.

Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Configuration/Programming Pins (Continued)			
MSEN	11	O	Monitor sense/programmable output 1. The operation of this pin depends on whether the I^2C interface is enabled or disabled. This pin has an open-drain output and is only 3.3-V tolerant. An external 5-kΩ pullup resistor connected to V_{DD} is required on this pin. When I^2C is disabled (ISEL = low), a low level indicates a powered on receiver is detected at the differential outputs. A high level indicates a powered-on receiver is not detected. This function is valid only in dc-coupled systems. When I^2C is enabled (ISEL = high), this output is programmable through the I^2C interface (see the I^2C *register descriptions*).
$\overline{PD}$	10	I	Power down (active low). In the power-down state only the digital I/O buffers and I^2C interface remain active. When I^2C is disabled (ISEL = low), a high level selects the normal operating mode. A low level selects the power-down mode. When I^2C is enabled (ISEL = high), the power-down state is selected through I^2C. In this configuration, the $\overline{PD}$ pin should be tied to GND. Note: The default register value for $\overline{PD}$ is low, so the device is in power-down mode when I^2C is first enabled or after an I^2C RESET.
V_{REF}	3	I	Input reference voltage. Selects the swing range of the digital data inputs (DATA[23:0], DE, HSYNC, VSYNC, and IDCK±). For high-swing 3.3-V input signal levels, V_{REF} should be tied to V_{DD}. For low-swing input signal levels, V_{REF} should be set to half of the maximum input voltage level. See the *recommended operating conditions* section for the allowable range for V_{REF}. The desired V_{REF} voltage level is typically derived using a simple voltage divider circuit.
Reserved			
NC	49	I	No connection required. If connected, tie high.
RESERVED	34, 35	I	These pins are reserved and must be tied to GND for normal operation.
DVI Differential Signal Output Pins			
TFADJ	19	I	Full-scale adjust. This pin controls the amplitude of the DVI output voltage swing, determined by the value of the pullup resistor R_{TFADJ} connected to TV_{DD}.
TX0+ TX0–	25 24	O	Channel-0 DVI differential output pair. TX0± transmits the 8-bit blue pixel data during active video and HSYNC and VSYNC during the blanking interval.
TX1+ TX1–	28 27	O	Channel-1 DVI differential output pair. TX1± transmits the 8-bit green pixel data during active video and CTL[1] during the blanking interval.
TX2+ TX2–	31 30	O	Channel-2 DVI differential output pair. TX2± transmits the 8-bit red pixel data during active video and CTL[3:2] during the blanking interval.
TXC+ TXC–	22 21	O	DVI differential output clock.

Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Power and Ground Pins			
DGND	16, 48, 64		Digital ground
DV_{DD}	1, 12, 33		Digital power supply. Must be set to 3.3 V nominal
PGND	17		PLL ground
PV_{DD}	18		PLL power supply. Must be set to 3.3 V nominal
TGND	20, 26, 32		Transmitter differential output driver ground
TV_{DD}	23, 29		Transmitter differential output driver power supply. Must be set to 3.3 V nominal

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, DV_{DD}, PV_{DD}, TV_{DD} . . . . . –0.5 V to 4 V
Input voltage, logic/analog signals . . . . . –0.5 V to 4 V
External DVI single-ended termination resistance, $r_{(T)}$ . . . . . 0 Ω to open circuit
External TFADJ resistance, $r_{(TFADJ)}$ . . . . . 300 Ω to open circuit
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds . . . . . 260°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds . . . . . 260°C
ESD protection, DVI pins . . . . . 4 kV Human body model
ESD protection, all other pins . . . . . 2 kV Human body model
JEDEC latchup (EIA/JESD78) . . . . . 100 mA

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (DV_{DD}, PV_{DD}, TV_{DD})		3	3.3	3.6	V
Input reference voltage, V_{REF}	Low-swing mode	0.55	$V_{DDQ}/2$†	0.9	V
	High-swing mode			DV_{DD}	
DVI termination supply voltage, AV_{DD} (see Note 1)	At DVI receiver	3.14	3.3	3.46	V
DVI Single-ended termination resistance, $r_{(T)}$ (see Note 2)	At DVI receiver	45	50	55	Ω
TFADJ resistor for DVI-compliant $V_{(SWING)}$ range, $r_{(TFADJ)}$	400 mV = $V_{(SWING)}$ = 600 mV	505	510	515	Ω
Operating free-air temperature range, T_A		0	25	70	°C

† V_{DDQ} defines the maximum low–level input voltage, it is not an actual input voltage.

NOTES: 1. AV_{DD} is the termination supply voltage of the DVI link.
2. $r_{(T)}$ is the single-ended termination resistance at the receiver end of the DVI link.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

dc specifications

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High–level input voltage (CMOS input)	$V_{REF} = DV_{DD}$	$0.7V_{DD}$			V
		$0.55\ V \le V_{REF} \le 0.9\ V$	$V_{REF} + 0.2$			
V_{IL}	Low–level input voltage (CMOS input)	$V_{REF} = DV_{DD}$			$0.3\ V_{DD}$	V
		$0.55\ V \le V_{REF} \le 0.9\ V$			$V_{REF} – 0.2$	
V_{OH}	High-level digital output voltage (open-drain output)	V_{DD} = 3 V I_{OH} = 20 µA	2.4			V
V_{OL}	Low-level digital output voltage (open-drain output)	VDD = 3.6 V I_{OL} = 4 mA			0.4	V
I_{IH}	High-level input current	V_I = 3.6 V			±25	µA
I_{IL}	Low-level input current	V_I = 0			±25	µA
$V_{(H)}$	DVI single-ended high-level output voltage	AV_{DD} = 3.3 V ±5% $r_{(T)}$‡ = 50 Ω ±10% $r_{(TFADJ)}$ = 510 Ω ±1%	$AV_{DD} – 0.01$		$AV_{DD} + 0.01$	V
$V_{(L)}$	DVI single-ended low-level output voltage		$AV_{DD} – 0.6$		$AV_{DD} – 0.4$	V
$V_{(SWING)}$	DVI single-ended output swing voltage		400		600	$mV_{P–P}$
$V_{(OFF)}$	DVI single-ended standby/off output voltage		$AV_{DD} – 0.01$		$AV_{DD} + 0.01$	V
$I_{(PD)}$	Power-down current (see Note 3)			200	500	µA
$I_{(IDD)}$	Normal power supply current	Worst case pattern§		200	250	mA

‡ $r_{(T)}$ is the single-ended termination resistance at the receiver end of the DVI link.
§ Black and white checkerboard pattern, each checker is one pixel wide.
NOTE 3: Assumes all inputs to the transmitter are not toggling.

ac specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(IDCK)}$	IDCK frequency		25		165	MHz
$t_{(pixel)}$	Pixel time period (see Note 4)		6.06		40	ns
$t_{(IDCK)}$	IDCK duty cycle		30%		70%	
$t_{(ijit)}$	IDCK clock jitter tolerance			2		ns
t_r	DVI output rise time (20–80%) (see Note 5)	$f_{(IDCK)}$ = 165 MHz	75		240	ps
t_f	DVI output fall time (20–80%) (see Note 5)		75		240	
$t_{sk(D)}$	DVI output intra-pair + to – differential skew (see Note 6)			50		
$t_{sk(CC)}$	DVI output inter-pair or channel-to-channel skew (see Note 6)				1.2	ns
t_{ojit}	Output clock jitter, maximum (see Note 7)				150	ps
$t_{su(IDF)}$	Data, DE, VSYNC, HSYNC setup time to IDCK+ falling edge	Single edge (BSEL = 1, DSEL = 0, DKEN = 0, EDGE = 0)	1.2			ns
$t_{h(IDF)}$	Data, DE, VSYNC, HSYNC hold time to IDCK+ falling edge		1.3			
$t_{su(IDR)}$	Data, DE, VSYNC, HSYNC setup time to IDCK+ rising edge	Single edge (BSEL = 1, DSEL = 0, DKEN = 0, EDGE = 1)	1.2			ns
$t_{h(IDR)}$	Data, DE, VSYNC, HSYNC hold time to IDCK+ rising edge		1.3			
$t_{su(ID)}$	Data, DE, VSYNC, HSYNC setup time to IDCK+ falling/rising edge	Dual edge (BSEL = 0, DSEL = 1, DKEN = 0)	0.9			ns
$t_{h(ID)}$	Data, DE, VSYNC, HSYNC hold time to IDCK+ falling/rising edge		1			
$t_{(STEP)}$	De-skew trim increment	DKEN = 1		350		ps

NOTES: 4. $t_{(pixel)}$ is the pixel time defined as the period of the TXC output clock. The period of IDCK is equal to $t_{(pixel)}$.
5. Rise and fall times are measured as the time between 20% and 80% of signal amplitude.
6. Measured differentially at the 50% crossing point using the IDCK+ input clock as a trigger.
7. Relative to input clock (IDCK).

timing diagrams

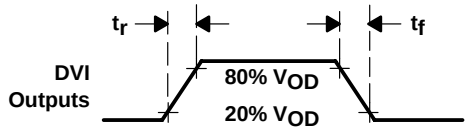


Figure 1. Rise and Fall Time for DVI Outputs

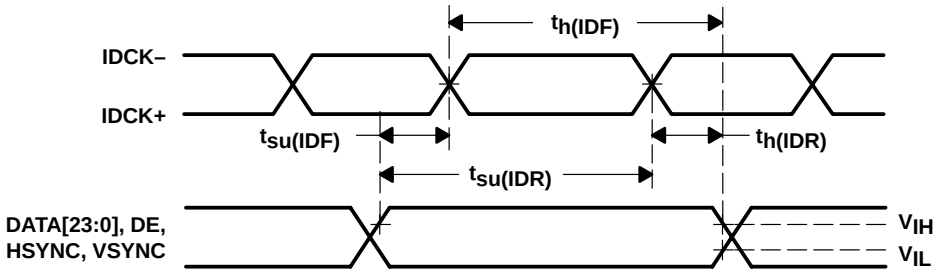


Figure 2. Control and Single-Edge-Data Setup/Hold Time to IDCK±

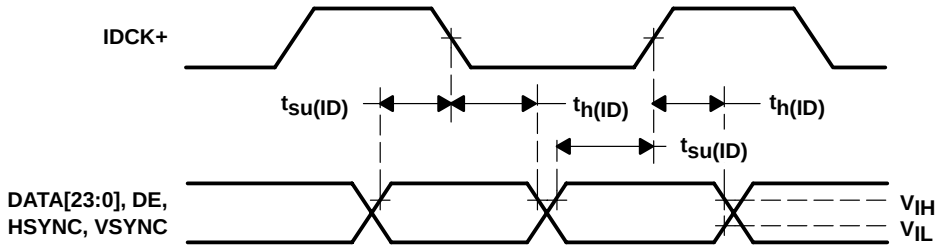


Figure 3. Dual-Edge Data Setup/Hold Times to IDCK+

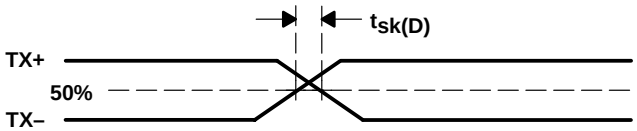


Figure 4. Analog Output Intra-Pair ± Differential Skew

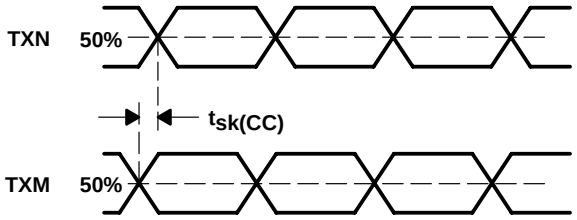


Figure 5. Analog Output Channel-to-Channel Skew

functional description

The TFP510 is a DVI-compliant digital transmitter that is used in digital host monitor systems to T.M.D.S. encode and serialize RGB pixel data streams. TFP510 supports resolutions from VGA to UXGA and can be controlled in two ways: 1) configuration and state pins or 2) the programmable I^2C serial interface (see the *terminal functions* section).

The host in a digital display system, usually a PC or consumer electronics device, contains a DVI-compatible transmitter such as the TI TFP510 that receives 24-bit pixel data along with appropriate control signals. The TFP510 encodes the signals into a high speed, low voltage, differential serial bit stream optimized for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor, requires a DVI compatible receiver like the TI TFP501 to decode the serial bit stream back to the same 24-bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the flat panel drive circuitry to produce an image on the display. Since the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred (see the *T.M.D.S. pixel data and control signal encoding, pixel data and control signal encoding, universal graphics contoller interface voltage signal levels,* and *unversal graphics controller interface clock inputs* sections).

The TFP510 integrates a high-speed digital interface, an HDCP cipher, a T.M.D.S. encoder, and three differential T.M.D.S. drivers. Data is driven to the TFP510 encoder across 12 or 24 data lines, along with differential clock pair and sync signals. The flexibility of the TFP510 allows for multiple clock and data formats that enhance system performance.

The TFP510 also has enhanced PLL noise immunity, an enhancement accomplished with on-chip regulators and bypass capacitors.

The TFP510 is versatile and highly programmable to provide maximum flexibility for the user. An I^2C host interface is provided to allow enhanced configurations in addition to power-on default settings programmed by pin-strapping resistors.

The TFP510 offers monitor detection through receiver detection, or hot-plug detection when I^2C is enabled. The monitor detection feature allows the user enhanced flexibility when attaching to digital displays or receivers (see the *terminal functions, hot-plug/unplug,* and *register descriptions* sections).

The TFP510 has a data de-skew feature allowing the users to *de-skew* the input data with respect to the IDCK± (see the *data de-skew feature* section).

The TFP510 incorporates high-bandwidth digital content protection (HDCP). This provides secure data transmission for high-definition video (see the *HDCP overview* section).

T.M.D.S. pixel data and control signal encoding

For T.M.D.S., only one of two possible T.M.D.S. characters for a given pixel is transmitted at a given time. The transmitter keeps a running count of the number of ones and zeros previously sent and transmits the character that minimizes the number of transitions and approximate a dc balance of the transmission line. Three T.M.D.S. channels are used to transmit RGB pixel data during the active video interval (DE = high). These same three channels are also used to transmit HSYNC, VSYNC, and three control signals, CTL[3:1], during the inactive display or blanking interval (DE = low). The following table maps the transmitted output data to the appropriate T.M.D.S. output channel in a DVI-compliant system.

INPUT PINS (VALID FOR DE = high)	**T.M.D.S. OUTPUT CHANNEL**	**TRANSMITTED PIXEL DATA ACTIVE DISPLAY (DE = high)**
DATA[23:16]	Channel 2 (TX2 ±)	Red[7:0]
DATA[15:8]	Channel 1 (TX1 ±)	Green[7:0]
DATA[7:0]	Channel 0 (TX0 ±)	Blue[7:0]
INPUT PINS (VALID FOR DE = low)	**T.M.D.S. OUTPUT CHANNEL**	**TRANSMITTED CONTROL DATA BLANKING INTERVAL (DE = low)**
CTL3, CTL2 (see Note 8)	Channel 2 (TX2 ±)	CTL[3:2]
CTL1 (see Note 8)	Channel 1 (TX1 ±)	CTL[1]
HSYNC, VSYNC	Channel 0 (TX0 ±)	HSYNC, VSYNC

NOTE 8: The TFP510 encodes and transfers the CTL[3:1] inputs during the vertical blanking interval. The TFP510 internally generates CTL3 for HDCP operation and the CTL[2:1] inputs are reserved for future use. When DE = high, the CTL and SYNC pins must be held constant.

universal graphics controller interface voltage signal levels

The universal graphics controller interface can operate in the following two distinct voltage modes:

- The high-swing mode where standard 3.3-V CMOS signaling levels are used
- The low-swing mode where adjustable 1.1-V to 1.8-V signaling levels are used

To select the high-swing mode, the V_{REF} input pin must be tied to the 3.3-V power supply.

To select the low-swing mode, the V_{REF} input must be = 0.55 to 0.9 V.

In the low-swing mode, V_{REF} is used to set the midpoint of the adjustable signaling levels. The allowable range of values for V_{REF} is from 0.55 V to 0.9 V. The typical approach is to provide V_{REF} to the chip using a simple voltage-divider circuit. The minimum allowable input signal swing in the low-swing mode is $V_{REF} \pm 0.2$ V. In low-swing mode, the V_{REF} input is common to all differential input receivers.

universal graphics controller interface clock inputs

The universal graphics controller interface of the TFP510 supports both single-ended and fully differential clock input modes. In the differential clock input mode, the universal graphics controller interface uses the crossover point between the IDCK+ and IDCK– signals as the timing reference for latching incoming data (DATA[23:0], DE, HSYNC, and VSYNC). Differential clock inputs provide greater common-mode noise rejection. The differential clock input mode is only available in the low-swing mode. In the single-ended clock input mode, the IDCK+ input (pin 57) should be connected to the single-ended clock source and the IDCK– input (pin 56) should be tied to GND.

The universal graphics controller interface of the TFP510 provides selectable 12-bit, dual-edge and 24-bit, single-edge input clocking modes. In the 12-bit dual-edge mode, the 12-bit data is latched on each edge of the input clock. In the 24-bit single-edge mode, the 24-bit data is latched on the rising edge of the input clock when EDGE = 1 and the falling edge of the input clock when EDGE = 0.

DKEN and DK[3:1] allow the user to compensate the skew between IDCK± and the pixel data and control signals. See the description of the CTL_3_MODE register for details.

universal graphics controller interface modes

Table 1 is a tabular representation of the different modes for the universal graphics controller interface. The 12-bit mode is selected when BSEL = 0 and the 24-bit mode when BSEL = 1. The 12-bit mode uses dual-edge clocking and the 24-bit mode uses single-edge clocking. The EDGE input is used to control the latching edge in 24-bit mode, or the primary latching edge in 12-bit mode. When EDGE = 1, the data input is latched on the rising edge of the input clock; and when EDGE = 0, the data input is latched on the falling edge of the input clock. A fully differential input clock is available only in the low-swing mode. Single-ended clocking is not recommended in the low-swing mode as this decreases common-mode noise rejection.

Note that BSEL, DSEL, and EDGE are determined by register CTL_1_MODE when I^2C is enabled (ISEL = 1) and by input pins when I^2C is disabled (ISEL = 0).

Table 1. Universal Graphics Controller Interface Options (Tabular Representation)

V_{REF}	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK EDGE	CLOCK MODE
0.55 V – 0.9 V	0	0	0	12-bit	Dual-edge	Falling	Differential (see Notes 9 and 10)
0.55 V – 0.9 V	0	0	1	12-bit	Dual-edge	Falling	Single-ended
0.55 V – 0.9V	0	1	0	12-bit	Dual-edge	Rising	Differential (see Notes 9 and 10)
0.55 V – 0.9 V	0	1	1	12-bit	Dual-edge	Rising	Single-ended
0.55 V – 0.9 V	1	0	0	24-bit	Single-edge	Falling	Single-ended
0.55 V – 0.9 V	1	0	1	24-bit	Single-edge	Falling	Differential (see Notes 9 and 11)
0.55 V – 0.9 V	1	1	0	24-bit	Single-edge	Rising	Single-ended
0.55 V – 0.9 V	1	1	1	24-bit	Single-edge	Rising	Differential (see Notes 9 and 11)
DV_{DD}	0	0	X	12-bit	Dual-edge	Falling	Single-ended (see Note 12)
DV_{DD}	0	1	X	12-bit	Dual-edge	Rising	Single-ended (see Note 12)
DV_{DD}	1	0	X	24-bit	Single-edge	Falling	Single-ended (see Note 12)
DV_{DD}	1	1	X	24-bit	Single-edge	Rising	Single-ended (see Note 12)

NOTES: 9. The differential clock input mode is only available in the low signal swing mode (i.e., $V_{REF} \leq 0.9$ V).
10. The TFP510 does not support a 12-bit dual-clock, single-edge input clocking mode.
11. The TFP510 does not support a 24-bit single-clock, dual-edge input clocking mode.
12. In the high-swing mode ($V_{REF} = DV_{DD}$), DSEL is a don't care; therefore, the device is always in the single-ended latch mode.

universal graphics controller interface modes (continued)

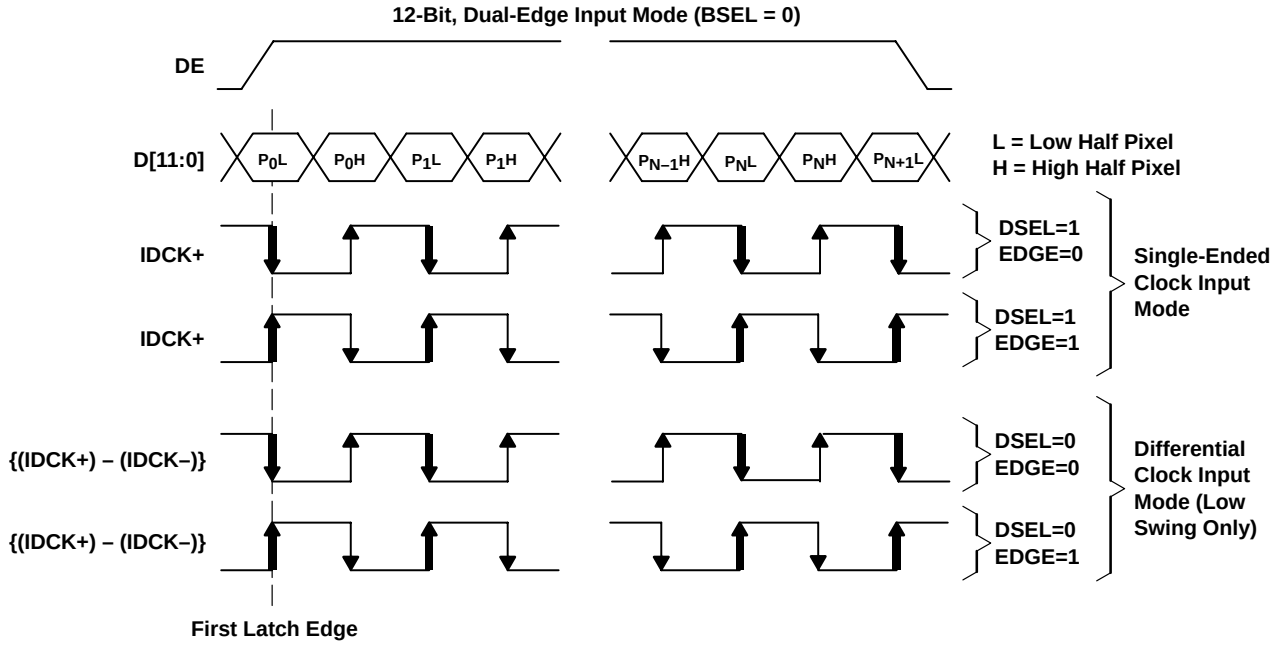


Figure 6. Universal Graphics Controller Interface Options for 12-Bit Mode (Graphical Representation)

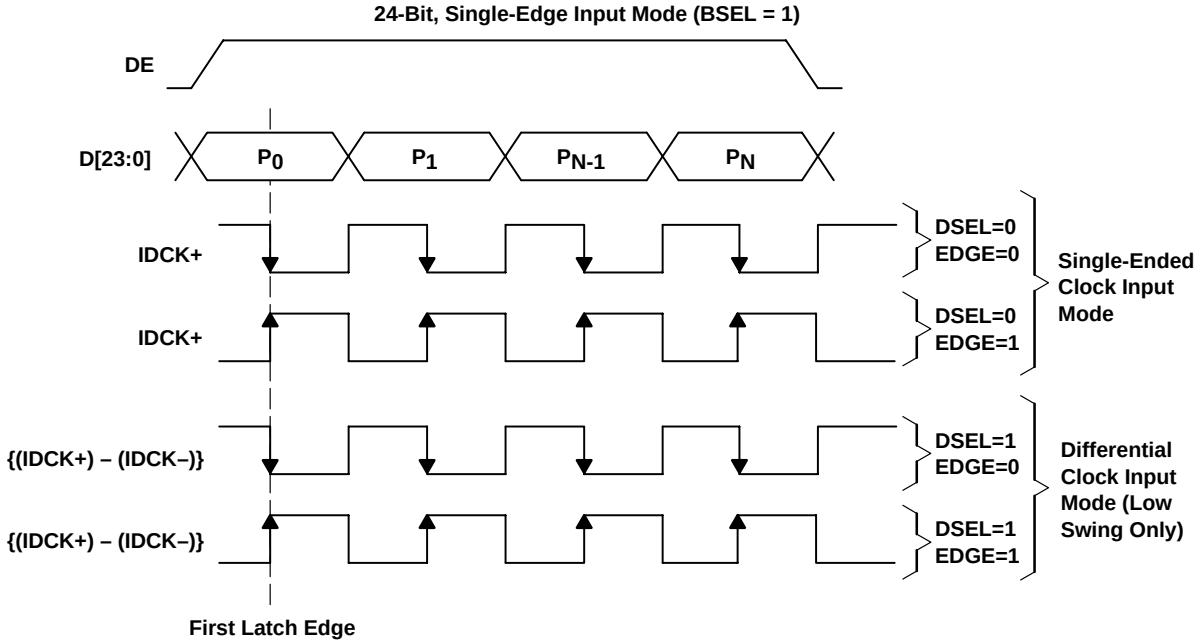


Figure 7. Universal Graphics Controller Interface Options for 24-Bit Mode (Graphical Representation)

12-bit mode data mapping

PIN NAME	P0		P1		P2	
	P0L	P0H	P1L	P1H	P2L	P2H
	LOW	HIGH	LOW	HIGH	LOW	HIGH
D11	G0[3]	R0[7]	G1[3]	R1[7]	G2[3]	R2[7]
D10	G0[2]	R0[6]	G1[2]	R1[6]	G2[2]	R2[6]
D9	G0[1]	R0[5]	G1[1]	R1[5]	G2[1]	R2[5]
D8	G0[0]	R0[4]	G1[0]	R1[4]	G2[0]	R2[4]
D7	B0[7]	R0[3]	B1[7]	R1[3]	B2[7]	R2[3]
D6	B0[6]	R0[2]	B1[6]	R1[2]	B2[6]	R2[2]
D5	B0[5]	R0[1]	B1[5]	R1[1]	B2[5]	R2[1]
D4	B0[4]	R0[0]	B1[4]	R1[0]	B2[4]	R2[0]
D3	B0[3]	G0[7]	B1[3]	G1[7]	B2[3]	G2[7]
D2	B0[2]	G0[6]	B1[2]	G1[6]	B2[2]	G2[6]
D1	B0[1]	G0[5]	B1[1]	G1[5]	B2[1]	G2[5]
D0	B0[0]	G0[4]	B1[0]	G1[4]	B2[0]	G2[4]

24-bit mode data mapping

PIN NAME	P0	P1	P2	PIN NAME	P0	P1	P2
D23	R0[7]	R1[7]	R2[7]	D11	G0[3]	G1[3]	G2[3]
D22	R0[6]	R1[6]	R2[6]	D10	G0[2]	G1[2]	G2[2]
D21	R0[5]	R1[5]	R2[5]	D9	G0[1]	G1[1]	G2[1]
D20	R0[4]	R1[4]	R2[4]	D8	G0[0]	G1[0]	G2[0]
D19	R0[3]	R1[3]	R2[3]	D7	B0[7]	B1[7]	B2[7]
D18	R0[2]	R1[2]	R2[2]	D6	B0[6]	B1[6]	B2[6]
D17	R0[1]	R1[1]	R2[1]	D5	B0[5]	B1[5]	B2[5]
D16	R0[0]	R1[0]	R2[0]	D4	B0[4]	B1[4]	B2[4]
D15	G0[7]	G1[7]	G2[7]	D3	B0[3]	B1[3]	B2[3]
D14	G0[6]	G1[6]	G2[6]	D2	B0[2]	B1[2]	B2[2]
D13	G0[5]	G1[5]	G2[5]	D1	B0[1]	B1[1]	B2[1]
D12	G0[4]	G1[4]	G2[4]	D0	B0[0]	B1[0]	B2[0]

data de-skew feature

The de-skew feature allows adjustment of the input setup/hold time. Specifically, the input data DATA[23:0] can be latched slightly before or after the latching edge of the clock IDCK± depending on the amount of de-skew desired. When de-skew enable (DKEN) is enabled, the amount of de-skew is programmable by setting the three bits DK[3:1]. When disabled, a default de-skew setting is used. To allow maximum flexibility and ease of use, DKEN and DK[3:1] are accessed directly through configuration pins when I^2C is disabled, or through registers of the same name when I^2C is enabled. When using I^2C mode, the DKEN pin should be tied to ground to avoid a floating input.

The input setup/hold time (see Figure 8) can be varied with respect to the input clock by an amount t_{CD} given by the formula:

$$t_{(CD)} = (DK[3:1] - 4) \times t_{(STEP)}$$

Where:

$t_{(STEP)}$ is the adjustment increment amount
DK[3:1] is a number from 0 to 7 represented as a 3-bit binary number
$t_{(CD)}$ is the cumulative de-skew amount

(DK[3:1]-4) is simply a multiplier in the range {-4,-3,-2,-1, 0, 1, 2, 3} for $t_{(STEP)}$. Therefore, data can be latched in increments from 4 times the value of $t_{(STEP)}$ before the latching edge of the clock to 3 times the value of $t_{(STEP)}$ after the latching edge. Note that the input clock is not changed, only the time when data is latched with respect to the clock.

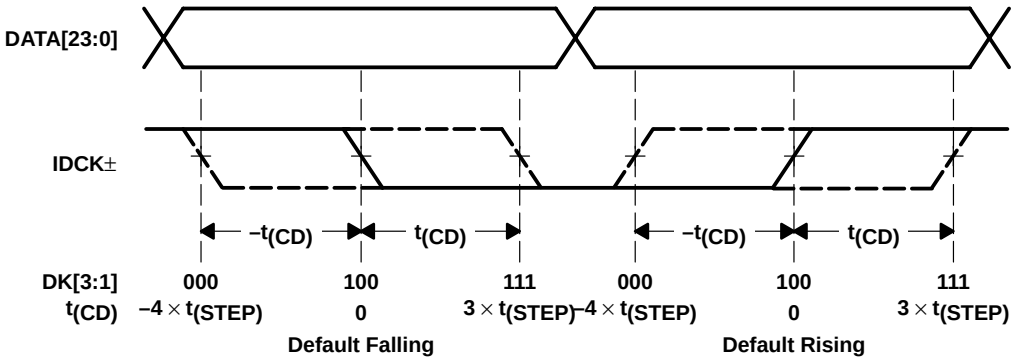


Figure 8. De-Skew Function Timing Diagram

hot plug/unplug (auto connect/disconnect detection)

The TFP510 supports hot plug/unplug (auto connect/disconnect detection) for the DVI link. The receiver sense input (RSEN) bit indicates if a DVI receiver is connected to TXC+ and TXC–. The HTPLG bit reflects the current state of the HTPLG pin connected to the monitor via the DVI connector. When I^2C is disabled (ISEL = 0), the RSEN value is available on the MSEN pin. When I^2C is enabled, the connection status of the DVI link and HTPLG sense pins is provided by the CTL_2_MODE register. The MSEL bits of the CTL_2_MODE register can be used to program the MSEN to output the HTPLG value, the RSEN value, an interrupt, or be disabled.

The source of the interrupt event is selected by TSEL in the CTL_2_MODE register. An interrupt is generated by a change in status of the selected signal. The interrupt status is indicated in the MDI bit of CTL_2_MODE and can be output on the MSEN pin. The interrupt continues to be asserted until a 1 is written to the MDI bit, resetting the bit back to 1. Writing 0 to the MDI bit has no effect.

device configuration and I²C RESET description

The TFP510 device configuration can be programmed by several different methods to allow maximum flexibility for the user's application. Device configuration is controlled depending on the state of the ISEL/$\overline{\text{RST}}$ pin, configuration pins (BSEL, DSEL, EDGE, V_{REF}) and state pin ($\overline{\text{PD}}$). I²C bus select and I²C RESET (active low) are shared functions on the ISEL/$\overline{\text{RST}}$ pin, which operates asynchronously.

Holding ISEL/$\overline{\text{RST}}$ low causes the device configuration to be set by the configuration pins (BSEL, DSEL, EDGE, and V_{REF}) and state pin ($\overline{\text{PD}}$). The I²C bus is disabled.

Holding ISEL/$\overline{\text{RST}}$ high causes the chip configuration to be set based on the configuration bits (BSEL, DSEL, EDGE) and state bits ($\overline{\text{PD}}$, DKEN) in the I²C registers. The I²C bus is enabled.

Momentarily bringing ISEL/$\overline{\text{RST}}$ low and then back high while the device is operating in normal or power-down mode resets the I²C registers to their default values, and the device configuration is changed to the default power-up state with I²C enabled. After power up, the device must be reset. It is suggested that a low going pulse with 100 ns minimum width be applied to this pin after all the power supplies are fully functional.

DE generator

The TFP510 contains a DE generator that can be used to generate an internal DE signal when the original data source does not provide one. There are several I²C programmable values that control the DE generator (see Figure 9). DE_GEN in the DE_CTL register enables this function. When enabled, the DE pin is ignored.

DE_TOP and DE_LIN are line counts used to control the number of lines after VSYNC goes active that DE is enabled, and the total number of lines that DE remains active, respectively. The polarity of VSYNC must be set by VS_POL in the DE_CTL register.

DE_DLY and DE_CNT are pixel counts used to control the number of pixels after HSYNC goes active that DE is enabled, and the total number of pixels that DE remains active, respectively. The polarity of HSYNC must be set by HS_POL in the DE_CTL register.

The TFP510 also counts the total number of HSYNC pulses between VSYNC pulses, and the total number of pixels between HSYNC pulses. These values, the total vertical and horizontal resolutions, are available in V_RES and H_RES, respectively. These values are available at all times, whether or not the DE generator is enabled.

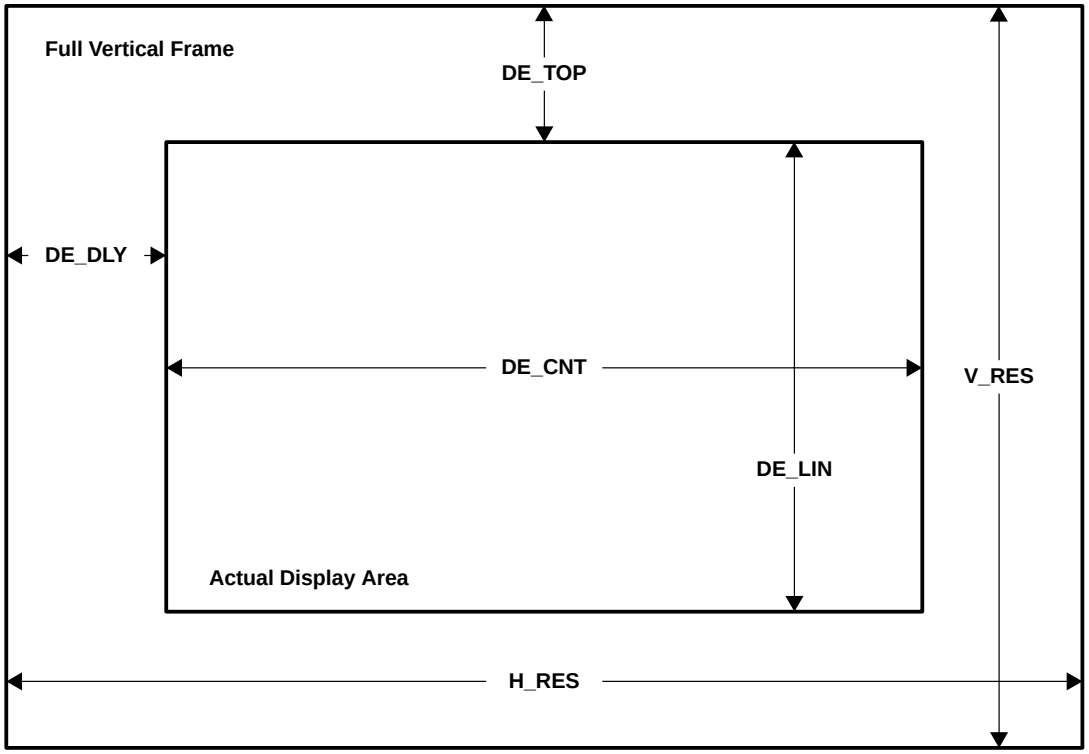


Figure 9. DE Generator Register Functions

HDCP overview

The TFP510 provides high-bandwidth digital content protection (HDCP) by encrypting the transmitted active pixel data stream sent to an HDCP receiver (like the TFP501). The HDCP algorithm is fully incorporated, and only requires an external source of HDCP keys and a software driver to implement an HDCP host.

The HDCP technology requires adherence to the HDCP license's compliance (available from www.digital-cp.com) and robustness rules. These rules require that HDCP implementation both protect the confidentiality of keys and other values from compromise as well as deliver the desired protection for high-value video content. The TFP510 provides a complete, easily implemented solution to these requirements.

Details of TFP510 HDCP operation are available in a separate document.

register map

The TFP510 is a standard I^2C slave device. All the registers can be written and read through the I^2C interface (unless otherwise specified). The TFP510 slave machine supports only byte read and write cycles. Page mode is not supported. The 8-bit binary address of the I^2C machine is 0111 000X, where X = 0 for write and X = 1 for read on the TFP510.

REGISTER	RW	SUB-ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VEN_ID	R	00	VEN_ID[7:0]							
	R	01	VEN_ID[15:8]							
DEV_ID	R	02	DEV_ID[7:0]							
	R	03	DEV_ID[15:8]							
REV_ID	R	04	REV_ID[7:0]							
RESERVED	R	05-07	Reserved							
CTL_1_MODE	RW	08	RSVD	TDIS	VEN	HEN	DSEL	BSEL	EDGE	$\overline{PD}$
CTL_2_MODE	RW	09	VLOW	MSEL			TSEL	RSEN	HTPLG	MDI
CTL_3_MODE	RW	0A	DK			DKEN	RSVD	CTL		RSVD
CFG	R	0B	CFG							
RESERVED	RW	0C-31	Reserved							
DE_DLY	RW	32	DE_DLY[7:0]							
DE_CTL	RW	33	RSVD	DE_GEN	VS_POL	HS_POL	RSVD			DE_DLY[8]
DE_TOP	RW	34	RSVD	DE_DLY[6:0]						
RESERVED	RW	35	Reserved							
DE_CNT	RW	36	DE_CNT[7:0]							
	RW	37	Reserved					DE_CNT[10:8]		
DE_LIN	RW	38	DE_LIN[7:0]							
	RW	39	Reserved					DE_LIN[10:8]		
H_RES	R	3A	H_RES[7:0]							
	R	3B	Reserved					H_RES[10:8]		
V_RES	R	3C	V_RES[7:0]							
	R	3D	Reserved					V_RES[10:8]		
RESERVED	R	3E–FF								

register descriptions

VEN_ID **Sub-Address = 01–00** **Read Only** **Default = 0x014C**

7	6	5	4	3	2	1	0
VEN_ID[7:0]							
VEN_ID[15:8]							

These read-only registers contain the 16-bit Texas Instruments vendor ID. VEN_ID is hardwired to 0x014C.

DEV_ID **Sub-Address = 03–02** **Read Only** **Default = 0x0510**

7	6	5	4	3	2	1	0
DEV_ID[7:0]							
DEV_ID[15:8]							

These read-only registers contain the 16-bit device ID. DEV_ID is hardwired to 0x0510 for the TFP510.

register descriptions (continued)

REV_ID	Sub-Address = 04			Read Only			Default = 0x00
7	6	5	4	3	2	1	0
REV_ID[7:0]							

This read-only register contains the revision ID.

RESERVED	Sub-Address = 07–05			Read Only			Default = 0x641400
7	6	5	4	3	2	1	0
RESERVED							

CTL_1_MODE	Sub-Address = 08			Read/Write			Default = 0xBE
7	6	5	4	3	2	1	0
RSVD	TDIS	VEN	HEN	DSEL	BSEL	EDGE	$\overline{PD}$

$\overline{PD}$: This read/write register contains the power-down mode.

0: Power down (default after RESET)
1: Normal operation

EDGE: This read/write register contains the edge select mode.

0: Input data latches to the falling edge of IDCK+
1: Input data latches to the rising edge of IDCK+

BSEL: This read/write register contains the input bus select mode.

0: 12-bit operation with dual-edge clock
1: 24-bit operation with single-edge clock

DSEL: This read/write register is used in combination with BSEL and VREF to select the single-ended or differential input clock mode. In the high-swing mode, DSEL is a don't care because IDCK is always single-ended.

HEN: This read/write register contains the horizontal sync enable mode.

0: HSYNC input is transmitted as a fixed low
1: HSYNC input is transmitted in its original state

VEN: This read/write register contains the vertical sync enable mode.

0: VSYNC input is transmitted as a fixed low
1: VSYNC input is transmitted in its original state

TDIS: This read/write register contains the T.M.D.S. disable mode.

0: T.M.D.S. circuitry enable state is determined by $\overline{PD}$
1: T.M.D.S. circuitry is disabled

register descriptions (continued)

CTL_2_MODE	Sub-Address = 09			Read/Write			Default = 0x00
7	6	5	4	3	2	1	0
VLOW	MSEL[3:1]			TSEL	RSEN	HTPLG	MDI

MDI: This read/write register contains the monitor detect interrupt mode.

0: Detected logic level change in detection signal (to clear, write 1 to this bit)
1: Logic level remains the same

HTPLG: This read-only register contains the hot plug detection input logic state.

0: Low level detected on the EDGE/HTPLG pin (pin 9)
1: High level detected on the EDGE/HTPLG pin (pin 9)

RSEN: This read only register contains the receiver sense input logic state, which is valid only for dc-coupled systems.

0: A powered-on receiver is not detected
1: A powered-on receiver is detected (i.e., connected to the DVI transmitter outputs)

TSEL: This read/write register contains the interrupt generation source select.

0: Interrupt bit (MDI) is generated by monitoring RSEN
1: Interrupt bit (MDI) is generated by monitoring HTPLG

MSEL[3:1]: This read/write register contains the source select of the monitor sense output pin.

000: Disabled. MSEN output high
001: Outputs the MDI bit (interrupt)
010: Outputs the RSEN bit (receiver detect)
011: Outputs the HTPLG bit (hot plug detect)

VLOW: This read-only register indicates the V_{REF} input level.

0: This bit is a logic level 0 if the V_{REF} analog input selects high-swing inputs.
1: This bit is a logic level 1 if the V_{REF} analog input selects low-swing inputs.

CTL_3_MODE	Sub-Address = 0A			Read/Write			Default = 0x80
7	6	5	4	3	2	1	0
DK[3:1]			DKEN	RSVD	CTL[2:1]		RSVD

CTL[2:1]: This read/write register contains the values of the two CTL[2:1] bits that are output on the DVI port during the blanking interval. CTL[3] is not available on the TFP510 because it is inetrnally generated by the HDCP circuitry.

DKEN: This read/write register controls the data de-skew enable.

0: Data de-skew is disabled; the values in DK[3:1] are not used.
1: Data de-skew is enabled; the de-skew setting is controlled through DK[3:1].

DK[3:1]: This read/write register contains the de-skew setting, each increment adjusts the skew by $t_{(STEP)}$.

000: Step 1 (minimum setup/maximum hold)
001: Step 2
010: Step 3
011: Step 4
100: Step 5 (default)
101: Step 6
110: Step 7
111: Step 8 (maximum setup/minimum hold)

register descriptions (continued)

CFG	Sub-Address = 0B					Read Only	
7	6	5	4	3	2	1	0
CFG[7:0] (D[23:16])							

This read-only register contains the state of the inputs D[23:16]. These pins can be used to provide the user with selectable configuration data through the I^2C bus.

RESERVED	Sub-Address = 0E–0C			Read/Write		Default = 0x97D0A9	
7	6	5	4	3	2	1	0
RESERVED							
RESERVED							
RESERVED							

These read/write registers have no effect on TFP510 operation.

DE_DLY	Sub-Address = 32			Read/Write		Default = 0x00	
7	6	5	4	3	2	1	0
DE_DLY[7:0]							

This read/write register defines the number of pixels after HSYNC goes active that DE is generated, when the DE generator is enabled.

DE_CTL	Sub-Address = 33			Read/Write		Default = 0x00	
7	6	5	4	3	2	1	0
Reserved	DE_GEN	VS_POL	HS_POL	Reserved			DE_DLY[8]

DE_DLY[8]: This read/write register contains the top bit of DE_DLY.

HS_POL: This read/write register sets the HSYNC polarity.

0: HSYNC is considered active low.
1: HSYNC is considered active high.
Pixel counts are reset on the HSYNC active edge.

VS_POL: This read/write register sets the VSYNC polarity.

0: VSYNC is considered active low.
1: VSYNC is considered active high.
Line counts are reset on the VSYNC active edge.

DE_GEN: This read/write register enables the internal DE generator.

0: DE generator is disabled. Signal required on DE pin
1: DE generator is enabled. DE pin is ignored.

DE_TOP	Sub-Address = 34			Read/Write		Default = 0x00	
7	6	5	4	3	2	1	0
DE_TOP[7:0]							

This read/write register defines the number of pixels after VSYNC goes active that DE is generated, when the DE generator is enabled.

register descriptions (continued)

DE_CNT **Sub-Address = 37–36** **Read/Write** **Default = 0x0000**

7	6	5	4	3	2	1	0
DE_CNT[7:0]							
Reserved					DE_CNT[10:8]		

These read/write registers define the width of the active display, in pixels, when the DE generator is enabled.

DE_LIN **Sub-Address = 39–38** **Read/Write** **Default = 0x0000**

7	6	5	4	3	2	1	0
DE_LIN[7:0]							
Reserved					DE_LIN[10:8]		

These read/write registers define the height of the active display, in lines, when the DE generator is enabled.

H_RES **Sub-Address = 3B–3A** **Read Only**

7	6	5	4	3	2	1	0
H_RES[7:0]							
Reserved					H_RES[10:8]		

These read-only registers return the number of pixels between consecutive HSYNC pulses.

V_RES **Sub-Address = 3D–3C** **Read Only**

7	6	5	4	3	2	1	0
V_RES[7:0]							
Reserved					V_RES[10:8]		

These read-only registers return the number of lines between consecutive VSYNC pulses.

I²C interface

The I²C interface is used to access the internal registers. This two-pin interface consists of the SCL clock line and the SDA serial data line. The basic I²C access cycles are shown in Figures 9 and 10.

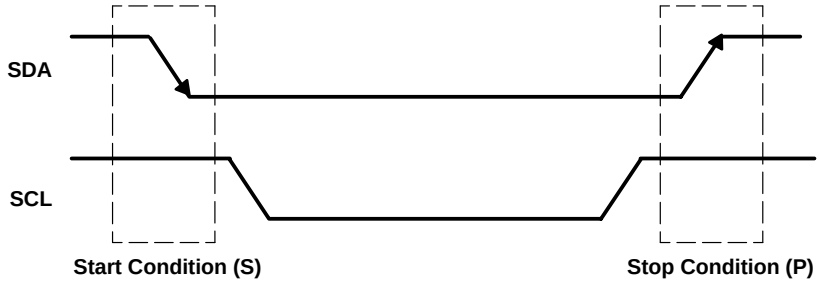


Figure 10. I²C Start and Stop Conditions

The basic access write cycle consists of the following:

1. A start condition
2. A slave address cycle
3. A sub-address cycle
4. Any number of data cycles
5. A stop condition

The basic access read cycle consists of the following:

1. A start condition
2. A slave write address cycle
3. A sub-address cycle
4. A restart condition
5. A slave read address cycle
6. Any number of data cycles
7. A stop condition

The start and stop conditions are shown in Figure 9. The high-to-low transition of SDA while SCL is high defines the start condition. The low to high transition of SDA while SCL is high defines the stop condition. Each cycle, data or address, consists of 8 bits of serial data followed by one acknowledge bit generated by the receiving device. Thus, each data/address cycle contains 9 bits as shown in Figure 10.

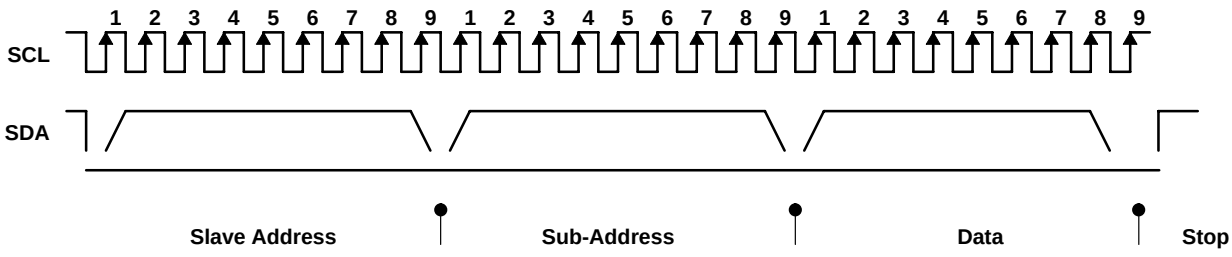


Figure 11. I²C Access Cycles

I²C interface (continued)

Following a start condition, each I²C device decodes the slave address. The TFP510 responds with an acknowledge by pulling the SDA line low during the ninth clock cycle if it decodes the address as its address. During subsequent sub-address and data cycles, the TFP510 responds with acknowledge as shown in Figure 11. The sub-address is auto-incremented after each data cycle.

The transmitting device must not drive the SDA signal during the acknowledge cycle so that the receiving device may drive the SDA signal low. The master indicates a *not acknowledge* condition (/A) by keeping the SDA signal high just before it asserts the stop condition (P). This sequence terminates a read cycle as shown in Figure 12.

In order to minimize the number of bits that must be transferred for the HDCP link integrity check, a second read format is supported. This access, shown in Figure 13, has an implicit sub-address equal to the starting location for the HDCP receiver link verification response (R'_i).

The slave address consists of 7 bits of address along with 1 bit of read/write information (i.e., read = 1 and write = 0) as shown in Figures 12 and 13. For the TFP510 the slave addresses are 0x70 for write cycles and 0x71 for read cycles.

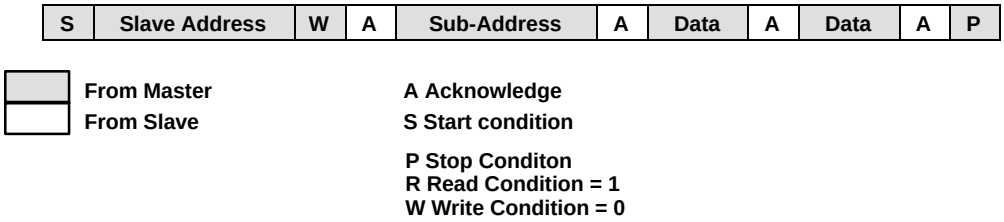


Figure 12. I²C Write Cycle

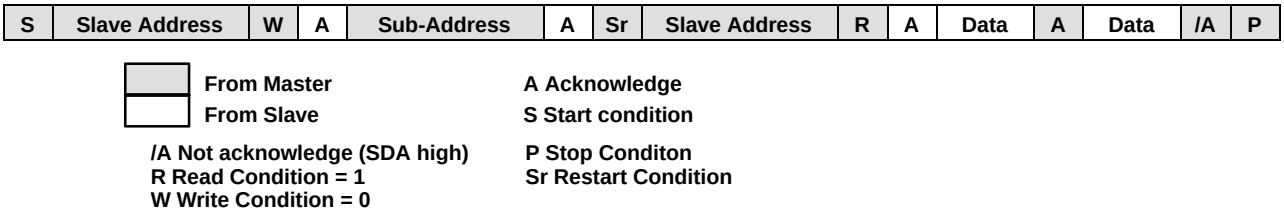


Figure 13. I²C Read Cycle

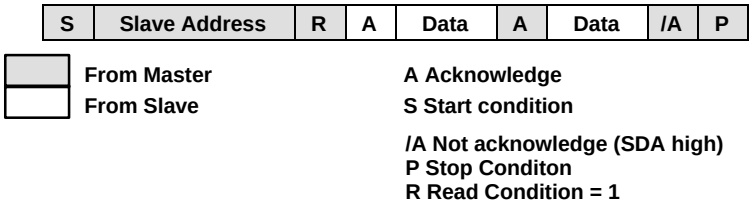


Figure 14. HDCP Port Link Integrity Message Read

TI 64-pin TQFP PowerPAD package

The TFP510 is available in TI's thermally enhanced 64-pin TQFP PowerPAD package. The PowerPAD package is a 10-mm × 10-mm × 1,0-mm TQFP outline with 0,5-mm lead-pitch. The PowerPAD package has a specially designed die mount pad that offers improved thermal capability over typical TQFP packages of the same outline. The TI 64-pin TQFP PowerPAD package offers a backside solder plane that connects directly to the die mount pad for enhanced thermal conduction. For thermal considerations, soldering the backside of the TFP510 to the application board is not required because the device power dissipation is well within the package capability when not soldered.

Soldering the backside of the device to the PCB ground plane is recommended for electrical considerations. Because the die pad is electrically connected to the chip substrate and hence to chip ground, connecting the back side of the PowerPAD package to a PCG ground plane provides a low-inductance, low-impedance connection to help improve EMI, ground bounce, and power-supply noise performance.

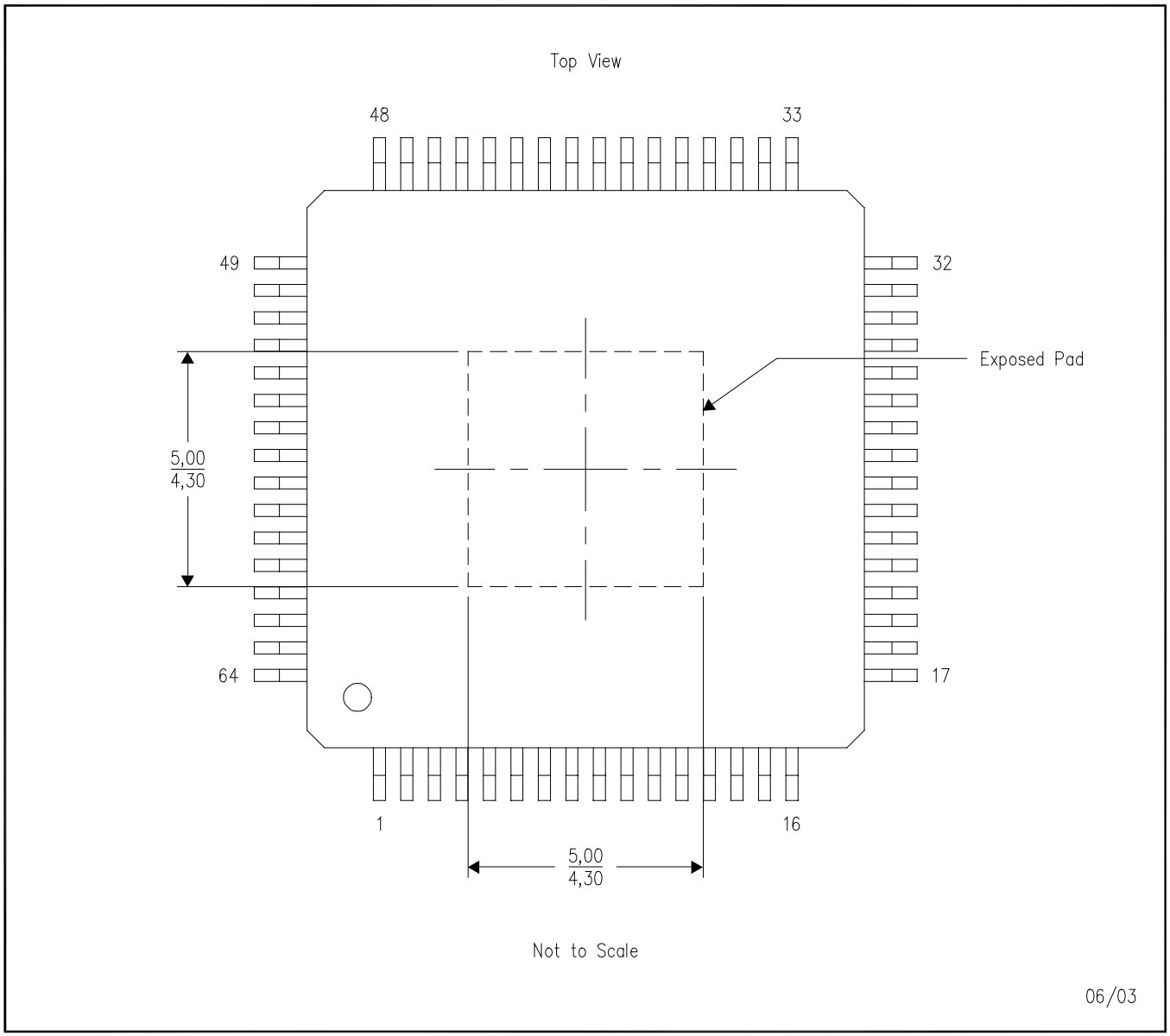
Table 2 contains the thermal properties of the TI 64-pin TQFP PowerPAD package. The 64-pin TQFP non-PowerPAD package is included only for reference.

Table 2. TI 64-Pin TQFP (10 × 10 × 1,0 mm)/0,5 mm Lead-Pitch

PARAMETER		WITHOUT PowerPAD™	PowerPAD™ NOT CONNECTED TO PCB THERMAL PLANE	PowerPAD™ CONNECTED TO PCB THERMAL PLANE (see Note 14)
$R_{\theta JA}$	Thermal resistance, junction-to-ambient (see Notes 13 and 14)	75.83°C/W	42.20°C/W	21.47°C/W
$R_{\theta JC}$	Thermal resistance, junction-to-case (see Notes 13 and 14)	7.80°/W	0.38°C/W	0.38°C/W
P_D	Power handling capabilities of package (see Notes 13, 14, and 15)	0.92 W	1.66 W	3.26 W

NOTES: 13. Specified with the bond pad on the backside of the PowerPAD package soldered to a 2-oz. Cu plate PCB thermal plane
14. Airflow is at 0 LFM (no airflow).
15. Specified at 150°C junction temperature and 80°C ambient temperature

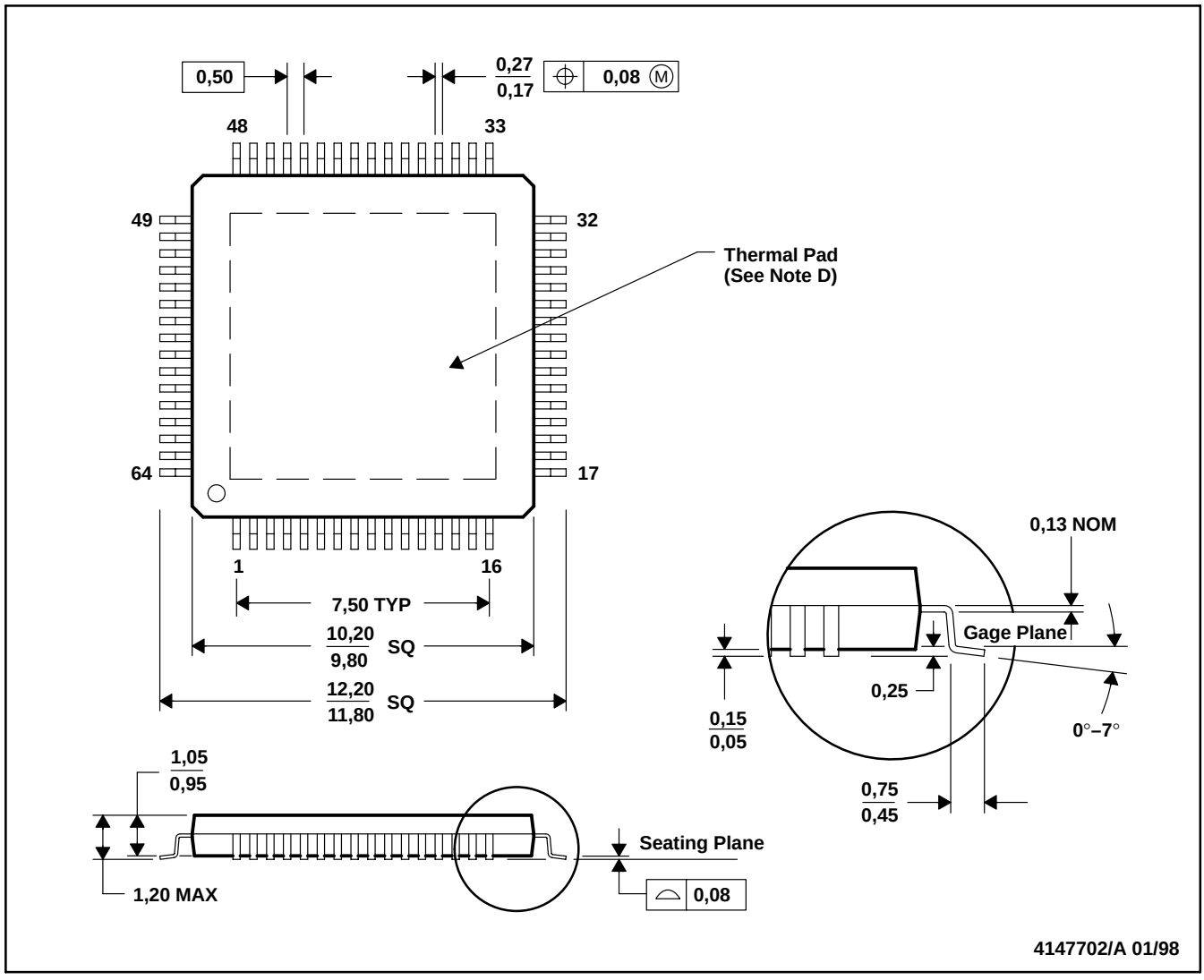
PAP (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, ***PowerPAD Thermally Enhanced Package***, Texas Instruments Literature No. SLMA002 and Application Brief, ***PowerPAD Made Easy***, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

MECHANICAL DATA

PAP (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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