

- Digital Visual Interface (DVI) Compliant¹
- Supports Resolutions From VGA to UXGA (25-MHz through 165-MHz Pixel Rates)
- Universal Graphics Controller Interface
 - 12-Bit, Dual-Edge and 24-Bit, Single-Edge Input Modes
 - Adjustable 1.1-V to 1.8-V and Standard 3.3-V CMOS Input Signal Levels
 - Fully Differential and Single-Ended Input Clocking Modes
 - Standard Intel 12-Bit Digital Video Port Compatible as on Intel™ 81x Chipsets
- Enhanced PLL Noise Immunity
 - On-Chip Regulators and Bypass Capacitors for Reducing Systems Costs
- Enhanced Jitter Performance
 - No HSYNC Jitter Anomaly
 - Negligible Data-Dependent Jitter
- Programmable Using I²C Serial Interface
- Monitor Detection Through Hot-Plug and Receiver Detection
- Single 3.3-V Supply Operation
- 64-Pin TQFP Using TI's PowerPAD™ Package
- TI's Advanced 0.18 μm EPIC-5™ CMOS Process Technology
- Pin Compatible With Si1164 and Si1168 DVI Transmitters
- High-Bandwidth Digital Content Protection (HDCP) Specifications Compliant²
- Embedded Preprogrammed HDCP Keys

description

The TFP513 is a Texas Instruments *PanelBus* flat panel display product, part of a comprehensive family of end-to-end DVI 1.0 compliant solutions, targeted at the PC and consumer electronics industry.

The TFP513 provides a universal interface to allow a glueless connection to most commonly available graphics controllers. Some of the advantages of this universal interface include selectable bus widths, adjustable signal levels, and differential and single-ended clocking. The adjustable 1.1-V to 1.8-V digital interface provides a low-EMI, high-speed bus that connects seamlessly with a 12-bit or 24-bit interface. The DVI interface supports flat panel display resolutions up to UXGA at 165 MHz in 24-bit true color pixel format.

The TFP513 combines *PanelBus* circuit innovation with TI's advanced 0.18 μm EPIC-5 CMOS process technology and TI's ultralow ground inductance PowerPAD package. The result is a compact 64-pin TQFP package providing a reliable, low-noise, high-speed, digital interface solution. The TFP513 comes with embedded preprogrammed HDCP keys, thus eliminating the need for an external storage device to store the HDCP keys and the need for the customer to purchase HDCP keys from the licensing authority. An encryption scheme ensures that the embedded HDCP keys are encrypted thus providing the highest level of key security.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Footnotes:

1. The digital visual interface (DVI) specification is an industry standard developed by the digital display working group (DDWG) for high-speed digital connection to digital displays. The TFP513 is compliant to the digital visual interface (DVI) Revision 1.0 specification. The DVI 1.0 specification has been adopted by the industry leading PC and consumer electronics manufacturers.
2. The high-bandwidth digital content protection system (HDCP) is an industry standard for protecting DVI outputs from being copied. HDCP was developed by Intel Corporation and is licensed by the Digital Content Protection, LLC. The TFP513 is compliant to the HDCP Revision 1.0 specification.

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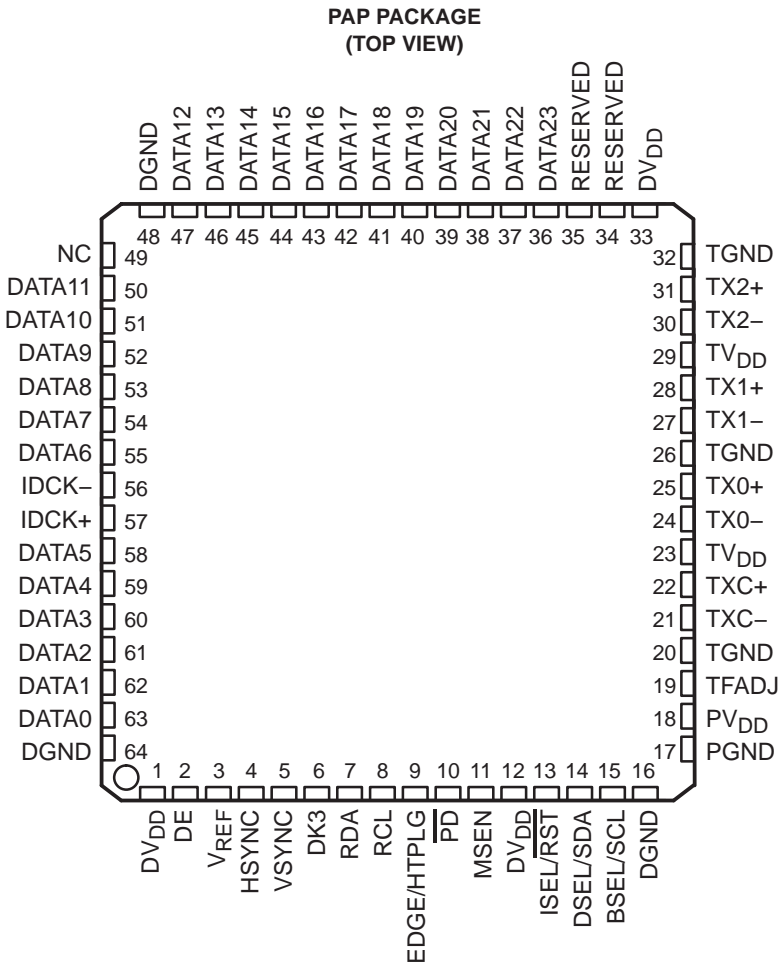
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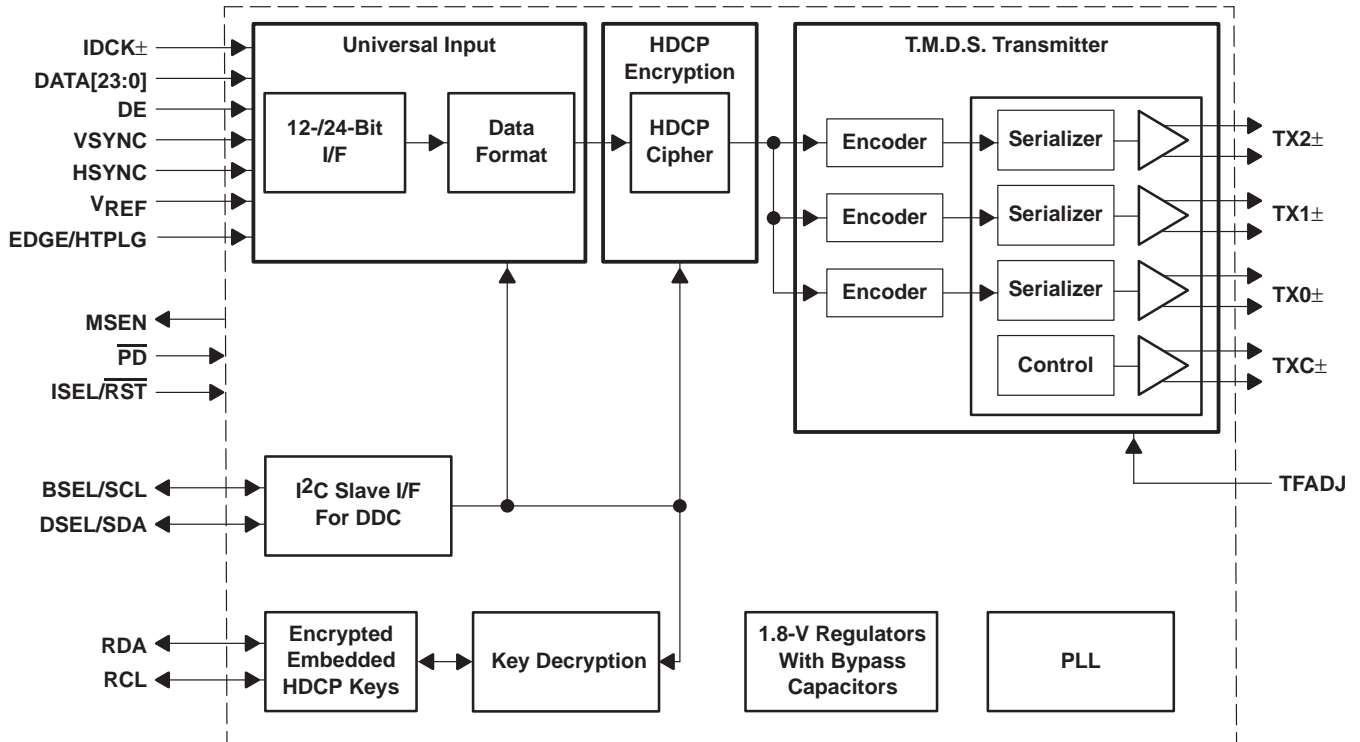


This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads must be shorted together or the device must be placed in conductive foam. In a circuit, unused inputs must always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

pin assignments



functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NUMBER		
Input Pins			
DATA[23:12]	36–47	I	<p>The upper 12 bits of the 24-bit pixel bus.</p> <p>In 24-bit, single-edge input mode (BSEL = high), this bus inputs the top half of the 24-bit pixel bus.</p> <p>In 12-bit, dual-edge input mode (BSEL = low), these bits do not input pixel data. In this mode, the state of DATA[23:16] is input to the I²C register CFG. This allows 8 bits of user configuration data to be read by the graphics controller through the I²C interface (see the I²C <i>register descriptions</i> section).</p> <p>Note: All unused data inputs must be tied to GND or V_{DD}.</p>
DATA[11:0]	50–55, 58–63	I	<p>The lower 12 bits of the 24-bit pixel bus/12-bit pixel bus input.</p> <p>In 24-bit, single-edge input mode (BSEL = high), this bus inputs the bottom half of the 24-bit pixel bus.</p> <p>In 12-bit, dual-edge input mode (BSEL = low), this bus inputs 1/2 pixel (12 bits) at every latch edge (both rising and falling) of the clock.</p>
DE	2	I	<p>Data enable. As defined in the DVI 1.0 specification, the DE signal allows the transmitter to encode pixel data or control data on any given input clock cycle. During active video (DE = high), the transmitter encodes pixel data, DATA[23:0]. During the blanking interval (DE = low), the transmitter encodes HSYNC, VSYNC, and CTL[3:1].</p>

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Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NUMBER		
Input Pins (Continued)			
DK3	6	I	This input pin is not used for the TFP513. It contains a weak pulldown resistor and may be left unconnected. If a pullup resistor is connected to V _{DD} , it must be in the range of 900 Ω to 5 kΩ.
HSYNC	4	I	Horizontal sync input
IDCK– IDCK+	56 57	I	Differential clock input. The TFP513 supports both single-ended and fully differential clock input modes. In the single-ended clock input mode, the IDCK+ input (pin 57) must be connected to the single-ended clock source and the IDCK input (pin 56) must be tied to GND. In the differential clock input mode, the TFP513 uses the crossover point between the IDCK+ and IDCK– signals as the timing reference for latching incoming data DATA[23:0], DE, HSYNC, and VSYNC. The differential clock input mode is only available in the low-signal-swing mode.
VSYNC	5	I	Vertical sync input
Configuration/Programming Pins			
BSEL/SCL	15	I/O	Input bus select / I ² C clock input. The operation of this pin depends on whether the I ² C interface is enabled or disabled. This pin is only 3.3-V tolerant. When I ² C is disabled (ISEL = low), a high level selects the 24-bit input, single-edge input mode. A low level selects the 12-bit input, dual-edge input mode. When I ² C is enabled (ISEL = high), this pin functions as the I ² C clock input (see the I ² C register descriptions section). In this configuration, this pin has an open-drain output that requires an external 5-kΩ pullup resistor connected to V _{DD} .
DSEL/SDA	14	I/O	DSEL / I ² C data. The operation of this pin depends on whether the I ² C interface is enabled or disabled. This pin is only 3.3-V tolerant. When I ² C is disabled (ISEL = low), this pin is used with BSEL and V _{REF} to select the single-ended or differential input clock mode (see the universal graphics controller interface modes section). When I ² C is enabled (ISEL = high), this pin functions as the I ² C bidirectional data line. In this configuration, this pin has an open-drain output that requires an external 5-kΩ pullup resistor connected to V _{DD} .
EDGE/HTPLG	9	I	Edge select / hot plug input. The operation of this pin depends on whether the I ² C interface is enabled or disabled. This input is 3.3-V tolerant only. When I ² C is disabled (ISEL = low), a high level selects the primary latch to occur on the rising edge of the input clock IDCK+. A low level selects the primary latch to occur on the falling edge of the input clock IDCK+. This is the case for both single-ended and differential input clock modes. When I ² C is enabled (ISEL = high), this pin monitors the hot plug detect signal (see the DVI or VESA™ P&D and DFP standards). When used for hot-plug detection, this pin requires a series 1-kΩ resistor.
ISEL/RST	13	I	I ² C interface select / I ² C RESET (active low, asynchronous). If ISEL is high, then the I ² C interface is active. Default values for the I ² C registers can be found in the I ² C register descriptions section. If ISEL is low, then I ² C is disabled and the chip configuration is specified by the configuration pins (BSEL, DSEL, EDGE, V _{REF}) and state pin (PD). If ISEL is brought low and then back high, the I ² C state machine is reset. The register values are changed to their default values and are not preserved from before the reset.
MSEN	11	O	Monitor sense / programmable output 1. The operation of this pin depends on whether the I ² C interface is enabled or disabled. This pin has an open-drain output and is only 3.3-V tolerant. An external 5-kΩ pullup resistor connected to V _{DD} is required on this pin. When I ² C is disabled (ISEL = low), a high level indicates a powered-on receiver is detected at the differential outputs. A low level indicates a powered-on receiver is not detected. This function is valid only in dc-coupled systems. When I ² C is enabled (ISEL = high), this output is programmable through the I ² C interface (see the I ² C register descriptions).

Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NUMBER		
Configuration/Programming Pins (Continued)			
$\overline{\text{PD}}$	10	I	Power down (active low). In the power-down state only the digital I/O buffers and I ² C interface remain active. When I ² C is disabled (ISEL = low), a high level selects the normal operating mode. A low level selects the power-down mode. When I ² C is enabled (ISEL = high), the power-down state is selected through I ² C. In this configuration, the $\overline{\text{PD}}$ pin must be tied to GND. Note: The default register value for $\overline{\text{PD}}$ is low, so the device is in power-down mode when I ² C is first enabled or after an I ² C RESET.
RDA RCL	7 8	I/O	These terminals are the I ² C interface to the internal HDCP key EEPROM. Each terminal requires a pullup resistor in the range of 900 Ω to 5 k Ω connected to V _{DD} .
V _{REF}	3	I	Input reference voltage. Selects the swing range of the digital data inputs (DATA[23:0], DE, HSYNC, VSYNC, and IDCK \pm). For high-swing 3.3-V input signal levels, V _{REF} must be tied to V _{DD} . For low-swing input signal levels, V _{REF} must be set to half of the maximum input voltage level. See the <i>recommended operating conditions</i> section for the allowable range for V _{REF} . The desired V _{REF} voltage level is typically derived using a simple voltage divider circuit.
Reserved			
NC	49	I	No connection required. If this terminal is connected, tie it to V _{DD} .
RESERVED	34, 35	I	These pins are reserved and must be tied to GND for normal operation.
DVI Differential Signal Output Pins			
TFADJ	19	I	Full-scale adjust. This pin controls the amplitude of the DVI output voltage swing, determined by the value of the pullup resistor R _(TFADJ) connected to TV _{DD} .
TX0+ TX0–	25 24	O	Channel-0 DVI differential output pair. TX0 \pm transmits the 8-bit blue pixel data during active video and HSYNC and VSYNC during the blanking interval.
TX1+ TX1–	28 27	O	Channel-1 DVI differential output pair. TX1 \pm transmits the 8-bit green pixel data during active video and CTL[1] during the blanking interval.
TX2+ TX2–	31 30	O	Channel-2 DVI differential output pair. TX2 \pm transmits the 8-bit red pixel data during active video and CTL[3:2] during the blanking interval.
TXC+ TXC–	22 21	O	DVI differential output clock.
Power and Ground Pins			
DGND	16, 48, 64		Digital ground
DV _{DD}	1, 12, 33		Digital power supply. Must be set to 3.3 V nominal
PGND	17		PLL ground
PV _{DD}	18		PLL power supply. Must be set to 3.3 V nominal
TGND	20, 26, 32		Transmitter differential output driver ground
TV _{DD}	23, 29		Transmitter differential output driver power supply. Must be set to 3.3 V nominal

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, DV_{DD} , PV_{DD} , TV_{DD}	–0.5 V to 4 V
Input voltage, logic/analog signals	–0.5 V to 4 V
External DVI single-ended termination resistance, $R_{(T)}$	0 Ω to open circuit
External TFADJ resistance, $R_{(TFADJ)}$	300 Ω to open circuit
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 10 seconds	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
ESD protection, DVI pins	4-kV Human body model
ESD protection, all other pins	2-kV Human body model
JEDEC latchup (EIA/JESD78)	100 mA

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (DV_{DD} , PV_{DD} , TV_{DD})		3	3.3	3.6	V
Input reference voltage, V_{REF}	Low-swing mode	0.55	$V_{DDQ}/2^{\dagger}$	0.9	V
	High-swing mode		DV_{DD}		
DVI termination supply voltage, AV_{DD} (see Note 1)	At DVI receiver	3.14	3.3	3.46	V
DVI Single-ended termination resistance, $R_{(T)}$ (see Note 2)	At DVI receiver	45	50	55	Ω
TFADJ resistor for DVI-compliant $V_{(SWING)}$ range, $R_{(TFADJ)}$	400 mV = $V_{(SWING)}$ = 600 mV	505	510	515	Ω
Operating free-air temperature range, T_A		0	25	70	°C

† V_{DDQ} defines the maximum low-level input voltage, it is not an actual input voltage.

NOTES: 1. AV_{DD} is the termination supply voltage of the DVI link.

2. $R_{(T)}$ is the single-ended termination resistance at the receiver end of the DVI link.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

dc specifications

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	High-level input voltage (DATA, DE, VSYNC, HSYNC, and IDCK±)	V _{REF} = DV _{DD}	0.7V _{DD}		V	
		0.55 V ≤ V _{REF} ≤ 0.9 V	V _{REF} + 0.2			
	High-level input voltage (other inputs)		0.7V _{DD}			
V _{IL}	Low-level input voltage (DATA, DE, VSYNC, HSYNC, and IDCK±)	V _{REF} = DV _{DD}	0.3 V _{DD}		V	
		0.55 V ≤ V _{REF} ≤ 0.9 V	V _{REF} – 0.2			
	Low-level input voltage (other inputs)		0.3 V _{DD}			
V _{OH}	High-level digital output voltage (open-drain output)	V _{DD} = 3 V I _{OH} = 20 μA	2.4		V	
V _{OL}	Low-level digital output voltage (open-drain output)	V _{DD} = 3.6 V I _{OL} = 4 mA	0.4		V	
I _{IH}	High-level input current	V _I = 3.6 V	±25		μA	
I _{IL}	Low-level input current	V _I = 0	±25		μA	
V _(H)	DVI single-ended high-level output voltage	AV _{DD} = 3.3 V ±5% R _(T) [‡] = 50 Ω ±10% R _(TFADJ) = 510 Ω ±1%	AV _{DD} – 0.01	AV _{DD} + 0.01	V	
V _(L)	DVI single-ended low-level output voltage		AV _{DD} – 0.6	AV _{DD} – 0.4	V	
V _(SWING)	DVI single-ended output swing voltage		400	600	mV _{P–P}	
V _(OFF)	DVI single-ended standby/off output voltage		AV _{DD} – 0.01	AV _{DD} + 0.01	V	
I _(PD)	Power-down current (see Note 3)		200	500	μA	
I _(IDD)	Normal power supply current	Worst case pattern [§]	200	250	mA	

[‡] $R_{(T)}$ is the single-ended termination resistance at the receiver end of the DVI link.

[§] Black and white checkerboard pattern, each checker is one pixel wide.

NOTE 3: Assumes all inputs to the transmitter are not toggling.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

ac specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(IDCK)}$ IDCK frequency		25		165	MHz
$t_{(pixel)}$ Pixel time period (see Note 4)		6.06		40	ns
$t_{(IDCK)}$ IDCK duty cycle		30%		70%	
$t_{(jitt)}$ IDCK clock jitter tolerance			2		ns
t_r DVI output rise time (20–80%) (see Note 5)	$f_{(IDCK)} = 165$ MHz	75		240	ps
t_f DVI output fall time (20–80%) (see Note 5)		75		240	
$t_{sk(D)}$ DVI output intra-pair + to – differential skew (see Note 6)			50		
$t_{sk(CC)}$ DVI output inter-pair or channel-to-channel skew (see Note 6)				1.2	ns
t_{ojit} Output clock jitter, maximum (see Note 7)				150	ps
$t_{su(IDF)}$ Data, DE, VSYNC, HSYNC setup time to IDCK+ falling edge	Single edge (BSEL = 1, DSEL = 0, DKEN = 0, EDGE = 0)	1.2			ns
$t_{h(IDF)}$ Data, DE, VSYNC, HSYNC hold time to IDCK+ falling edge		1.3			
$t_{su(IDR)}$ Data, DE, VSYNC, HSYNC setup time to IDCK+ rising edge	Single edge (BSEL = 1, DSEL = 0, DKEN = 0, EDGE = 1)	1.2			ns
$t_{h(IDR)}$ Data, DE, VSYNC, HSYNC hold time to IDCK+ rising edge		1.3			
$t_{su(ID)}$ Data, DE, VSYNC, HSYNC setup time to IDCK+ falling/rising edge	Dual edge (BSEL = 0, DSEL = 1, DKEN = 0)	0.9			ns
$t_{h(ID)}$ Data, DE, VSYNC, HSYNC hold time to IDCK+ falling/rising edge		1			
$t_{(STEP)}$ De-skew trim increment	DKEN = 1		350		ps

- NOTES:
- $t_{(pixel)}$ is the pixel time defined as the period of the TXC output clock. The period of IDCK is equal to $t_{(pixel)}$.
 - Rise and fall times are measured as the time between 20% and 80% of signal amplitude.
 - Measured differentially at the 50% crossing point using the IDCK+ input clock as a trigger.
 - Relative to input clock (IDCK).

timing diagrams

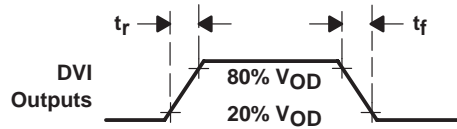


Figure 1. Rise and Fall Time for DVI Outputs

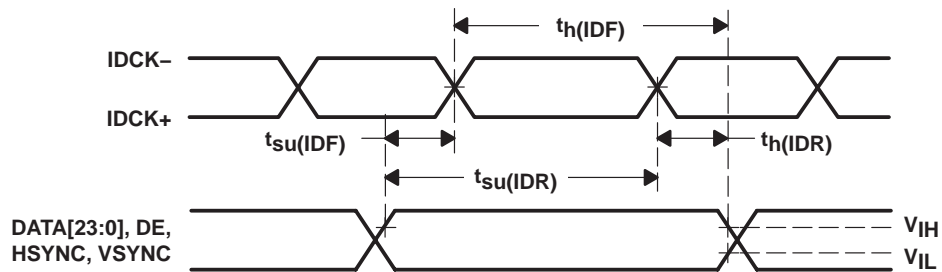


Figure 2. Control and Single-Edge-Data Setup/Hold Time to IDCK±

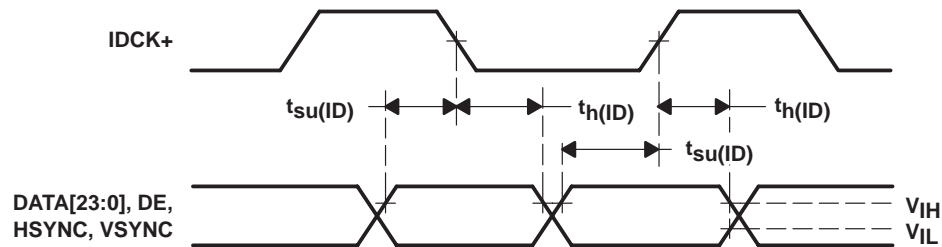


Figure 3. Dual-Edge Data Setup/Hold Times to IDCK+

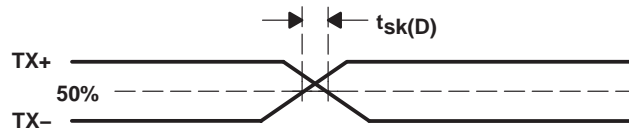


Figure 4. Analog Output Intra-Pair ± Differential Skew

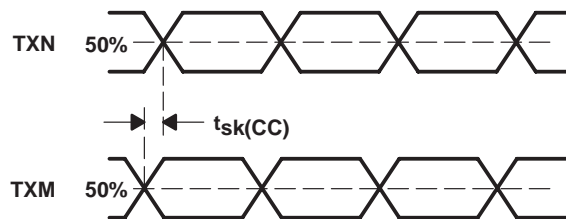


Figure 5. Analog Output Channel-to-Channel Skew

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functional description

The TFP513 is a DVI-compliant digital transmitter that is used in digital host monitor systems to T.M.D.S. encode and serialize RGB pixel data streams. The TFP513 supports resolutions from VGA to UXGA and can be controlled in two ways:

- Configuration and state pins
- The programmable I²C serial interface (see the *terminal functions* section).

The host in a digital display system, usually a PC or consumer electronics device, contains a DVI-compatible transmitter such as the TFP513 that receives 24-bit pixel data along with appropriate control signals. The TFP513 encodes the signals into a high-speed, low voltage, differential serial bit stream optimized for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor, requires a DVI compatible receiver like the TI TFP501 or TFP503 to decode the serial bit stream back to the same 24-bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the flat panel drive circuitry to produce an image on the display. Since the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred (see the *T.M.D.S. pixel data and control signal encoding*, *pixel data and control signal encoding*, *universal graphics controller interface voltage signal levels*, and *universal graphics controller interface clock inputs* sections).

The TFP513 integrates a high-speed digital interface, an HDCP cipher, a T.M.D.S. encoder, and 3 differential T.M.D.S. drivers. Data is driven to the TFP513 encoder across 12 or 24 data lines, along with differential clock pair and sync signals. The flexibility of the TFP513 allows for multiple clock and data formats that enhance system performance.

The TFP513 also has enhanced PLL noise immunity, an enhancement accomplished with on-chip regulators and bypass capacitors.

The TFP513 is versatile and highly programmable to provide maximum flexibility for the user. An I²C host interface is provided to allow enhanced configurations in addition to power-on default settings programmed by pin-strapping resistors.

The TFP513 offers monitor detection through receiver detection, or hot-plug detection when I²C is enabled. The monitor detection feature allows the user enhanced flexibility when attaching to digital displays or receivers (see the *terminal functions*, *hot-plug/unplug*, and *register descriptions* sections).

The TFP513 has a data de-skew feature allowing the users to *de-skew* the input data with respect to the IDCK± (see the *data de-skew feature* section).

The TFP513 incorporates high-bandwidth digital content protection (HDCP). This provides secure data transmission for high-definition video (see the *HDCP overview* section). The TFP513 comes with embedded preprogrammed HDCP keys, thus eliminating the need for an external storage device to store the HDCP keys and the need for the customer to purchase HDCP keys from the licensing authority. An encryption scheme ensures that the embedded HDCP keys are encrypted thus providing the highest level of key security.

T.M.D.S. pixel data and control signal encoding

For T.M.D.S., only one of two possible T.M.D.S. characters for a given pixel is transmitted at a given time. The transmitter keeps a running count of the number of 1s and 0s previously sent and transmits the character that minimizes the number of transitions and approximate a dc balance of the transmission line. Three T.M.D.S. channels transmit RGB pixel data during the active video interval (DE = high). These same three channels also transmit HSYNC, VSYNC, and three control signals, CTL[3:1], during the inactive display or blanking interval (DE = low). The following table maps the transmitted output data to the appropriate T.M.D.S. output channel in a DVI-compliant system.

INPUT PINS (VALID FOR DE = high)	T.M.D.S. OUTPUT CHANNEL	TRANSMITTED PIXEL DATA ACTIVE DISPLAY (DE = high)
DATA[23:16]	Channel 2 (TX2 ±)	Red[7:0]
DATA[15:8]	Channel 1 (TX1 ±)	Green[7:0]
DATA[7:0]	Channel 0 (TX0 ±)	Blue[7:0]
INPUT PINS (VALID FOR DE = low)	T.M.D.S. OUTPUT CHANNEL	TRANSMITTED CONTROL DATA BLANKING INTERVAL (DE = low)
CTL3, CTL2 (see Note 8)	Channel 2 (TX2 ±)	CTL[3:2]
CTL1 (see Note 8)	Channel 1 (TX1 ±)	CTL[1]
HSYNC, VSYNC	Channel 0 (TX0 ±)	HSYNC, VSYNC

NOTE 8: The TFP513 encodes and transfers the CTL[3:1] inputs during the vertical blanking interval. The TFP513 internally generates CTL3 for HDCP operation and the CTL[2:1] inputs are reserved for future use. When DE = high, the CTL and SYNC pins must be held constant.

universal graphics controller interface voltage signal levels

The universal graphics controller interface can operate in the following two distinct voltage modes:

- The high-swing mode where standard 3.3-V CMOS signaling levels are used.
- The low-swing mode where adjustable 1.1-V to 1.8-V signaling levels are used.

To select the high-swing mode, the V_{REF} input pin must be tied to the 3.3-V power supply.

To select the low-swing mode, the V_{REF} input range must be 0.55 V to 0.9 V.

In the low-swing mode, V_{REF} sets the midpoint of the adjustable signaling levels. The allowable range of values for V_{REF} is from 0.55 V to 0.9 V. The typical approach is to provide V_{REF} to the chip using a simple voltage-divider circuit. The minimum allowable input signal swing in the low-swing mode is $V_{REF} \pm 0.2$ V. In low-swing mode, the V_{REF} input is common to all differential input receivers.

universal graphics controller interface clock inputs

The universal graphics controller interface supports both single-ended and fully differential clock input modes. In the differential clock input mode, the universal graphics controller interface uses the crossover point between the IDCK+ and IDCK– signals as the timing reference for latching incoming data (DATA[23:0], DE, HSYNC, and VSYNC). Differential clock inputs provide greater common-mode noise rejection. The differential clock input mode is only available in the low-swing mode. In the single-ended clock input mode, the IDCK+ input (pin 57) must be connected to the single-ended clock source and the IDCK– input (pin 56) must be tied to GND.

The universal graphics controller interface provides selectable 12-bit, dual-edge and 24-bit, single-edge input clocking modes. In the 12-bit, dual-edge mode, the 12-bit data is latched on each edge of the input clock. In the 24-bit, single-edge mode, the 24-bit data is latched on the rising edge of the input clock when EDGE = 1 and the falling edge of the input clock when EDGE = 0.

DKEN and DK[3:1] allow the user to compensate the skew between IDCK± and the pixel data and control signals. See the description of the CTL_3_MODE register for details.

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universal graphics controller interface modes

Table 1 is a tabular representation of the different modes for the universal graphics controller interface. The 12-bit mode is selected when BSEL = 0 and the 24-bit mode when BSEL = 1. The 12-bit mode uses dual-edge clocking and the 24-bit mode uses single-edge clocking. The EDGE input controls the latching edge in 24-bit mode or the primary latching edge in 12-bit mode. When EDGE = 1, the data input is latched on the rising edge of the input clock; and when EDGE = 0, the data input is latched on the falling edge of the input clock. A fully differential input clock is available only in the low-swing mode. Single-ended clocking is not recommended in the low-swing mode as this decreases common-mode noise rejection.

Note that BSEL, DSEL, and EDGE are determined by register CTL_1_MODE when I²C is enabled (ISEL = 1) and by input pins when I²C is disabled (ISEL = 0).

Table 1. Universal Graphics Controller Interface Options

V _{REF}	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK EDGE	CLOCK MODE
0.55 V – 0.9 V	0	0	0	12-bit	Dual-edge	Falling	Differential (see Notes 9 and 10)
0.55 V – 0.9 V	0	0	1	12-bit	Dual-edge	Falling	Single-ended
0.55 V – 0.9 V	0	1	0	12-bit	Dual-edge	Rising	Differential (see Notes 9 and 10)
0.55 V – 0.9 V	0	1	1	12-bit	Dual-edge	Rising	Single-ended
0.55 V – 0.9 V	1	0	0	24-bit	Single-edge	Falling	Single-ended
0.55 V – 0.9 V	1	0	1	24-bit	Single-edge	Falling	Differential (see Notes 9 and 11)
0.55 V – 0.9 V	1	1	0	24-bit	Single-edge	Rising	Single-ended
0.55 V – 0.9 V	1	1	1	24-bit	Single-edge	Rising	Differential (see Notes 9 and 11)
DV _{DD}	0	0	X	12-bit	Dual-edge	Falling	Single-ended (see Note 12)
DV _{DD}	0	1	X	12-bit	Dual-edge	Rising	Single-ended (see Note 12)
DV _{DD}	1	0	X	24-bit	Single-edge	Falling	Single-ended (see Note 12)
DV _{DD}	1	1	X	24-bit	Single-edge	Rising	Single-ended (see Note 12)

- NOTES: 9. The differential clock input mode is only available in the low signal swing mode (that is, V_{REF} ≤ 0.9 V).
10. The TFP513 does not support a 12-bit, dual-clock, single-edge input clocking mode.
11. The TFP513 does not support a 24-bit, single-clock, dual-edge input clocking mode.
12. In the high-swing mode (V_{REF} = DV_{DD}), DSEL is a don't care; therefore, the device is always in the single-ended latch mode.

universal graphics controller interface modes (continued)

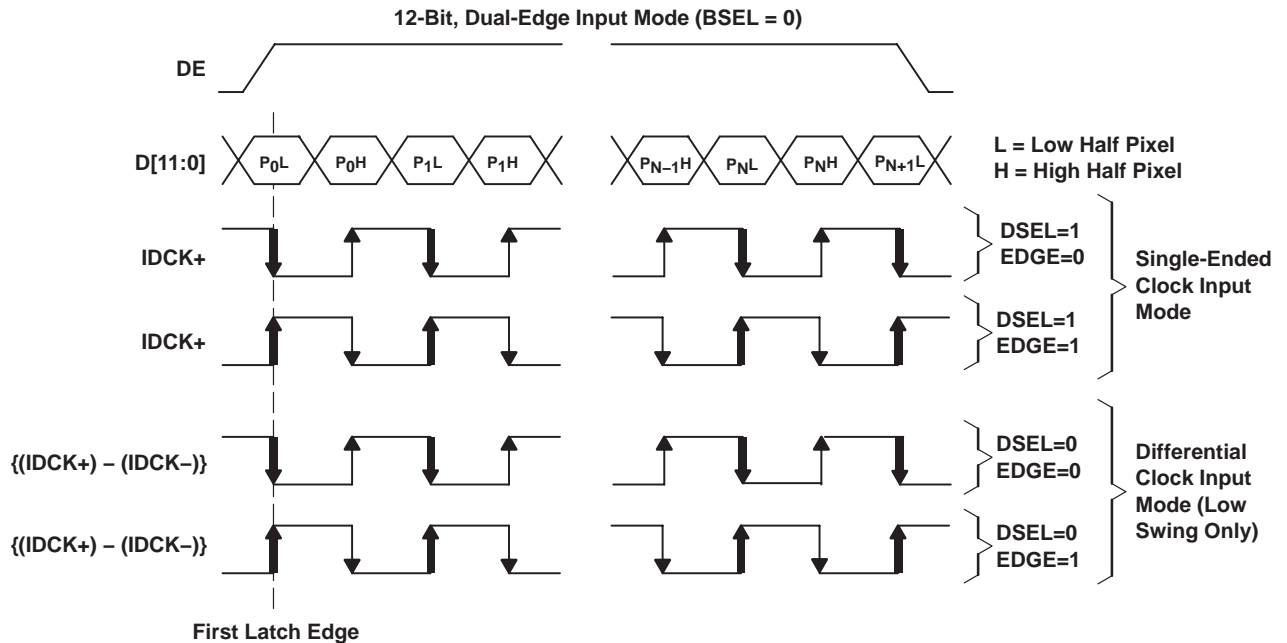


Figure 6. Universal Graphics Controller Interface Options for 12-Bit Mode

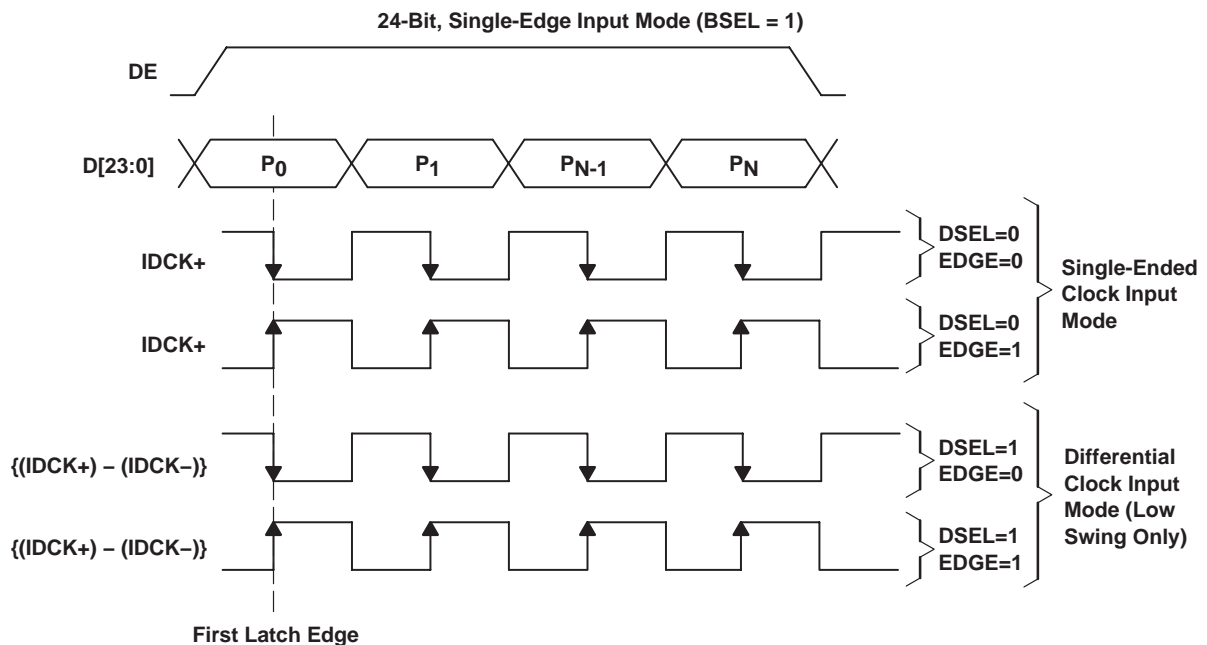


Figure 7. Universal Graphics Controller Interface Options for 24-Bit Mode

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12-bit mode data mapping

PIN NAME	P0		P1		P2	
	P0L	P0H	P1L	P1H	P2L	P2H
	LOW	HIGH	LOW	HIGH	LOW	HIGH
D11	G0[3]	R0[7]	G1[3]	R1[7]	G2[3]	R2[7]
D10	G0[2]	R0[6]	G1[2]	R1[6]	G2[2]	R2[6]
D9	G0[1]	R0[5]	G1[1]	R1[5]	G2[1]	R2[5]
D8	G0[0]	R0[4]	G1[0]	R1[4]	G2[0]	R2[4]
D7	B0[7]	R0[3]	B1[7]	R1[3]	B2[7]	R2[3]
D6	B0[6]	R0[2]	B1[6]	R1[2]	B2[6]	R2[2]
D5	B0[5]	R0[1]	B1[5]	R1[1]	B2[5]	R2[1]
D4	B0[4]	R0[0]	B1[4]	R1[0]	B2[4]	R2[0]
D3	B0[3]	G0[7]	B1[3]	G1[7]	B2[3]	G2[7]
D2	B0[2]	G0[6]	B1[2]	G1[6]	B2[2]	G2[6]
D1	B0[1]	G0[5]	B1[1]	G1[5]	B2[1]	G2[5]
D0	B0[0]	G0[4]	B1[0]	G1[4]	B2[0]	G2[4]

24-bit mode data mapping

PIN NAME	P0	P1	P2	PIN NAME	P0	P1	P2
D23	R0[7]	R1[7]	R2[7]	D11	G0[3]	G1[3]	G2[3]
D22	R0[6]	R1[6]	R2[6]	D10	G0[2]	G1[2]	G2[2]
D21	R0[5]	R1[5]	R2[5]	D9	G0[1]	G1[1]	G2[1]
D20	R0[4]	R1[4]	R2[4]	D8	G0[0]	G1[0]	G2[0]
D19	R0[3]	R1[3]	R2[3]	D7	B0[7]	B1[7]	B2[7]
D18	R0[2]	R1[2]	R2[2]	D6	B0[6]	B1[6]	B2[6]
D17	R0[1]	R1[1]	R2[1]	D5	B0[5]	B1[5]	B2[5]
D16	R0[0]	R1[0]	R2[0]	D4	B0[4]	B1[4]	B2[4]
D15	G0[7]	G1[7]	G2[7]	D3	B0[3]	B1[3]	B2[3]
D14	G0[6]	G1[6]	G2[6]	D2	B0[2]	B1[2]	B2[2]
D13	G0[5]	G1[5]	G2[5]	D1	B0[1]	B1[1]	B2[1]
D12	G0[4]	G1[4]	G2[4]	D0	B0[0]	B1[0]	B2[0]

data de-skew feature

The de-skew feature allows adjustment of the input setup/hold time. Specifically, the input data DATA[23:0] can be latched slightly before or after the latching edge of the clock IDCK± depending on the amount of de-skew desired. When de-skew enable (DKEN) is enabled, the amount of de-skew is programmable by setting the three bits DK[3:1]. When disabled, a default de-skew setting is used. DKEN and DK[3:1] are accessed through registers only when I²C is enabled.

The input setup/hold time (see Figure 8) can be varied with respect to the input clock by an amount t_{CD} given by the formula:

$$t_{CD} = (DK[3:1] - 4) \times t_{STEP}$$

where:

t_{STEP} is the adjustment increment amount

DK[3:1] is a number from 0 to 7 represented as a 3-bit binary number

t_{CD} is the cumulative de-skew amount

(DK[3:1]-4) is simply a multiplier in the range {-4,-3,-2,-1, 0, 1, 2, 3} for t_{STEP} . Therefore, data can be latched in increments from 4 times the value of t_{STEP} before the latching edge of the clock to 3 times the value of t_{STEP} after the latching edge. Note that the input clock is not changed, only the time when data is latched with respect to the clock.

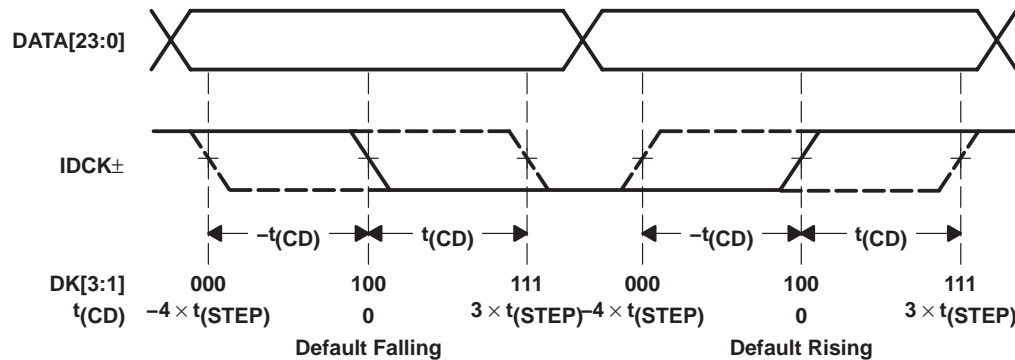


Figure 8. De-Skew Function Timing Diagram

hot plug/unplug (auto connect/disconnect detection)

The TFP513 supports hot plug/unplug (auto connect/disconnect detection) for the DVI link. The receiver sense input (RSEN) bit indicates if a DVI receiver is connected to TXC+ and TXC-. The HTPLG bit reflects the current state of the HTPLG pin connected to the monitor via the DVI connector. When I²C is disabled (ISEL = 0), the RSEN value is available on the MSEN pin. When I²C is enabled, the connection status of the DVI link and HTPLG sense pins is provided by the CTL_2_MODE register. The MSEL bits of the CTL_2_MODE register can program the MSEN to output the HTPLG value, the RSEN value, an interrupt, or be disabled.

The source of the interrupt event is selected by TSEL in the CTL_2_MODE register. An interrupt is generated by a change in status of the selected signal. The interrupt status is indicated in the MDI bit of CTL_2_MODE and can be output on the MSEN pin. The interrupt continues to be asserted until a 1 is written to the MDI bit, resetting the bit back to 1. Writing 0 to the MDI bit has no effect.

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device configuration and I²C RESET description

The TFP513 device configuration can be programmed by several different methods to allow maximum flexibility for the user's application. Device configuration is controlled by the state of the ISEL/RST pin, configuration pins (BSEL, DSEL, EDGE, V_{REF}), and state pin (PD). I²C bus select and I²C RESET (active low) are shared functions on the ISEL/RST pin, which operates asynchronously.

Holding ISEL/RST low causes the device configuration to be set by the configuration pins (BSEL, DSEL, EDGE, and V_{REF}) and state pin (PD). The I²C bus is disabled.

Holding ISEL/RST high causes the device configuration to be set by the configuration bits (BSEL, DSEL, EDGE) and state bits (PD, DKEN) in the I²C registers. The I²C bus is enabled.

Momentarily bringing ISEL/RST low and then back high while the device is operating in normal or power-down mode resets the I²C registers to their default values, and the device configuration is changed to the default power-up state with I²C enabled. After power up, the device must be reset. It is suggested that a low going pulse with 100-ns minimum width be applied to this pin after all the power supplies are fully functional.

DE generator

The TFP513 contains a DE generator that can generate an internal DE signal when the original data source does not provide one. There are several I²C programmable values that control the DE generator (see Figure 9). Register sizes limit the supportable resolutions. DE_GEN in the DE_CTL register enables this function. When enabled, the DE pin is ignored.

DE_TOP and DE_LIN are line counts that control the number of lines after VSYNC goes active that DE is enabled, and the total number of lines that DE remains active, respectively. The polarity of VSYNC must be set by VS_POL in the DE_CTL register.

DE_DLY and DE_CNT are pixel counts that control the number of pixels after HSYNC goes active that DE is enabled, and the total number of pixels that DE remains active, respectively. The polarity of HSYNC must be set by HS_POL in the DE_CTL register.

The TFP513 also counts the total number of HSYNC pulses between VSYNC pulses, and the total number of pixels between HSYNC pulses. These values, the total vertical and horizontal resolutions, are available in V_RES and H_RES, respectively. These values are available at all times, whether or not the DE generator is enabled.

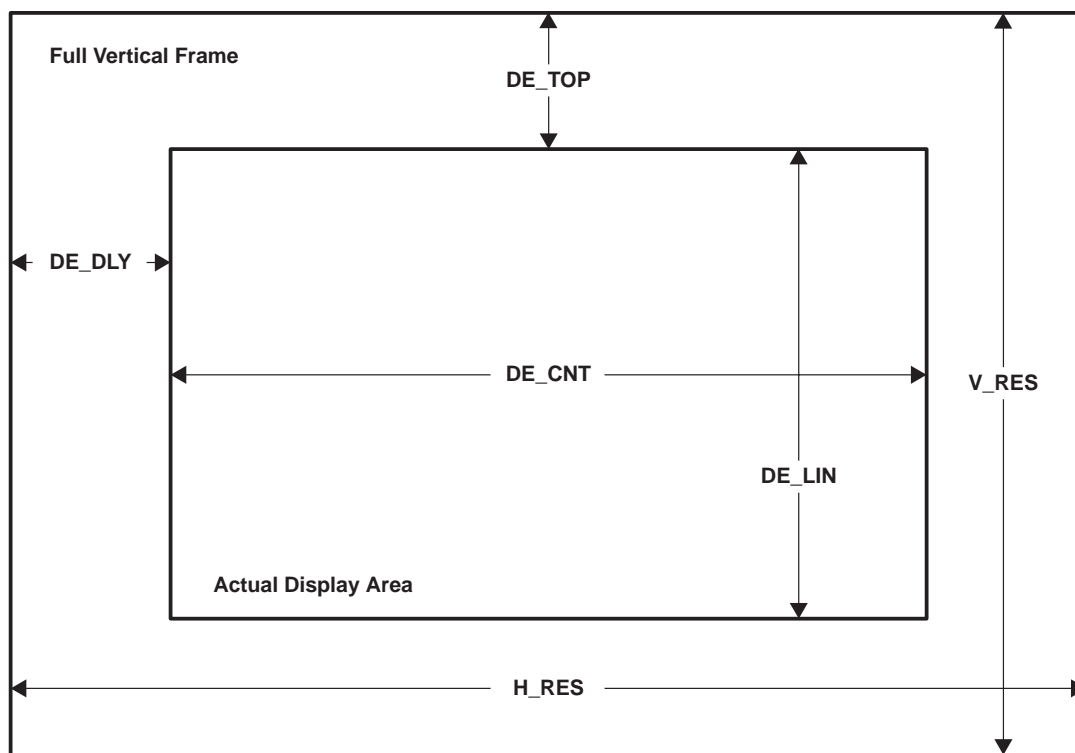


Figure 9. DE Generator Register Functions

HDCC overview

The TFP513 provides high-bandwidth digital content protection (HDCC) by encrypting the transmitted active pixel data stream sent to an HDCC receiver (like the TFP501). The HDCC algorithm is fully incorporated, and only requires an external source of HDCC keys and a software driver to implement an HDCC host.

The HDCC technology requires adherence to the HDCC license's compliance (available from www.digital-cp.com) and robustness rules. These rules require that HDCC implementation both protect the confidentiality of keys and other values from compromise as well as deliver the desired protection for high-value video content. The TFP513 provides a complete, easily implemented solution to these requirements.

The TFP513 HDCC operation requires use of the I²C interface. Details of the TFP513 HDCC operation are available in a separate document.

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register map

The TFP513 is a standard I²C slave device. All the registers can be written and read through the I²C interface (unless otherwise specified). The TFP513 slave machine supports only byte read and write cycles. Page mode is not supported. The 8-bit binary address of the I²C machine is 0111 000X, where X = 0 for write and X = 1 for read on the TFP513.

REGISTER	RW	SUB-ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VEN_ID	R	00	VEN_ID[7:0]							
	R	01	VEN_ID[15:8]							
DEV_ID	R	02	DEV_ID[7:0]							
	R	03	DEV_ID[15:8]							
REV_ID	R	04	REV_ID[7:0]							
RESERVED	R	05-07	Reserved							
CTL_1_MODE	RW	08	RSVD	TDIS	VEN	HEN	DSEL	BSEL	EDGE	$\overline{\text{PD}}$
CTL_2_MODE	RW	09	VLOW	MSEL			TSEL	RSEN	HTPLG	MDI
CTL_3_MODE	RW	0A	DK			DKEN	RSVD	CTL		RSVD
CFG	R	0B	CFG							
RESERVED	RW	0C-31	Reserved							
DE_DLY	RW	32	DE_DLY[7:0]							
DE_CTL	RW	33	RSVD	DE_GEN	VS_POL	HS_POL	Reserved			DE_DLY[8]
DE_TOP	RW	34	RSVD	DE_DLY[6:0]						
RESERVED	RW	35	Reserved							
DE_CNT	RW	36	DE_CNT[7:0]							
	RW	37	Reserved					DE_CNT[10:8]		
DE_LIN	RW	38	DE_LIN[7:0]							
	RW	39	Reserved					DE_LIN[10:8]		
H_RES	R	3A	H_RES[7:0]							
	R	3B	Reserved					H_RES[10:8]		
V_RES	R	3C	V_RES[7:0]							
	R	3D	Reserved					V_RES[10:8]		
RESERVED	R	3E-FF	Reserved							

register descriptions

VEN_ID			Subaddress = 01–00			Read Only		Default = 0x014C	
7	6	5	4	3	2	1	0		
VEN_ID[7:0]									
VEN_ID[15:8]									

These read-only registers contain the 16-bit Texas Instruments vendor ID. VEN_ID is hardwired to 0x014C.

DEV_ID			Subaddress = 03–02			Read Only		Default = 0x0510	
7	6	5	4	3	2	1	0		
DEV_ID[7:0]									
DEV_ID[15:8]									

These read-only registers contain the 16-bit device ID. DEV_ID is hardwired to 0x0510 for the TFP513.

register descriptions (continued)

REV_ID		Subaddress = 04		Read Only		Default = 0x00	
7	6	5	4	3	2	1	0
REV_ID[7:0]							

This read-only register contains the revision ID.

RESERVED		Subaddress = 07–05		Read Only		Default = 0x641400	
7	6	5	4	3	2	1	0
Reserved							

CTL_1_MODE		Subaddress = 08		Read/Write		Default = 0xBE	
7	6	5	4	3	2	1	0
RSVD	TDIS	VEN	HEN	DSEL	BSEL	EDGE	$\overline{\text{PD}}$

$\overline{\text{PD}}$: This read/write register contains the power-down mode.

- 0: Power down (default after RESET)
- 1: Normal operation

EDGE: This read/write register contains the edge select mode.

- 0: Input data latches to the falling edge of IDCK+.
- 1: Input data latches to the rising edge of IDCK+.

BSEL: This read/write register contains the input bus select mode.

- 0: 12-bit operation with dual-edge clock
- 1: 24-bit operation with single-edge clock

DSEL: This read/write register is used in combination with BSEL and VREF to select the single-ended or differential input clock mode. In the high-swing mode, DSEL is a don't care because IDCK is always single-ended.

HEN: This read/write register contains the horizontal sync enable mode.

- 0: HSYNC input is transmitted as a fixed low.
- 1: HSYNC input is transmitted in its original state.

VEN: This read/write register contains the vertical sync enable mode.

- 0: VSYNC input is transmitted as a fixed low.
- 1: VSYNC input is transmitted in its original state.

TDIS: This read/write register contains the T.M.D.S. disable mode.

- 0: T.M.D.S. circuitry enable state is determined by $\overline{\text{PD}}$.
- 1: T.M.D.S. circuitry is disabled.

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register descriptions (continued)

CTL_2_MODE		Subaddress = 09		Read/Write		Default = 0x00	
7	6	5	4	3	2	1	0
VLOW	MSEL[3:1]			TSEL	RSEN	HTPLG	MDI

MDI: This read/write register contains the monitor detect interrupt mode.

- 0: Detected logic level change in detection signal (to clear, write 1 to this bit).
- 1: Logic level remains the same.

HTPLG: This read-only register contains the hot plug detection input logic state.

- 0: Low level detected on the EDGE/HTPLG pin (pin 9).
- 1: High level detected on the EDGE/HTPLG pin (pin 9).

RSEN: This read only register contains the receiver sense input logic state, which is valid only for dc-coupled systems.

- 0: A powered-on receiver is not detected.
- 1: A powered-on receiver is detected (that is, connected to the DVI transmitter outputs).

TSEL: This read/write register contains the interrupt generation source select.

- 0: Interrupt bit (MDI) is generated by monitoring RSEN.
- 1: Interrupt bit (MDI) is generated by monitoring HTPLG.

MSEL[3:1]: This read/write register contains the source select of the monitor sense output pin.

- 000: Disabled. MSEN output high.
- 001: Outputs the MDI bit (interrupt).
- 010: Outputs the RSEN bit (receiver detect).
- 011: Outputs the HTPLG bit (hot plug detect).

VLOW: This read-only register indicates the V_{REF} input level.

- 0: This bit is a logic level 0 if the V_{REF} analog input selects high-swing inputs.
- 1: This bit is a logic level 1 if the V_{REF} analog input selects low-swing inputs.

CTL_3_MODE		Subaddress = 0A		Read/Write		Default = 0x80	
7	6	5	4	3	2	1	0
DK[3:1]			DKEN	RSVD	CTL[2:1]		RSVD

CTL[2:1]: This read/write register contains the values of the two CTL[2:1] bits that are output on the DVI port during the blanking interval. CTL[3] is not available on the TFP513 because it is internally generated by the HDCP circuitry.

DKEN: This read/write register controls the data de-skew enable.

- 0: Data de-skew is disabled; the values in DK[3:1] are not used.
- 1: Data de-skew is enabled; the de-skew setting is controlled through DK[3:1].

DK[3:1]: This read/write register contains the de-skew setting, each increment adjusts the skew by t_{STEP} .

- 000: Step 1 (minimum setup/maximum hold)
- 001: Step 2
- 010: Step 3
- 011: Step 4
- 100: Step 5 (default)
- 101: Step 6
- 110: Step 7
- 111: Step 8 (maximum setup/minimum hold)

register descriptions (continued)

CFG		Subaddress = 0B			Read Only		
7	6	5	4	3	2	1	0
CFG[7:0] (D[23:16])							

This read-only register contains the state of the inputs D[23:16]. These pins can provide the user with selectable configuration data through the I²C bus.

RESERVED		Subaddress = 0E–0C			Read/Write		Default = 0x97D0A9
7	6	5	4	3	2	1	0
Reserved							
Reserved							
Reserved							

These read/write registers have no effect on TFP513 operation.

DE_DLY		Subaddress = 32			Read/Write		Default = 0x00
7	6	5	4	3	2	1	0
DE_DLY[7:0]							

This read/write register defines the number of pixels after HSYNC goes active that DE is generated, when the DE generator is enabled. The value must be less than or equal to (2047 – DE_CNT).

DE_CTL		Subaddress = 33			Read/Write		Default = 0x00
7	6	5	4	3	2	1	0
Reserved	DE_GEN	VS_POL	HS_POL	Reserved			DE_DLY[8]

DE_DLY[8]: This read/write register contains the top bit of DE_DLY.

HS_POL: This read/write register sets the HSYNC polarity.

- 0: HSYNC is considered active low.
- 1: HSYNC is considered active high.
- Pixel counts are reset on the HSYNC active edge.

VS_POL: This read/write register sets the VSYNC polarity.

- 0: VSYNC is considered active low.
- 1: VSYNC is considered active high.
- Line counts are reset on the VSYNC active edge.

DE_GEN: This read/write register enables the internal DE generator.

- 0: DE generator is disabled. Signal required on DE pin
- 1: DE generator is enabled. DE pin is ignored.

DE_TOP		Subaddress = 34			Read/Write		Default = 0x00
7	6	5	4	3	2	1	0
DE_TOP[7:0]							

This read/write register defines the number of pixels after VSYNC goes active that DE is generated, when the DE generator is enabled.

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register descriptions (continued)

DE_CNT		Subaddress = 37–36		Read/Write		Default = 0x0000	
7	6	5	4	3	2	1	0
DE_CNT[7:0]							
Reserved				DE_CNT[10:8]			

These read/write registers define the width of the active display, in pixels, when the DE generator is enabled. The value must be less than or equal to (2047 – DE_DLY).

DE_LIN		Subaddress = 39–38		Read/Write		Default = 0x0000	
7	6	5	4	3	2	1	0
DE_LIN[7:0]							
Reserved				DE_LIN[10:8]			

These read/write registers define the height of the active display, in lines, when the DE generator is enabled.

H_RES		Subaddress = 3B–3A		Read Only			
7	6	5	4	3	2	1	0
H_RES[7:0]							
Reserved				H_RES[10:8]			

These read-only registers return the number of pixels between consecutive HSYNC pulses.

V_RES		Subaddress = 3D–3C		Read Only			
7	6	5	4	3	2	1	0
V_RES[7:0]							
Reserved				V_RES[10:8]			

These read-only registers return the number of lines between consecutive VSYNC pulses.

I²C interface

The I²C interface is used to access the internal registers. This two-pin interface consists of the SCL clock line and the SDA serial data line. The basic I²C access cycles are shown in Figure 10 and Figure 11.

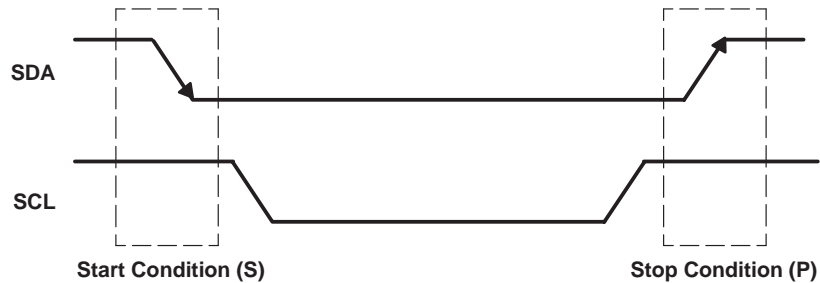


Figure 10. I²C Start and Stop Conditions

The basic access write cycle consists of the following:

1. A start condition
2. A slave address cycle
3. A subaddress cycle
4. Any number of data cycles
5. A stop condition

The basic access read cycle consists of the following:

1. A start condition
2. A slave write address cycle
3. A subaddress cycle
4. A restart condition
5. A slave read address cycle
6. Any number of data cycles
7. A stop condition

The start and stop conditions are shown in Figure 10. The high-to-low transition of SDA while SCL is high defines the start condition. The low-to-high transition of SDA while SCL is high defines the stop condition. Each cycle, data or address, consists of 8 bits of serial data followed by one acknowledge bit generated by the receiving device. Thus, each data/address cycle contains 9 bits as shown in Figure 11.

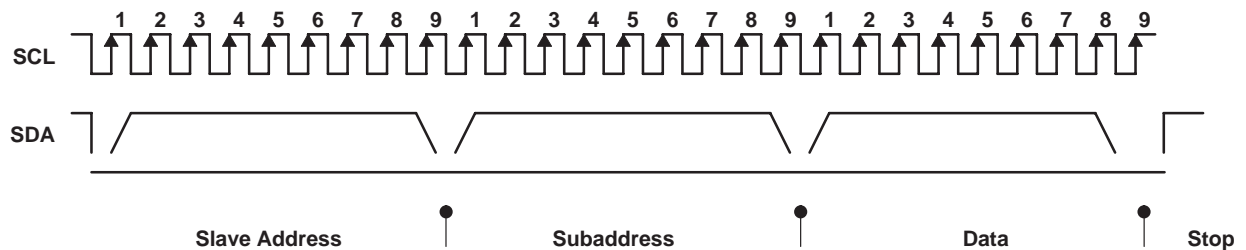


Figure 11. I²C Access Cycles

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I²C interface (continued)

Following a start condition, each I²C device decodes the slave address. The TFP513 responds with an acknowledge by pulling the SDA line low during the ninth clock cycle if it decodes the address as its address. During subsequent subaddress and data cycles, the TFP513 responds with acknowledge as shown in Figure 12. The subaddress is auto-incremented after each data cycle.

The transmitting device must not drive the SDA signal during the acknowledge cycle so that the receiving device may drive the SDA signal low. The master indicates a *not acknowledge* condition (/A) by keeping the SDA signal high just before it asserts the stop condition (P). This sequence terminates a read cycle as shown in Figure 13.

In order to minimize the number of bits that must be transferred for the HDCP link integrity check, a second read format is supported. This access, shown in Figure 14, has an implicit subaddress equal to the starting location for the HDCP receiver link verification response (R').

The slave address consists of 7 bits of address along with 1 bit of read/write information (that is, read = 1 and write = 0) as shown in Figure 12 through Figure 14. For the TFP513 the slave addresses are 0x70 for write cycles and 0x71 for read cycles.

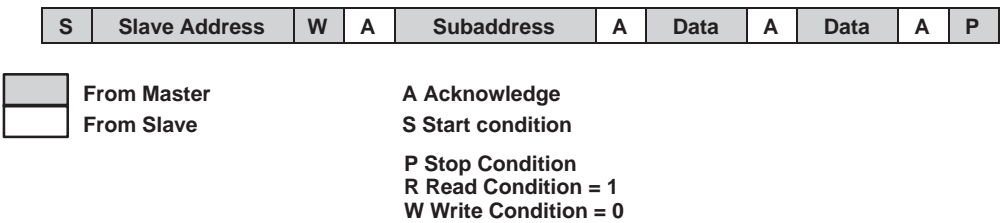


Figure 12. I²C Write Cycle

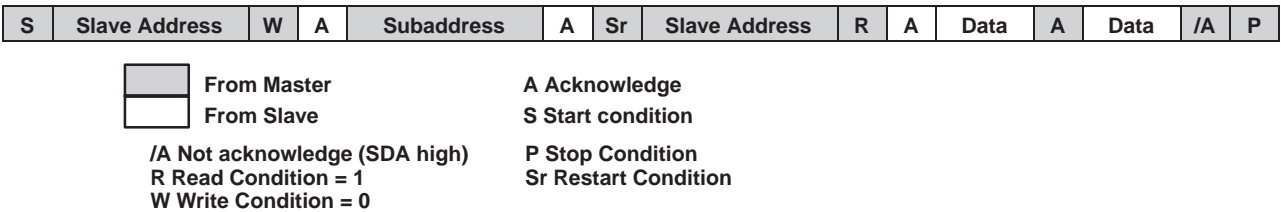


Figure 13. I²C Read Cycle

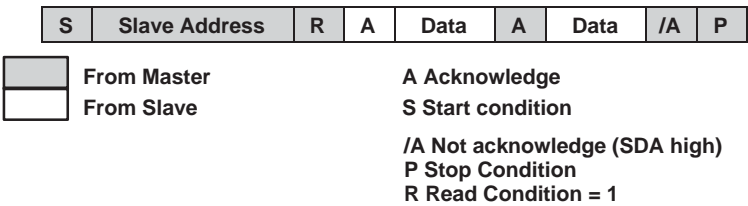


Figure 14. HDCP Port Link Integrity Message Read

TI 64-pin TQFP PowerPAD package

The TFP513 is available in TI's thermally enhanced 64-pin TQFP PowerPAD package. The PowerPAD package is a 10-mm × 10-mm × 1,0-mm TQFP outline with 0,5-mm lead-pitch. The PowerPAD package has a specially designed die mount pad that offers improved thermal capability over typical TQFP packages of the same outline. The TI 64-pin TQFP PowerPAD package offers a backside solder plane that connects directly to the die mount pad for enhanced thermal conduction. For thermal considerations, soldering the backside of the TFP513 to the application board is not required because the device power dissipation is well within the package capability when not soldered. If traces or vias are located under the backside pad, they must be protected by a suitable solder mask or other assembly technique to prevent inadvertent shorting to the exposed backside pad.

Soldering the backside of the device to a thermal land connected to the PCB ground plane is recommended for electrical and EMI considerations. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

The recommended pad size for the grounded thermal land is 5,5 mm minimum, centered in the device land pattern. When vias are required to ground the land, multiple vias are recommended for a low impedance connection to the ground plane. Vias in the exposed pad must be small enough or filled to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow.

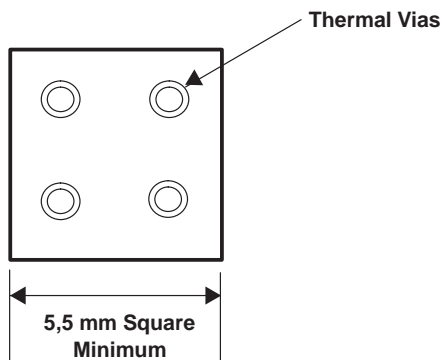


Figure 15. Thermal Vias

Table 2 contains the thermal properties of the TI 64-pin TQFP PowerPAD package. The 64-pin TQFP non-PowerPAD package is included only for reference.

Table 2. TI 64-Pin TQFP (10 × 10 × 1,0 mm)/0,5 mm Lead-Pitch

PARAMETER		WITHOUT PowerPAD™	PowerPAD™ NOT CONNECTED TO PCB THERMAL PLANE	PowerPAD™ CONNECTED TO PCB THERMAL PLANE (see Note 14)
R _{θJA}	Thermal resistance, junction-to-ambient (see Notes 13 and 14)	75.83°C/W	42.20°C/W	22.43°C/W
R _{θJC}	Thermal resistance, junction-to-case (see Notes 13 and 14)	7.80°C/W	0.38°C/W	0.38°C/W
P _D	Power handling capabilities of package (see Notes 13, 14, and 15)	0.92 W	1.66 W	3.26 W

NOTES: 13. Specified with the bond pad on the backside of the PowerPAD package soldered to a 2-oz. Cu plate PCB thermal plane
14. Airflow is at 0 LFM (no airflow).
15. Specified at 150°C junction temperature and 80°C ambient temperature

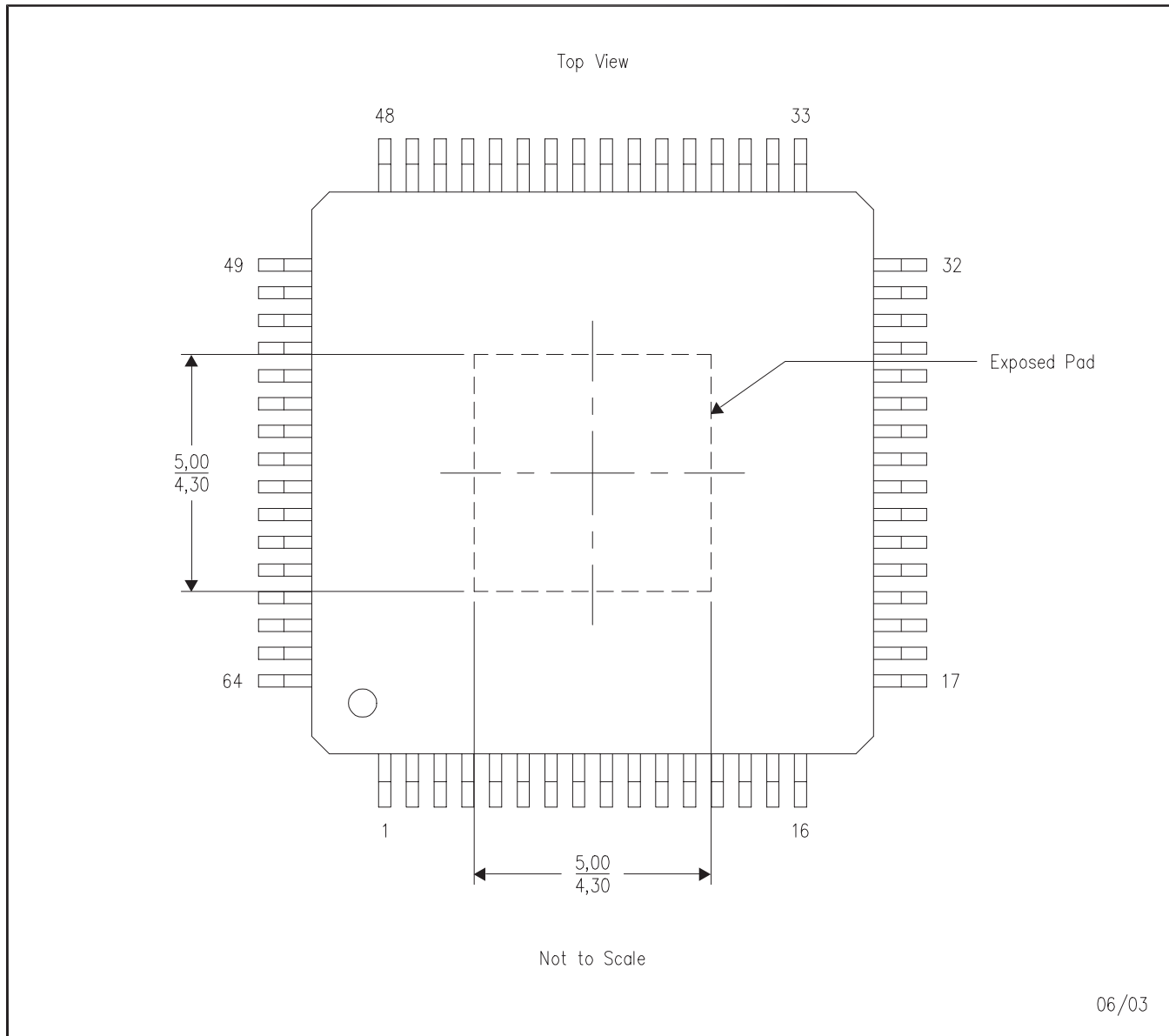
TFP513

TI *PanelBus*™ DIGITAL TRANSMITTER

SLLS611 – AUGUST 2004

PAP (S-PQFP-G64)

PowerPAD™ PLASTIC QUAD FLATPACK



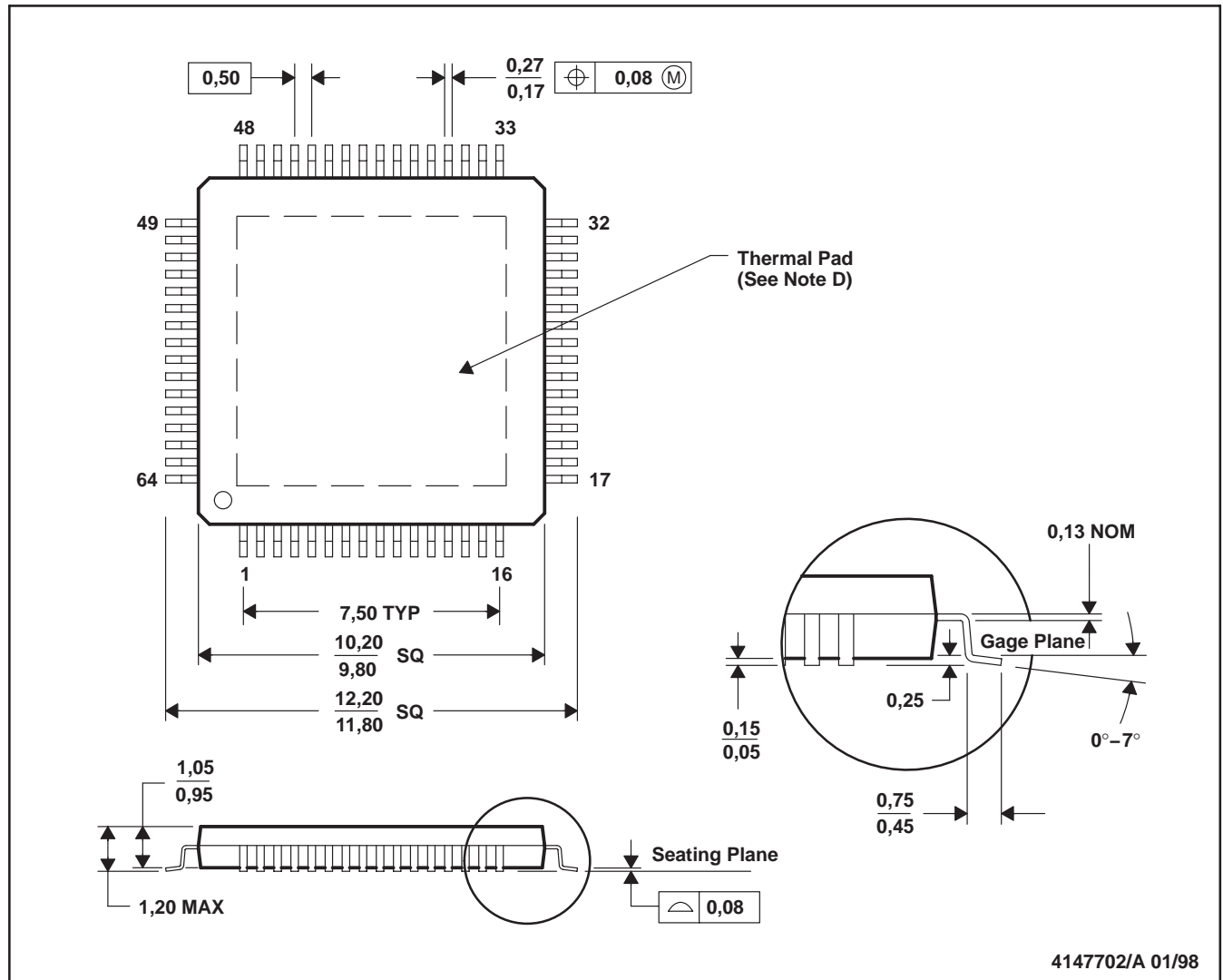
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, **PowerPAD Thermally Enhanced Package**, Texas Instruments Literature No. SLMA002 and Application Brief, **PowerPAD Made Easy**, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

PowerPAD is a trademark of Texas Instruments

MECHANICAL DATA

PAP (S-PQFP-G64)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 - E. Falls within JEDEC MS-026

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TFP513PAP	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TFP513PAPG4	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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