Features and Benefits

- Fully compatible with J2411 Single Wire CAN specification for Class B in vehicle communications
- 30 µA typical power consumption in sleep mode independent from CAN voltage range
- Operating voltage range 5…18V
- Up to 100 kbps high-speed transmission mode
- Up to 40 kbps bus speed
- Selective BUS wakeup
- Low RFI due to output wave shaping
- Fully integrated receiver filter
- Bus terminals proof against short-circuits and transients in automotive environment
- Loss of ground protection
- Protection against load dump, jump start
- Thermal overload and short circuit protection
- ESD protection of 4 kV on CAN pin (2kV on any other pin)
- Under- and over voltage lock out
- Bus dominant timeout feature

Ordering Information

Part No.	Temperature Suffix	Package
TH8055	J (-40 ….125 °C)	DC (SOIC 150mil)

General Description

The TH8055 is a physical layer device for a single wire data link capable of operating with various CSMA/CR protocols such as the Bosch Controller Area Network (CAN) version 2.0. This serial data link network is intended for use in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor and/or dedicated logic devices which use the network.

The network shall be able to operate in either the normal data rate mode or a high speed data download mode for assembly line and service data transfer operations. The high speed mode is only intended to be operational when the bus is attached to an off-board service node. This node shall provide temporary bus electrical loads which facilitate higher speed operation. Such temporary loads shall be removed when not performing download operations.

The bit rate for normal communications is typically 33 kbit/s, for high speed transmissions like described above a typical bit rate of 83 kbit/s is recommended. The TH8055 is designed in accordance to the Single Wire CAN Physical Layer Specification GMW3089 V1.4 and supports many additional features like undervoltage lockout , timeout for faulty blocked input signals, output blanking time in case of bus ringing and a very low sleep mode current.

Functional Diagram

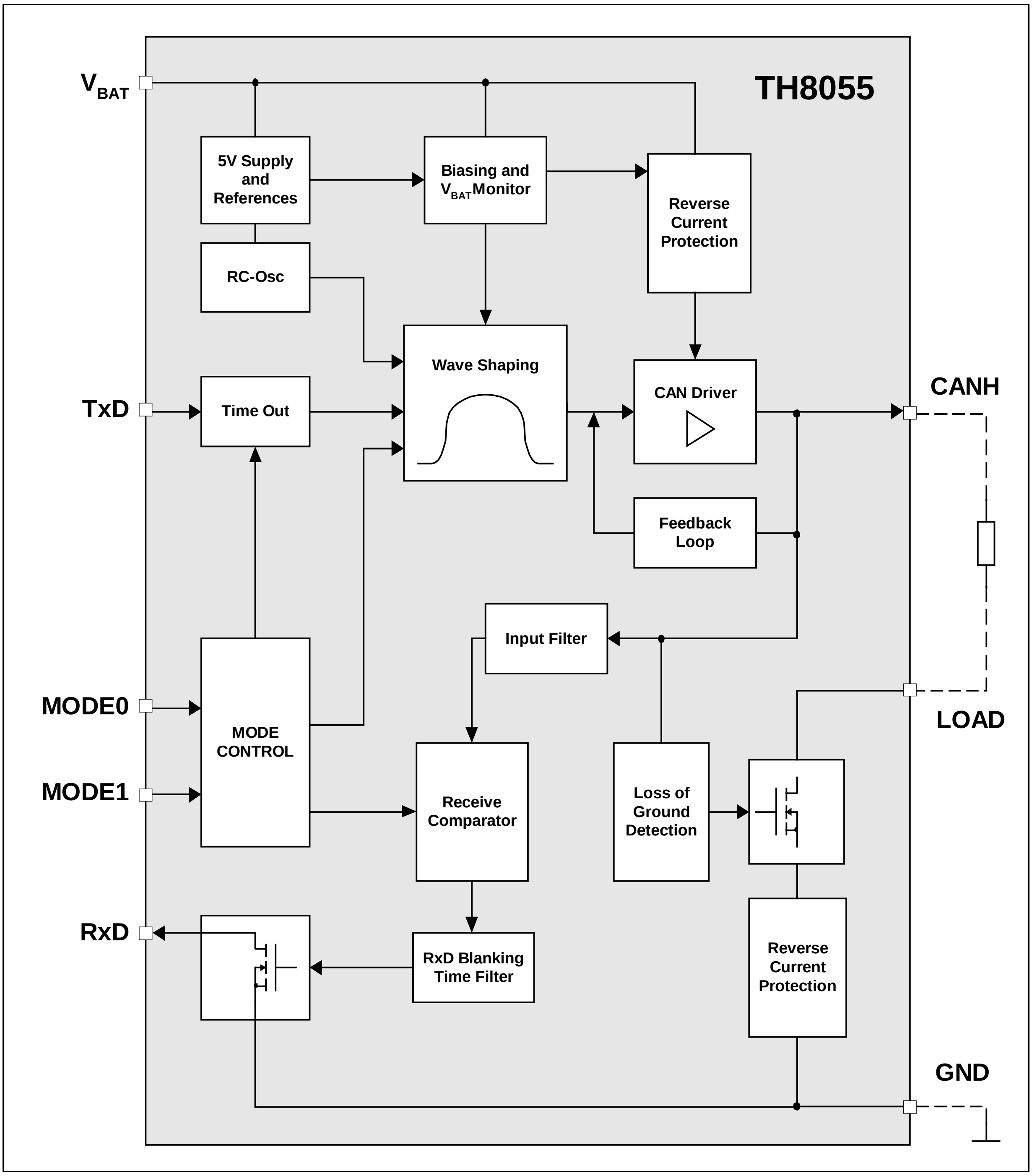


Figure 1- Block Diagram

Functional Description

TxD Input Pin - *Logic command to transmit on the single wire CAN bus as follows:*

TxD Polarity

- TxD = logic 1 (or floating) on this pin produce an undriven or recessive bus state (low bus voltage)
- TxD = logic 0 on this pin produce either a bus normal or a bus high voltage dominant state depending on the transceiver mode state (high bus voltage)

If the TxD pin is driven to a logic low state while the sleep mode (Mode0=0 and Mode1=0) is activated, the transceiver not drive the CANH pin to the dominant state.

The transceiver provides an internal pull up current on the TxD pin which will cause the transmitter to default to the bus recessive state when TxD is not driven.
TxD input signals are standard CMOS logic levels.

Timeout Feature

In case of a faulty blocked dominant TxD input signal the CANH output is switched off automatically after the specified TxD timeout reaction time to prevent a dominant bus.
The transmission is continued by next TxD L to H transition without delay.

Mode 0 and Mode 1 pins - *are used to select transceiver operating modes:*

The transceiver provides a weak internal pull down current on each of these pins which causes the transceiver to default to sleep mode when they are not driven. The mode input signals are standard CMOS logic level.

M0	M1	Mode
L	L	Sleep mode
H	L	High speed mode
L	H	Wake up
H	H	Normal mode

Sleep Mode

Transceiver is in low power state, waiting for wake up via high voltage signal or by mode pins change to any state other than 0,0. In this state, the CANH pin is not in the dominant state regardless of the state of the TxD pin.

High Speed Mode

This mode allows high speed download with bitrates up to 100Kbit/s. The output waveshaping circuit is disabled in this mode. Bus transmitter drive circuits for those nodes which are required to communicate in high speed mode are able to drive reduced bus resistance in this mode (see Table Static Characteristics). High speed communications shall utilize the normal mode signal voltage levels as specified in Static Characteristics.

Wake Up Mode

This bus includes a selective node awake capability, which allows normal communication to take place among some nodes while leaving the other nodes in an undisturbed sleep state. This is accomplished by controlling the signal voltages such that all nodes must wake up when they receive a higher voltage message signal waveform. The communication system communicates to the nodes information as to which nodes are to stay operational (awake) and which nodes are to put themselves into a non communicating low power “sleep” state. Communication at the lower, normal voltage levels shall not disturb the sleeping nodes.

Normal mode

Transmission bit rate in normal communication is 33 Kbits/s. In normal transmission mode the TH8055 supports controlled waveform rise and overshoot times. Waveform trailing edge control is required to assure that high frequency components are minimized at the beginning of the downward voltage slope. The remaining fall time occurs after the bus is inactive with drivers off and is determined by the RC time constant of the total bus load.

RxD Output pin - Logic data as sensed on the single wire CAN bus

RxD polarity

- RxD = logic 1 on this pin indicates a bus recessive state (low bus voltage)
- RxD = logic 0 on this pin indicates a bus normal or high voltage bus dominant state

RxD in Sleep Mode

RxD do not pass signals to the micro processor while in sleep mode until a valid wake up bus voltage level is received or the Mode 0,1 pins are not 0,0 respectively. When the valid wake up bus voltage signal awakens the transceiver, the RxD pin signalised an interrupt (logic 0). However, if the Mode 0 & 1 pins are at logic 0, the transceiver returns to the sleep condition when the wake up bus voltage signal is not present.
When not in sleep mode all valid bus signals will be sent out on the RxD pin.
RxD will be placed in the undriven or off state when in sleep mode .

RxD Typical Load

Resistance: 2.5 kohms
Capacitance: < 25 pF

Bus LOAD pin - Resistor ground with internal open-on-loss-of-ground protection

When the ECU experiences a loss of ground condition, this pin switch to a high impedance state.
The ground connection through this pin is not interrupted in any transceiver operating mode including the sleep mode. The ground connection only is interrupted when there is a valid loss of ground condition.

This pin provides the bus load resistor with a path to ground which contributes less than 0.1 volts to the bus offset voltage when sinking the maximum current through one unit load resistor.
The transceiver's maximum bus leakage current contribution to VOL from the LOAD pin when in a loss of ground state is 50uA over all operating temperatures and 3.5 < VBAT < 18 volts .

V_{BAT} INPUT pin - Vehicle Battery Voltage

The transceiver is fully operational as described in Table Static Characteristics over the range $5 < V_{BAT} < 18$ volts as measured between the GND pin and the V_{BAT} pin.

For $0 < V_{BAT} < 5$ volts, the bus is passive (not be driven dominant) and RxD is undriven (high), regardless of the state of the TxD pin (undervoltage lockout).

CAN BUS input/output pin

Wave Shaping in normal and wake up mode

Wave shaping is incorporated into the transmitter to minimize EMI radiated emissions. An important contributor to emissions is the rise and fall times during output transitions at the "corners" of the voltage waveform. The resultant waveform is one half of a sin wave of frequency 50 - 65 kHz at the rising waveform edge and one quarter of this sin wave at falling or trailing edge.

Wave Shaping in high speed mode

Wave shaping control of the rising and falling waveform edges are disabled during high speed mode. EMI emissions requirements are waived during this mode. The waveform rise time in this mode is less than one µs.

Short circuits

If the CAN BUS pin is shorted to ground for any duration of time, an over temperature shut down circuit disables the output high side drive source transistor before the local die temperature exceeds the damage limit threshold.

Loss of ground

If the CANH voltage decreases under the specified value below the ECU - ground, the LOAD pin is switched into high impedance state. The CANH transmission is continued until the undervoltage lock out voltage threshold is detected.

Loss of battery

In case of loss of battery (VBAT = 0 or open) the transceiver do not disturb bus communication. The maximum reverse current into power supply system doesn't exceed 500µA.

Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC. The absolute maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the TH8055 is only specified within the limits shown in ”Operating conditions”.

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery voltage	V_{BAT}	5.0	18	V
Operating ambient temperature	T_A	-40	125	°C
Junction temperature	T_J	-40	150	°C

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	VBAT		-0.3	18	V
Short-term supply voltage	VBAT.LD	Load dump; t<500ms		40	V
		Jump start; t<1 min		27	
Transient supply voltage	VBAT.TR1	ISO 7637/1 pulse 1 [1]	-50		V
Transient supply voltage	VBAT.TR2	ISO 7637/1 pulses 2 [1]		100	V
Transient supply voltage	VBAT.TR3	ISO 7637/1 pulses 3A, 3B	-200	200	V
CANH voltage	VCANH	VBAT=0	-20	40	V
Transient bus voltage	VCANHTR1	ISO 7637/1 pulse 1 [2]	-50		V
Transient bus voltage	VCANHTR2	ISO 7637/1 pulses 2 [2]		100	V
Transient bus voltage	VCANHTR3	ISO 7637/1 pulses 3A, 3B [2]	-200	200	V
DC voltage on pin LOAD	VLOAD	via RT > 2k	-40	40	V
DC voltage on pins TxD,MODE1,MODE0,RxD	VDC		-0.3	7	V
ESD capability of CANH	VESDBUS	Human body model Equivalent to discharge 100pF with 1.5k	-4000	4000	V
ESD capability of any other pins	VESD	Human body model Equivalent to discharge 100pF with 1.5k	-2000	2000	V
Maximum latch-up free current at any Pin	ILATCH		-500	500	mA
Maximum power dissipation	Ptot	At TA = 125 °C		197 [3]	mW
Thermal impedance	JA	in free air		152	K/W
Storage temperature	TSTG		-55	150	°C
Junction temperature	TJ		-40	150	°C

[1] ISO 7637 test pulses are applied to VBAT via a reverse polarity diode and >1uF blocking capacitor .
[2] ISO 7637 test pulses are applied to CANH via a coupling capacitance of 1 nF.
[3] The application board shall be realized with a ground copper foil area > $25mm^2$.

Static Characteristics

V_{BAT} = 5.0 to 18V, T_A = -40 to +125°C, unless otherwise specified
All voltages are refered to ground, positive currents flow into the IC.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN VBAT						
Operating supply voltage	V_{BAT}		5.0	12	18	V
Undervoltage lock out	V_{BATUV}		4.5		4.95	V
Overvoltage lock out	V_{BATOV}		18.5		21	V
Normal mode supply current, dominant	I_{BATNd}	V_{BAT} = 18V MODE0=MODE1=H, TxD=L, noload		3.5	5	mA
Normal mode supply current, recessiv	I_{BATNr}	V_{BAT} = 18V MODE0=MODE1=H, TxD open		3.5	5	mA
Wake up mode supply current	I_{BATW}	V_{BAT} = 18V MODE0=L,MODE1=H, TxD=L		4	5	mA
Sleep mode supply current	I_{BATS}	V_{BAT} = 18V TxD, RxD, MODE0, MODE1 open		30	60	µA
PIN CANH						
Bus output voltage	V_{OH}	R_L > 100Ω Normal, high speed mode 5.5V < V_{BAT} < 18V	3.5		4.55	V
Fixed wakeup output high voltage	$V_{OHWUFix}$	Wake-up mode, R_L>270Ω 11.2V < V_{BAT} < 18V	9.7		12	V
Offset wakeup output high voltage	$V_{OHWUOffs}$	Wake-up mode, R_L>270Ω 5.5V < V_{BAT} < 11.2V	V_{BAT} -1.5		V_{BAT}	V
Recessive state output voltage	V_{OL}	Recessive state or sleep mode, R_{load} = 9.1 kΩ,			0.20	V
Bus short circuit current	$I_{CANSHORT}$	V_{CANH} = 0V, V_{BAT}=18V, TxD=0V	40		150	mA
Bus leakage current during loss of ground [1]	I_{LKNCAN}	Loss of ground, V_{CANH}=0V	-50		10	µA
Bus leakage current, bus positive	I_{LKPCAN}	TxD high	-10		10	µA
Bus input threshold	V_{IH}	Normal, high-speed mode	1.8		2.2	V
Fixed wakeup input high voltage threshold [2]	$V_{IHWUFix}$	Sleep mode VBAT > 11.2V	6.15		8.1	V
Offset wakeup input high voltage threshold [2]	$V_{IHWUOffs}$	Sleep mode	V_{BAT} -4.3		V_{BAT} -3.25	V
Maximum reverse current into CANH	$I_{CANHOVlob}$	V_{CANH} > V_{BAT}			1	mA
Loss of ground detection threshold	$V_{CANHLOG}$	TxD open	-1600		-200	mV
PIN LOAD						
Voltage on switched ground pin	V_{LOAD}	I_{RTH} = 5mA			0.5	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN TXD,MODE0,MODE1						
High level input voltage	V_{IH}		3.4			V
Low level input voltage	V_{IL}				1.6	V
TxD pull up current	I_{IL_TXD}	TxD=L, MODE0 and 1=H	20		50	µA
MODE0 and 1 pull down current	I_{IH_MODE0}	MODE0 and 1=H	15		50	µA
PIN RXD						
Low level output voltage	V_{OLRxD}	I_{RxD} = 2mA			0.4	V
High level output leakage	I_{IHRxD}	V_{RxD}=5V	-10		10	µA
RxD output current	I_{RxD}	V_{RxD}=5V			70	mA
Overtemperature protection						
Thermal shutdown [3]	T_{SD}		155		180	°C
Thermal recovery [3]	T_{REC}		130		150	°C

[1] Leakage current in case of Loss of ground is the summary of both currents I_{LKN_CAN} and I_{LKN_RTH} .
[2] Wake up is detected at the minimum of $V_{ihWuFix}$ or $V_{ihWuOffset}$.
[3] thresholds not tested in production, guaranteed by design, only switch on/off tested

Dynamic Characteristics

All dynamic values of the table below refer to the timing diagrams on page 6.
($5.5V \le V_{BAT} \le 18V$, $-40°C \le T_A \le 125°C$, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Transmit delay in normal and wake up mode	t_T	max. and min bus load, 50% TXD high level to V_{CANH}=2.2V	3		6.3	µs
Transmit delay in high-speed mode	t_{THS}	max. and min bus load, 50% TXD high level to V_{CANH}=2.2V	0.2		1.5	µs
Receive delay in all active modes	t_{DR}	CANH to RxD, V_{CANH}=2V , RxD=L to H	0.3		1	µs
Receive delay in all active modes	t_{RD}	CANH to RxD, V_{CANH}=2V , RxD=L to H	0.3		1	µs
Input minimum pulse length, all active modes	t_{rp}	CANH to RxD, V_{CANH}=2V , RxD=H to L	0.2		1	µs
Input minimum pulse length, all active modes	t_{pr}	CANH to RxD, V_{CANH}=2V , RxD=L to H	0.2		1	µs
Bus output rise time (30%-70%)	t_R	Normal mode, max. and min bus loads,V_{BAT}=12V	0.6		1.4	µs
Bus output fall time (70%-30%)	t_F	Normal mode, max. and min bus loads, V_{BAT}=12V	1.3		4.7	µs
Bus output rise time (30%-70%)	t_{RHS}	High-speed mode, max. and min. bus loads, V_{BAT}=12V			0.5	µs
Bus output fall time (70%-30%)	t_{FHS}	High-speed mode, max. and min. bus loads, V_{BAT}=12V	1.6		2.5	µs
Wakeup filter time delay	t_{WUF}	See Timing diagrams	10		70	µs
Receive blanking time after TxD L-H transition	t_{RB}	See Timing diagrams	2		6	µs
TxD timeout reaction time	t_{TOUT}	Normal and high speed mode		12		ms
TxD timeout reaction time	t_{TOUTWA}	Wake up mode		20		ms
Delay from normal to high speed modes	t_{DNHS}				30	µs
Delay from normal to wake up mode	t_{DNHV}				30	µs
Delay from normal to sleep modes	t_{DNS}				500	µs
Delay from sleep to normal and wake up mode	t_{dsnwu}				50	µs

Bus loading requirements

Parameter	Symbol	Min	Typ	Max	Unit
Number of system nodes		2		32	
Network distance between any two ECU nodes	Bus length			60	m
Node series Inductor Resistance	R_{ind}			2.3	Ω
EMC Inductor voltage drop	V_{ind}			0.3	V
Ground offset voltage	V_{goff}			0.8	V
Device capacitance (unit load)	C_{ul}	198	220	242	pF
Network total capacitance	C_{tl}	396		13700	pF
Device resistance (unit load)	R_{ul}	9009	9100	9191	Ω
Device resistance (min load)	R_{min}	2000			Ω
Network total resistance	R_{tl}	270		4596	Ω
Network time constant [1]	τ	1		4	µs
High speed mode network resistance to GND	R_{load}	100		185	Ω

Timing Diagrams

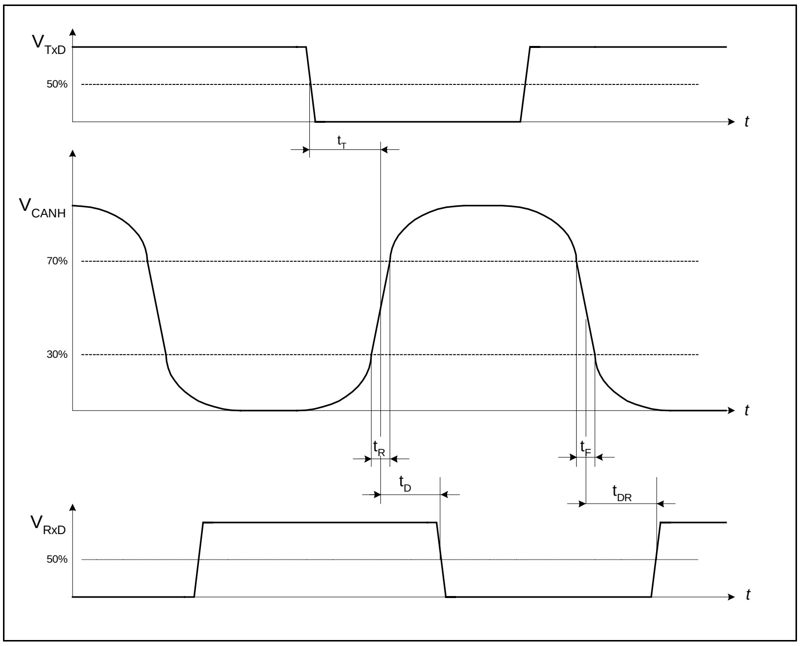


Figure 2 - Input/Output Timing

[1] The network time constant incorporates the bus wiring capacitance. The minimum value is selected to limit radiated emission. The maximum value is selected to ensure proper communication modes. Not all combinations of R and C are possible.

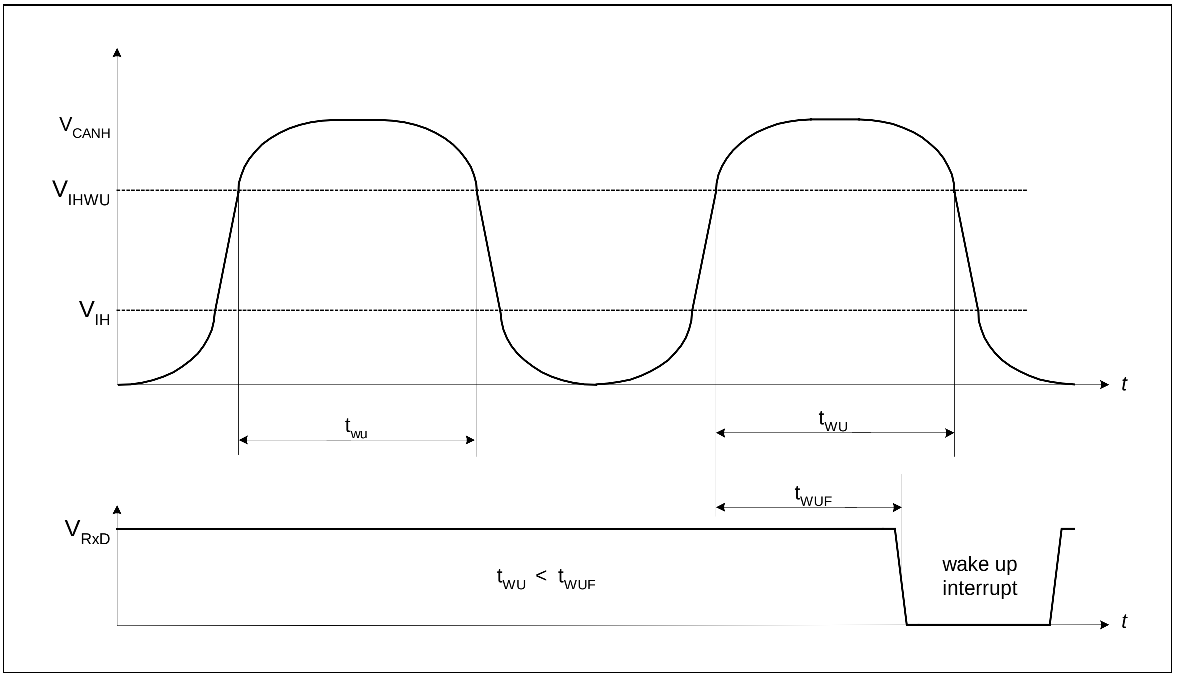


Figure 3 - Wake Up Filter Time Delay

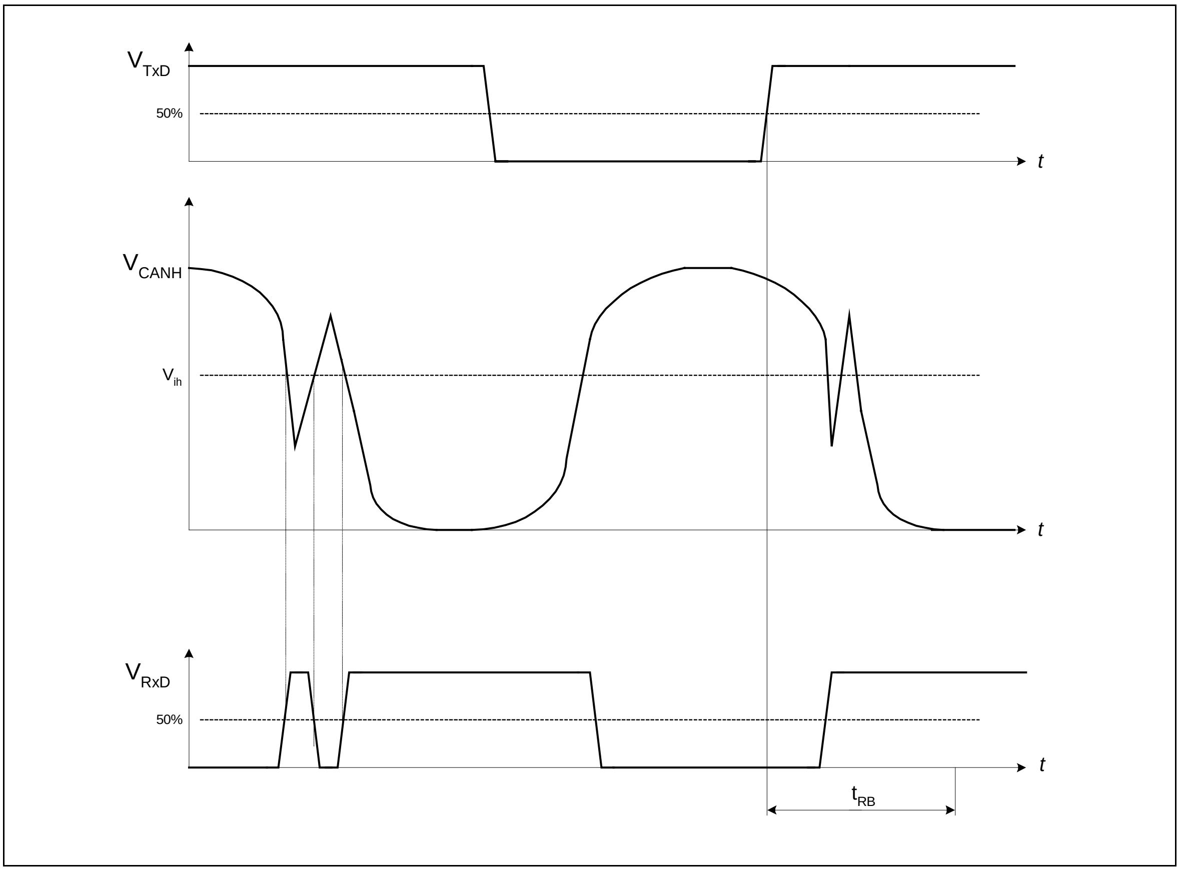


Figure 4 - Receive Blanking Time

Application Circuitry

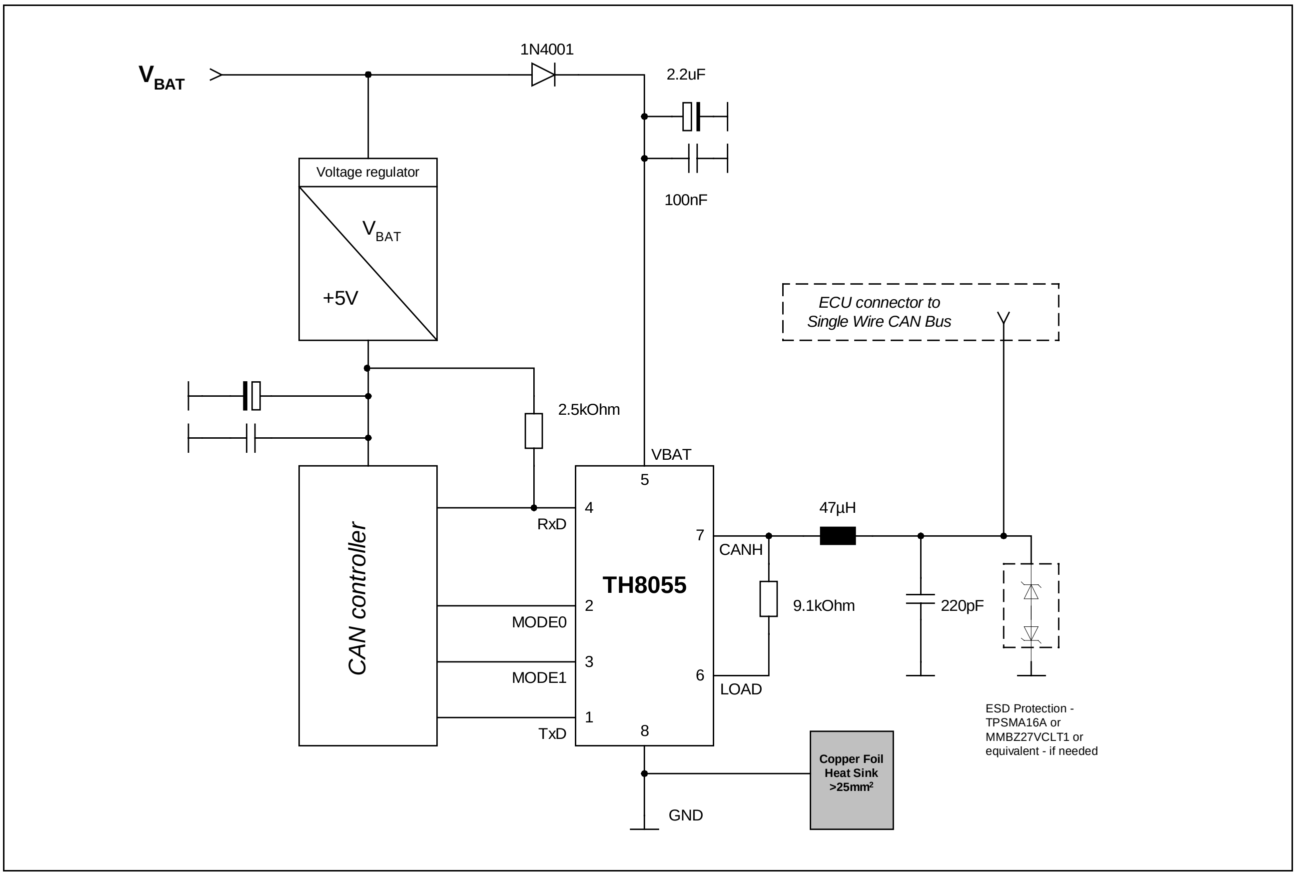


Figure 5 - Application Circuitry

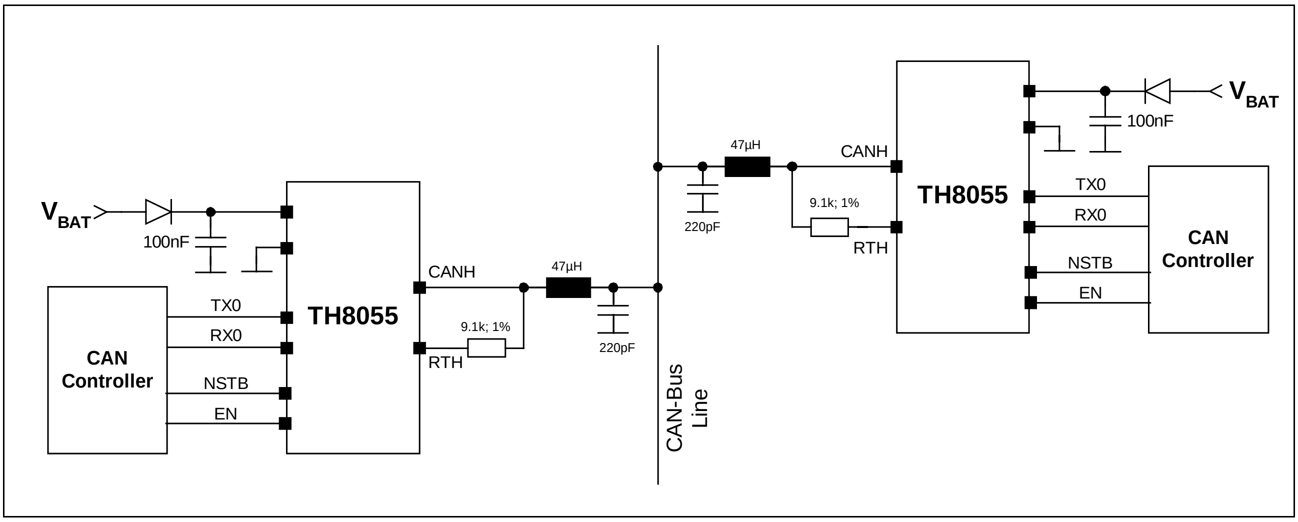
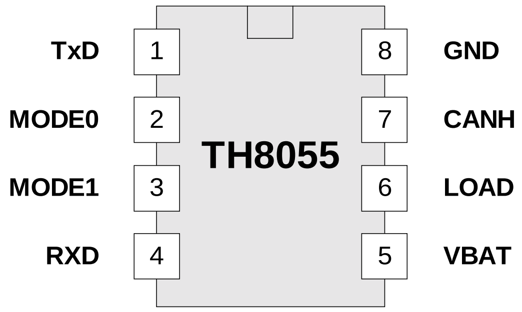


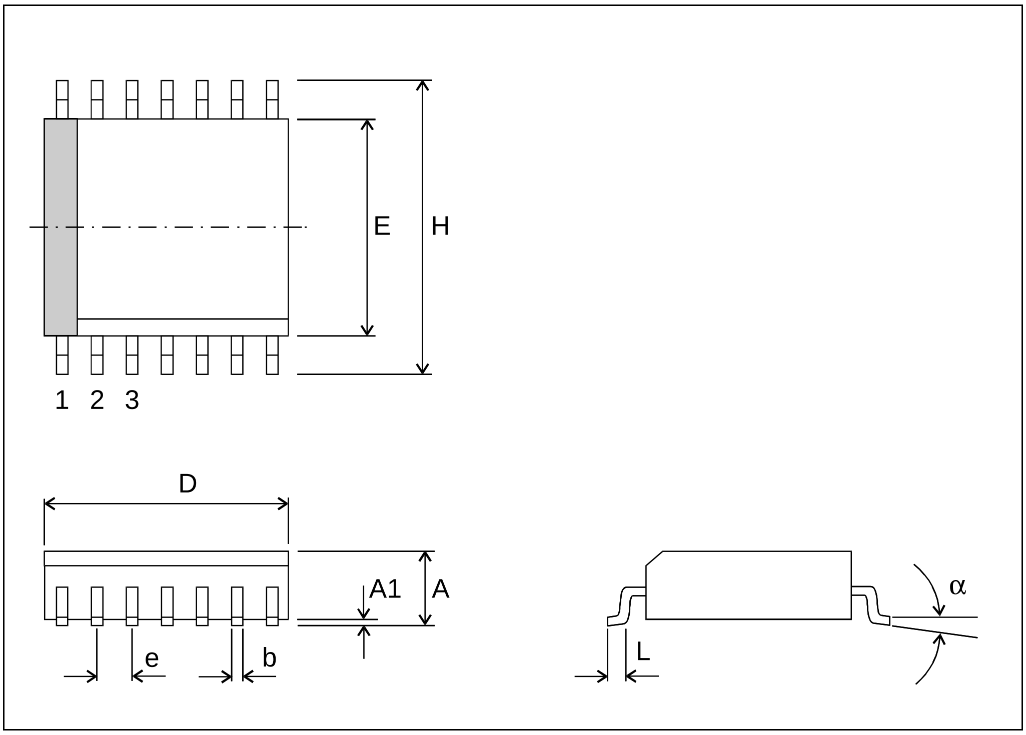
Figure 6 - CAN Network Circuitry

Pin Description



Pin	Name	IO-Typ	Description
1	TXD	I	Transmit data from core to CAN
2	MODE0	I	Operating mode select input 0
3	MODE1	I	Operating mode select input 1
4	RXD	O	Receive data from CAN to core
5	VBAT		Battery input voltage
6	LOAD		Resistor load (loss of ground low side switch)
7	CANH	I/O	Single wire CAN bus pin
8	GND		Ground

Mechanical Specification



Small Outline Integrated Circiut (SOIC), SOIC8 NB, 150 mil

All Dimension in mm, coplanarity < 0.1 mm									
	D	**E**	**H**	**A**	**A1**	**e**	**b**	**L**	**α**
min max	4.85.0	3.80 4.00	10.00 10.65	5.80 6.20	0.10 0.25	1.27	0.33 0.51	0.40 1.27	0°8° 0.10
All Dimension in inch, coplanarity < 0.004"									
min max	0.189 0.197	0.150 0.157	0.228 0.244	0.053 0.069	0.004 0.010	0.050	0.013 0.020	0.016 0.050	0° 8°

Your notes

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