THC63LVD823

Single(135MHz)/Dual(170MHz) Link LVDS Transmitter for SXGA/SXGA+/UXGA

General Description

The THC63LVD823 transmitter is designed to support Single Link transmission between Host and Flat Panel Display up to SXGA+ resolutions and Dual Link transmission between Host and Flat Panel Display up to UXGA resolutions.

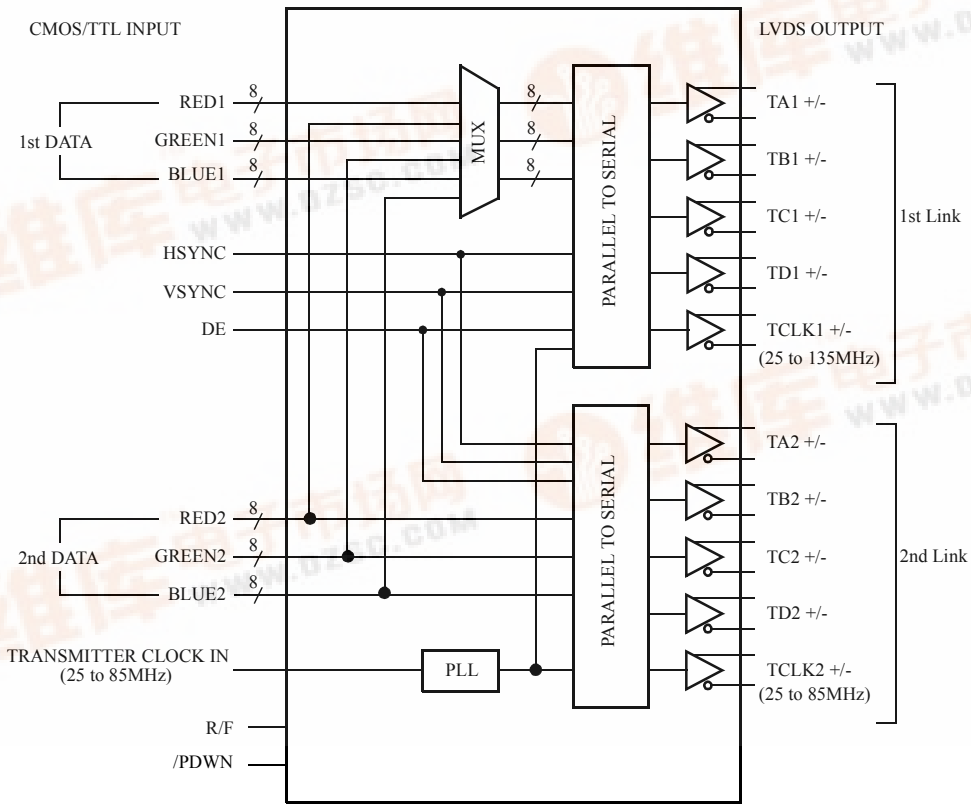
The THC63LVD823 converts 48bits of CMOS/TTL data into LVDS(Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. In Single Link, the transmit clock frequency of 135MHz, 48bits of RGB data are transmitted at an effective rate of 945Mbps per LVDS channel. Using a 135MHz clock, the data throughput is 472Mbytes per second.

In Dual Link, the transmit clock frequency of 85MHz, 48bits of RGB data are transmitted at an effective rate of 595Mbps per LVDS channel. Using a 85MHz clock, the data throughput is 595Mbytes per second.

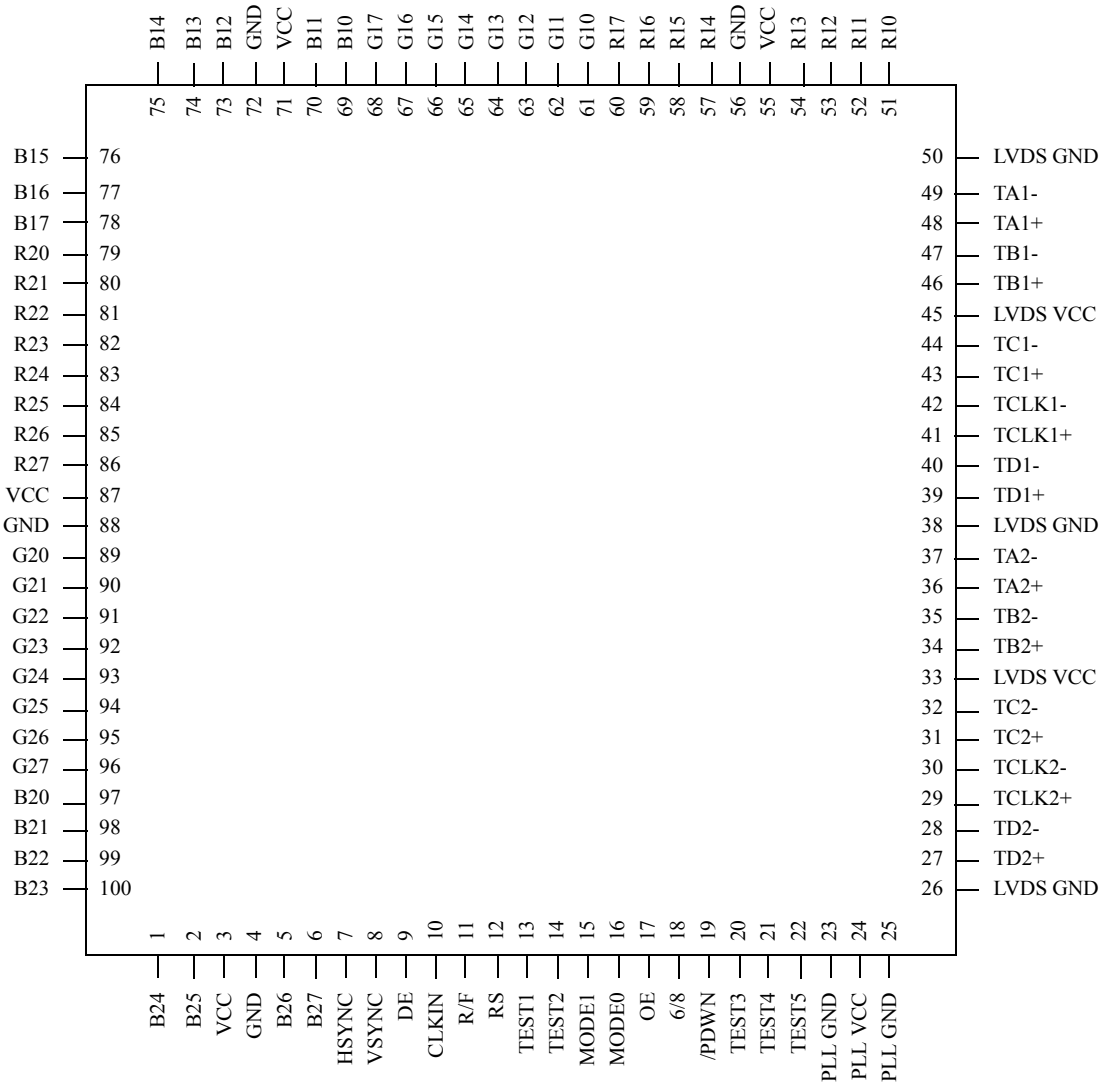
Features

- Wide dot clock range: 25-135MHz suited for VGA, SVGA, XGA, SXGA, SXGA+ and UXGA
- PLL requires No external components
- Supports Dual Link, Dual-in (TTL)/Dual-out (LVDS) pixel up to 170MHz dot clock for UXGA
- Supports Single Link, Dual-in (TTL)/Single-out (LVDS) pixel up to 135MHz dot clock for SXGA+
- Supports Single Link, Single-in (TTL)/Single-out (LVDS) pixel up to 85MHz dot clock for XGA
- Clock edge selectable
- Supports Reduced swing LVDS for Low EMI
- Power down mode
- Low power single 3.3V CMOS design
- 100pin TQFP
- THC63LVDM83R compatible

Block Diagram



Pin Out


B14 75
B13 74
B12 73
GND 72
VCC 71
B11 70
B10 69
G17 68
G16 67
G15 66
G14 65
G13 64
G12 63
G11 62
G10 61
R17 60
R16 59
R15 58
R14 57
GND 56
VCC 55
R13 54
R12 53
R11 52
R10 51
B15 76
B16 77
B17 78
R20 79
R21 80
R22 81
R23 82
R24 83
R25 84
R26 85
R27 86
VCC 87
GND 88
G20 89
G21 90
G22 91
G23 92
G24 93
G25 94
G26 95
G27 96
B20 97
B21 98
B22 99
B23 100
50 LVDS GND
49 TA1-
48 TA1+
47 TB1-
46 TB1+
45 LVDS VCC
44 TC1-
43 TC1+
42 TCLK1-
41 TCLK1+
40 TD1-
39 TD1+
38 LVDS GND
37 TA2-
36 TA2+
35 TB2-
34 TB2+
33 LVDS VCC
32 TC2-
31 TC2+
30 TCLK2-
29 TCLK2+
28 TD2-
27 TD2+
26 LVDS GND
1 B24
2 B25
3 VCC
4 GND
5 B26
6 B27
7 HSYNC
8 VSYNC
9 DE
10 CLKIN
11 R/F
12 RS
13 TEST1
14 TEST2
15 MODE1
16 MODE0
17 OE
18 6/8
19 /PDWN
20 TEST3
21 TEST4
22 TEST5
23 PLL GND
24 PLL VCC
25 PLL GND

Pin Description

Pin Name	Pin #	Type	Description
TA1+, TA1-	48, 49	LVDS OUT	The 1st Link. The 1st pixel output data when Dual Link.
TB1+, TB1-	46, 47	LVDS OUT	
TC1+, TC1-	43, 44	LVDS OUT	
TD1+, TD1-	39, 40	LVDS OUT	
TCLK1+, TCLK1-	41, 42	LVDS OUT	LVDS Clock Out for 1st Link.
TA2+, TA2-	36, 37	LVDS OUT	The 2nd Link. These pins are disabled when Single Link.
TB2+, TB2-	34, 35	LVDS OUT	
TC2+, TC2-	31, 32	LVDS OUT	
TD2+, TD2-	27, 28	LVDS OUT	
TCLK2+, TCLK2-	29, 30	LVDS OUT	LVDS Clock Out for 2nd Link.
R17 ~ R10	60, 59, 58, 57, 54, 53, 52, 51	IN	The 1st Pixel Data Inputs.
G17 ~ G10	68, 67, 66, 65, 64, 63, 62, 61	IN	
B17 ~ B10	78, 77, 76, 75, 74, 73, 70, 69	IN	
R27 ~ R20	86, 85, 84, 83, 82, 81, 80, 79	IN	The 2nd Pixel Data Inputs.
G27 ~ G20	96, 95, 94, 93, 92, 91, 90, 89	IN	
B27 ~ B20	6, 5, 2, 1, 100, 99, 98, 97	IN	
DE	9	IN	Data Enable Input.
VSYNC	8	IN	Vsync Input.
HSYNC	7	IN	Hsync Input.
CLKIN	10	IN	Clock Input.
TEST1, TEST5	13, 22	OUT	Test Pins.
TEST3, TEST4	20, 21	IN	Test Pins, must be L for normal operation.
TEST2	14	IN	Test Pins, must be H for normal operation.
/PDWN	19	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)
6/8	18	IN	6bit/8bit color select. H: 6bit (TDx+/- are GND), L: 8bit.
OE	17	IN	Output enable. H: Output enable, L: Output disable (all outputs are Hi-Z)
MODE1, MODE0	15, 16	IN	Pixel Data Mode.
RS	12	IN	LVDS swing range select. H: Normal range, L: Reduced range.

MODE1	MODE0	Mode
L	L	Dual Link (Dual-in/Dual-out)
L	H	Single Link (Dual-in/Single-out)
H	H	Single Link (Single-in/Single-out)

Pin Name	Pin #	Type	Description
R/F	11	IN	Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge
VCC	3, 55, 71, 87	Power	Power Supply Pins for TTL inputs, output and digital circuitry.
GND	4, 56, 72, 88	Ground	Ground Pins for TTL inputs, outputs and digital circuitry.
LVDS VCC	33, 45	Power	Power Supply Pins for LVDS Outputs.
LVDS GND	26, 38, 50	Ground	Ground Pins for LVDS Outputs.
PLL VCC	24	Power	Power Supply for PLL circuitry.
PLL GND	23, 25	Ground	Ground Pin for PLL circuitry.

Absolute Maximum Ratings [1]

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Driver Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Lead Temperature (Soldering, 4sec)	+260°C
Maximum Power Dissipation @+25°C	1.0W

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{INC}	Input Current	$0V \le V_{IN} \le V_{CC}$			±10	μA

1. "Absolute Maximum Ratings" are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

LVDS Transmitter DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
VOD	Differential Output Voltage	RL=100Ω	Normal swing	250	350	450	mV
			Reduced swing	100	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω				35	mV
VOC	Common Mode Voltage			1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states					35	mV
I_{OS}	Output Short Circuit Current	VOUT=0V, RL=100Ω				-24	mA
I_{OZ}	Output TRI-State current	/PDWN=0V, VOUT=0V to VCC				±10	μA

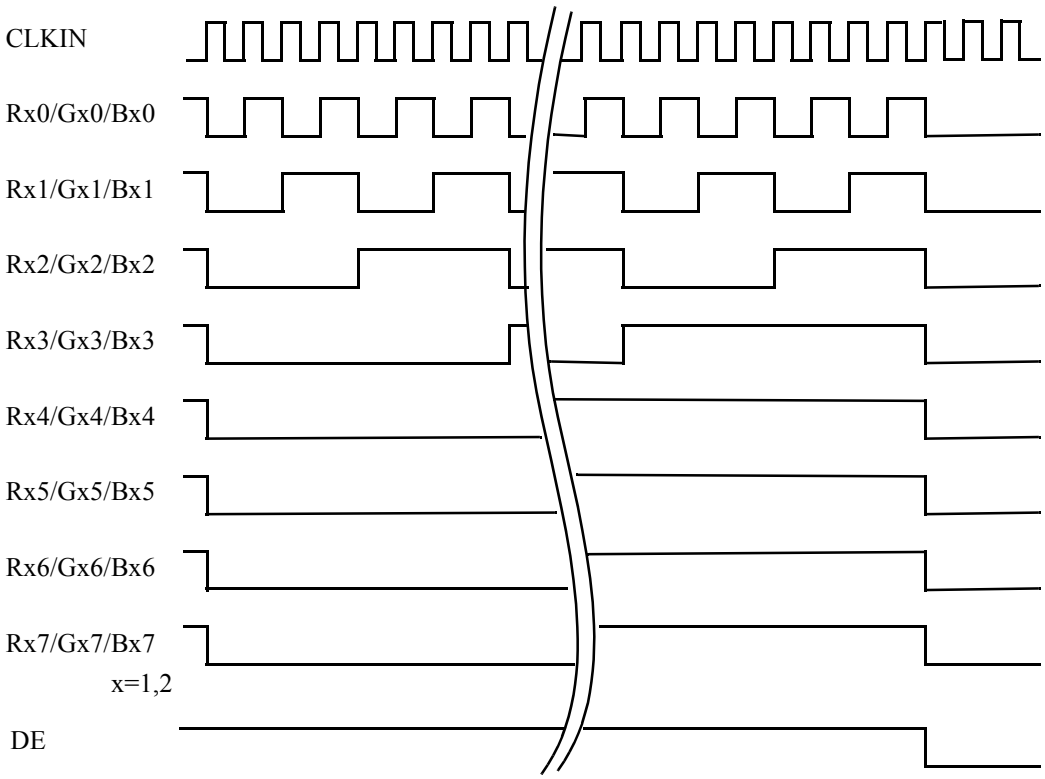
Supply Current

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

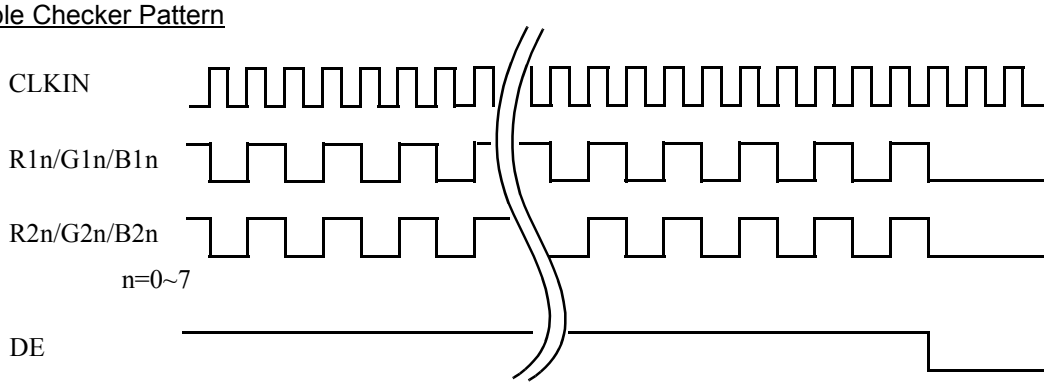
Symbol	Parameter	Condition(*)		Typ.	Max.	Units
I_{TCCG}	Transmitter Supply Current (256 Gray Scale Pattern)	VESA SXGA (60Hz) CLKIN=54MHz	MODE<1:0>=LH RL=100Ω,CL=5pF VCC=3.3V	50	58	mA
		VESA UXGA (60Hz) CLKIN=81MHz	MODE<1:0>=LL RL=100Ω,CL=5pF VCC=3.3V	78	89	mA
I_{TCCW}	Transmitter Supply Current (Double Checker Pattern)	VESA SXGA (60Hz) CLKIN=54MHz	MODE<1:0>=LH RL=100Ω,CL=5pF VCC=3.3V	53	61	mA
		VESA UXGA (60Hz) CLKIN=81MHz	MODE<1:0>=LL RL=100Ω,CL=5pF VCC=3.3	86	99	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN = L			10	μA

(*) VESA is a trademark of the Video Electronics Standards Association.

256 Gray Scale Pattern



Double Checker Pattern



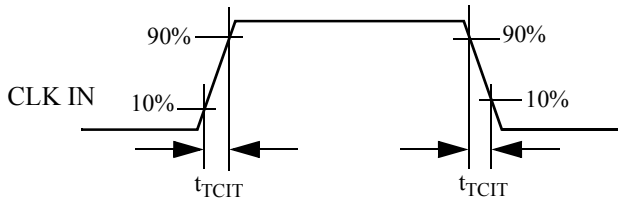
Switching Characteristics

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

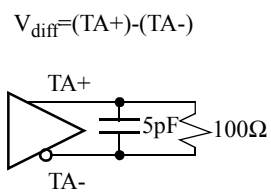
Symbol	Parameter		Min.	Typ.	Max.	Units
t_{TCIT}	CLK IN Transition time				5.0	ns
t_{TCIP}	CLK IN Period		11.76		40.0	ns
t_{TCH}	CLK IN High Time		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TCL}	CLK IN Low Time		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TS}	TTL Data Setup to CLK IN		2.5			ns
t_{TH}	TTL Data Hold from CKL IN		0.0			ns
t_{TCOP}	CLK OUT Period	Dual Link	11.76		40.0	ns
		Single Link	7.4		20.0	ns
t_{LVT}	LVDS Transition Time			0.5		ns
t_{TOP1}	Output Data Position0 (t_{TCOP} = 7.4ns)		-0.15	0.0	+0.15	ns
t_{TOP0}	Output Data Position1 (t_{TCOP} = 7.4ns)		$\frac{t_{TCOP}}{7} - 0.15$	$\frac{t_{TCOP}}{7}$	$\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP6}	Output Data Position2 (t_{TCOP} = 7.4ns)		$2\frac{t_{TCOP}}{7} - 0.15$	$2\frac{t_{TCOP}}{7}$	$2\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP5}	Output Data Position3 (t_{TCOP} = 7.4ns)		$3\frac{t_{TCOP}}{7} - 0.15$	$3\frac{t_{TCOP}}{7}$	$3\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP4}	Output Data Position4 (t_{TCOP} = 7.4ns)		$4\frac{t_{TCOP}}{7} - 0.15$	$4\frac{t_{TCOP}}{7}$	$4\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP3}	Output Data Position5 (t_{TCOP} = 7.4ns)		$5\frac{t_{TCOP}}{7} - 0.15$	$5\frac{t_{TCOP}}{7}$	$5\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP2}	Output Data Position6 (t_{TCOP} = 7.4ns)		$6\frac{t_{TCOP}}{7} - 0.15$	$6\frac{t_{TCOP}}{7}$	$6\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TPLL}	Phase Lock Loop Set				10.0	ms
t_{OE}	OE High to Data Valid		50			ns
t_{CK12}	Skew Time between TCLK1+ and TCLK2+				0.5	ns

AC Timing Diagrams

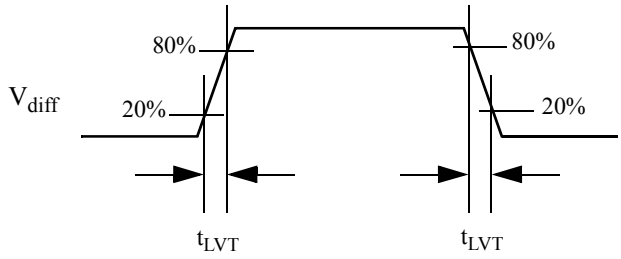
TTL Input



LVDS Output

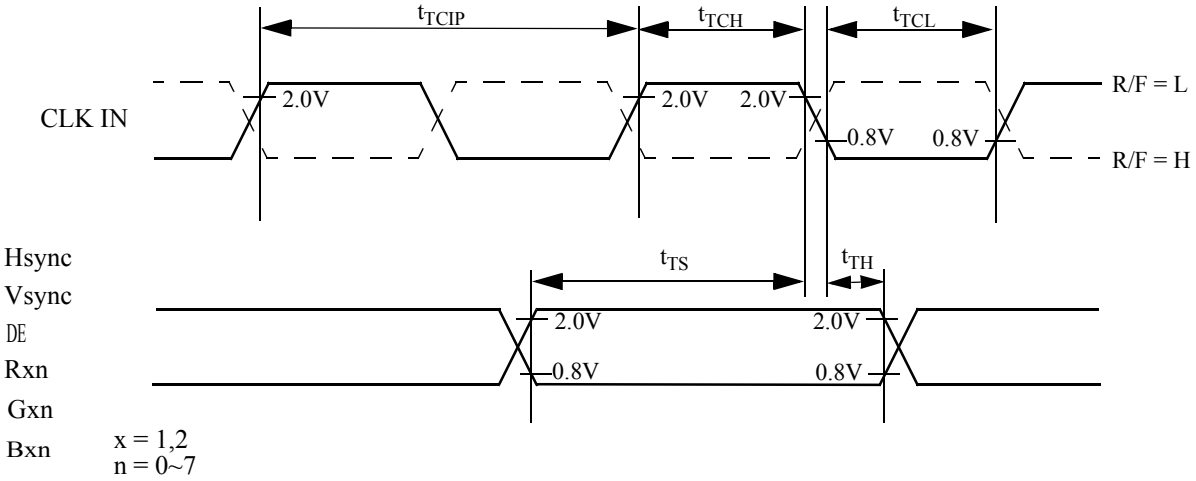


LVDS Output Load

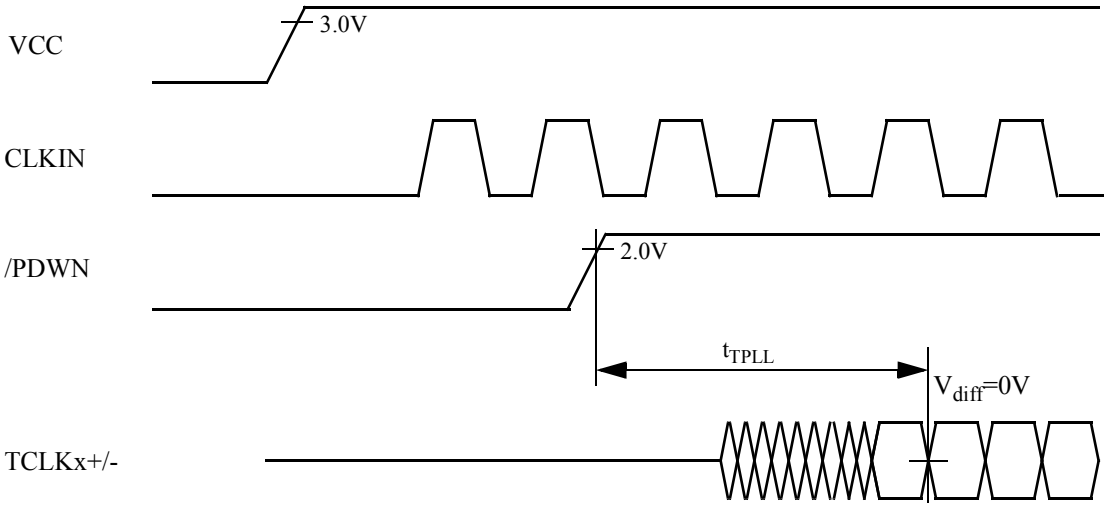


AC Timing Diagrams

TTL Inputs



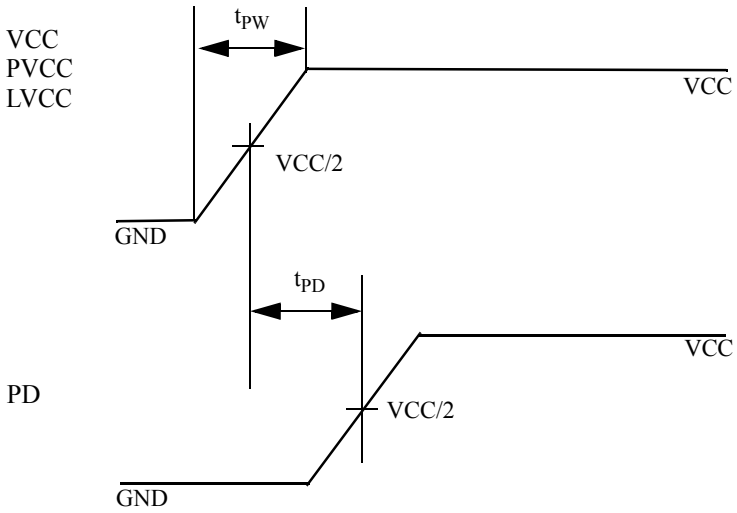
Phase Lock Loop Set Time



Power Up Sequence

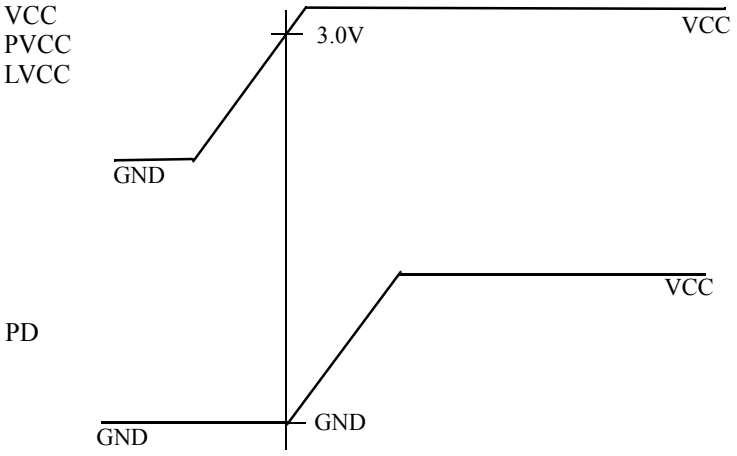
Power Up Sequence must be Sequence1 or Sequence2.

1)Sequence1



1) t_{PW} < 10msec
2) t_{PD} > t_{PW}

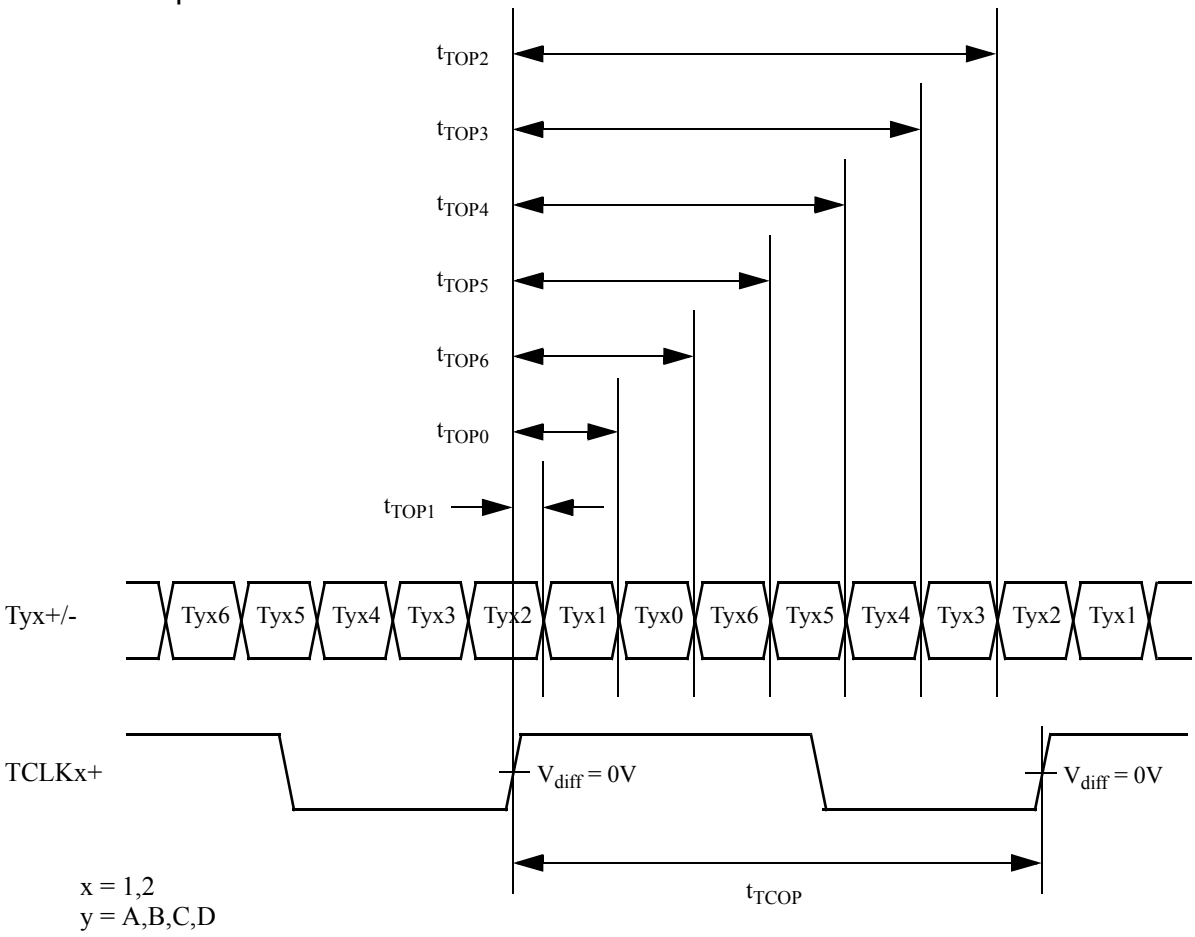
2)Sequence2

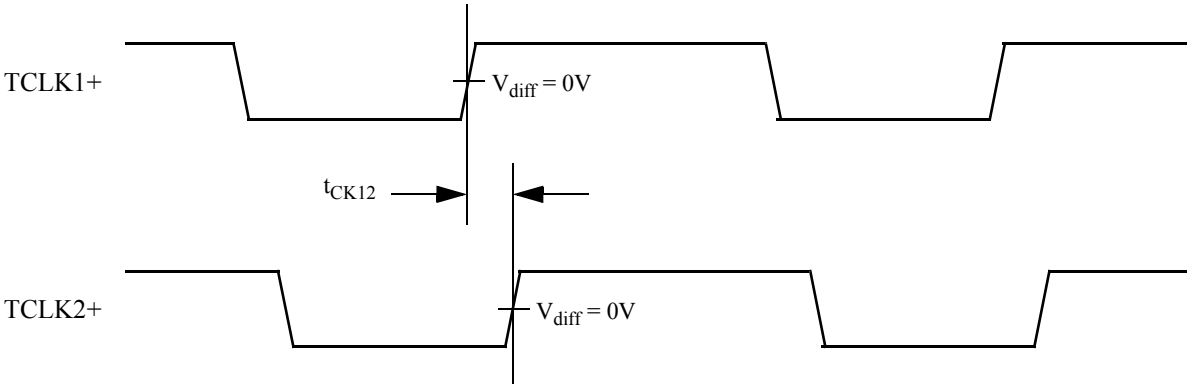


PD pin must be High after VCC voltage is 3.0V.

AC Timing Diagrams

LVDS Outputs



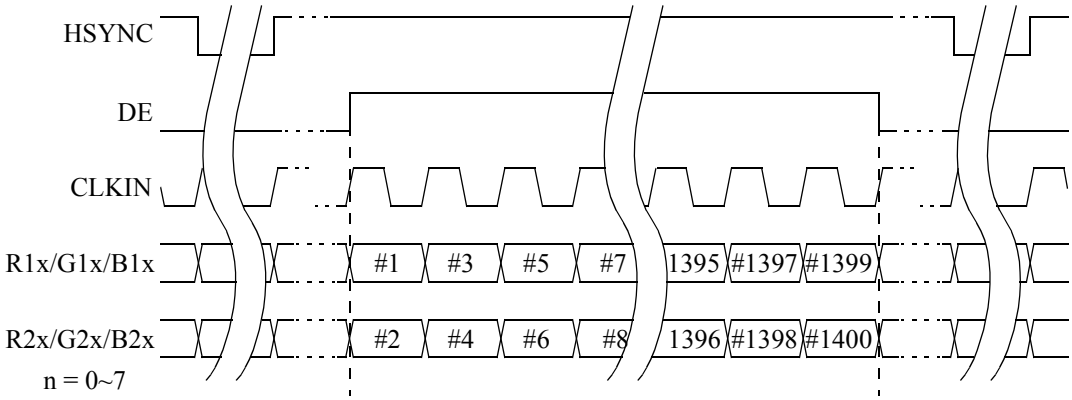


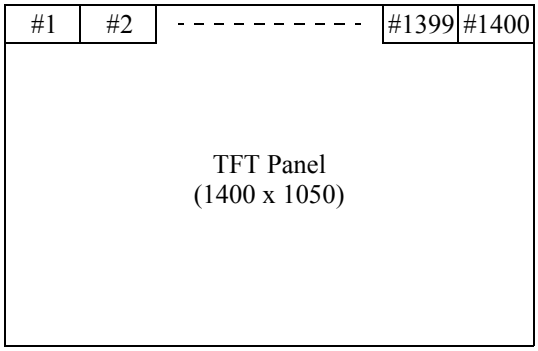
Note:
V_{diff} = (Tyx+) - (Tyx-) , (TCLKx+) - (TCLKx-)

Pixel Map Table for Single/Dual Link

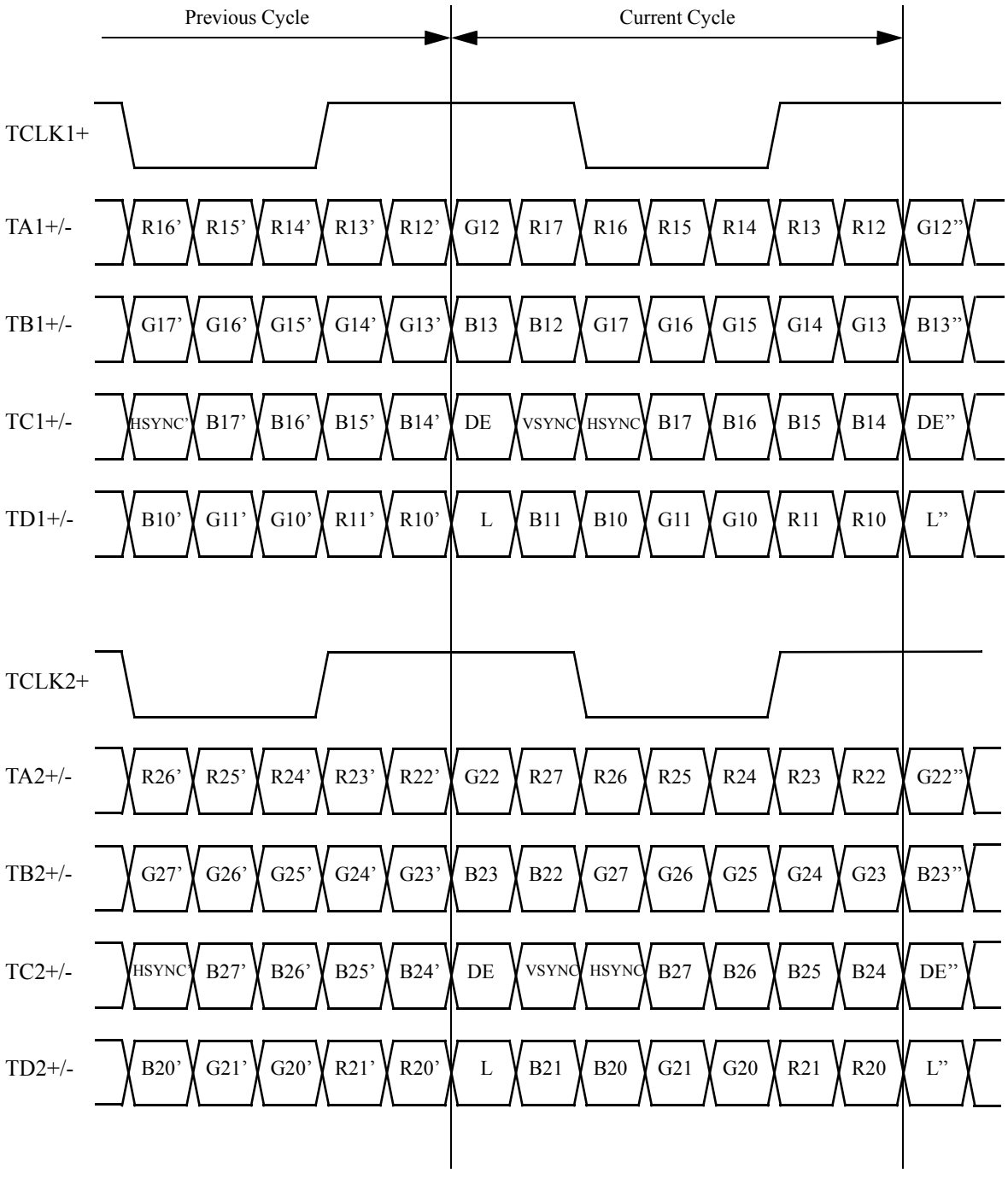
1st Pixel Data				2nd Pixel Data			
TFT Panel Data			823 TTL Input Pin	TFT Panel Data			823 TTL Input Pin
	24Bit	18Bit			24Bit	18Bit	
LSB	R10	-	R10	LSB	R20	-	R20
	R11	-	R11		R21	-	R21
	R12	R10	R12		R22	R20	R22
	R13	R11	R13		R23	R21	R23
	R14	R12	R14		R24	R22	R24
	R15	R13	R15		R25	R23	R25
	R16	R14	R16		R26	R24	R26
MSB	R17	R15	R17	MSB	R27	R25	R27
LSB	G10	-	G10	LSB	G20	-	G20
	G11	-	G11		G21	-	G21
	G12	G10	G12		G22	G20	G22
	G13	G11	G13		G23	G21	G23
	G14	G12	G14		G24	G22	G24
	G15	G13	G15		G25	G23	G25
	G16	G14	G16		G26	G24	G26
MSB	G17	G15	G17	MSB	G27	G25	G27
LSB	B10	-	B10	LSB	B20	-	B20
	B11	-	B11		B21	-	B21
	B12	B10	B12		B22	B20	B22
	B13	B11	B13		B23	B21	B23
	B14	B12	B14		B24	B22	B24
	B15	B13	B15		B25	B23	B25
	B16	B14	B16		B26	B24	B26
MSB	B17	B15	B17	MSB	B27	B25	B27

823 TTL Data Input Timing for Single/Dual Link
Example : SXGA+(1400 x 1050)

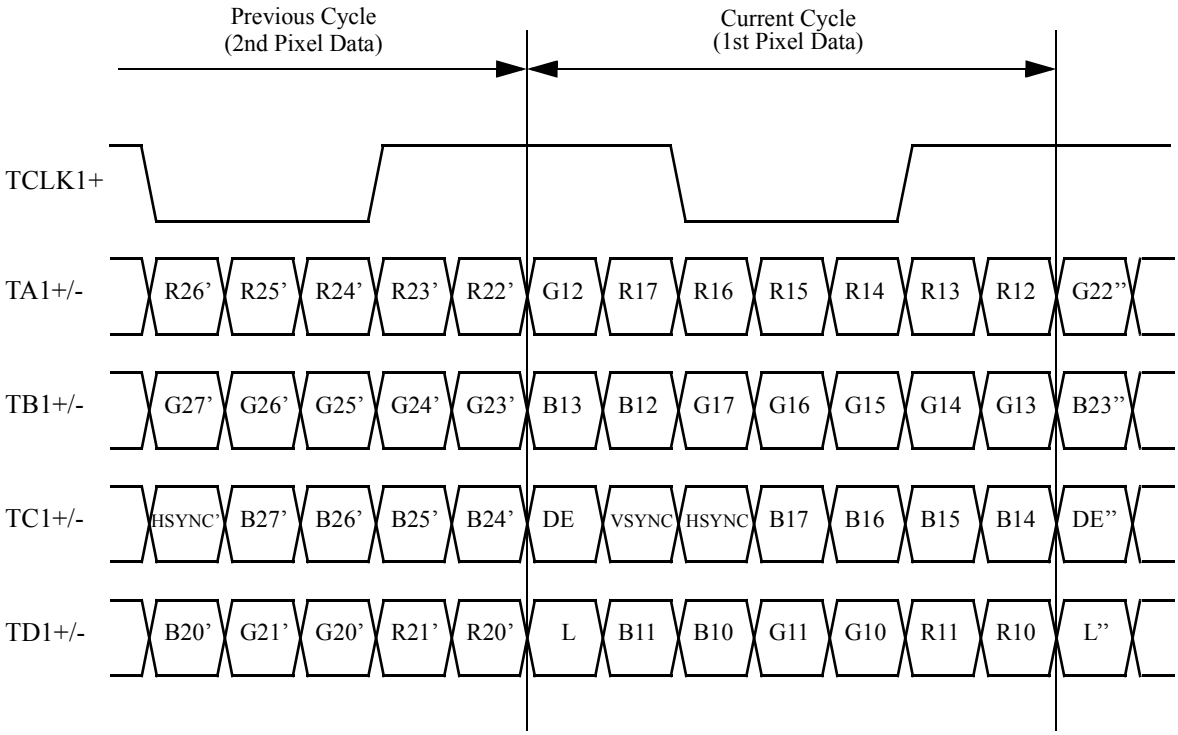




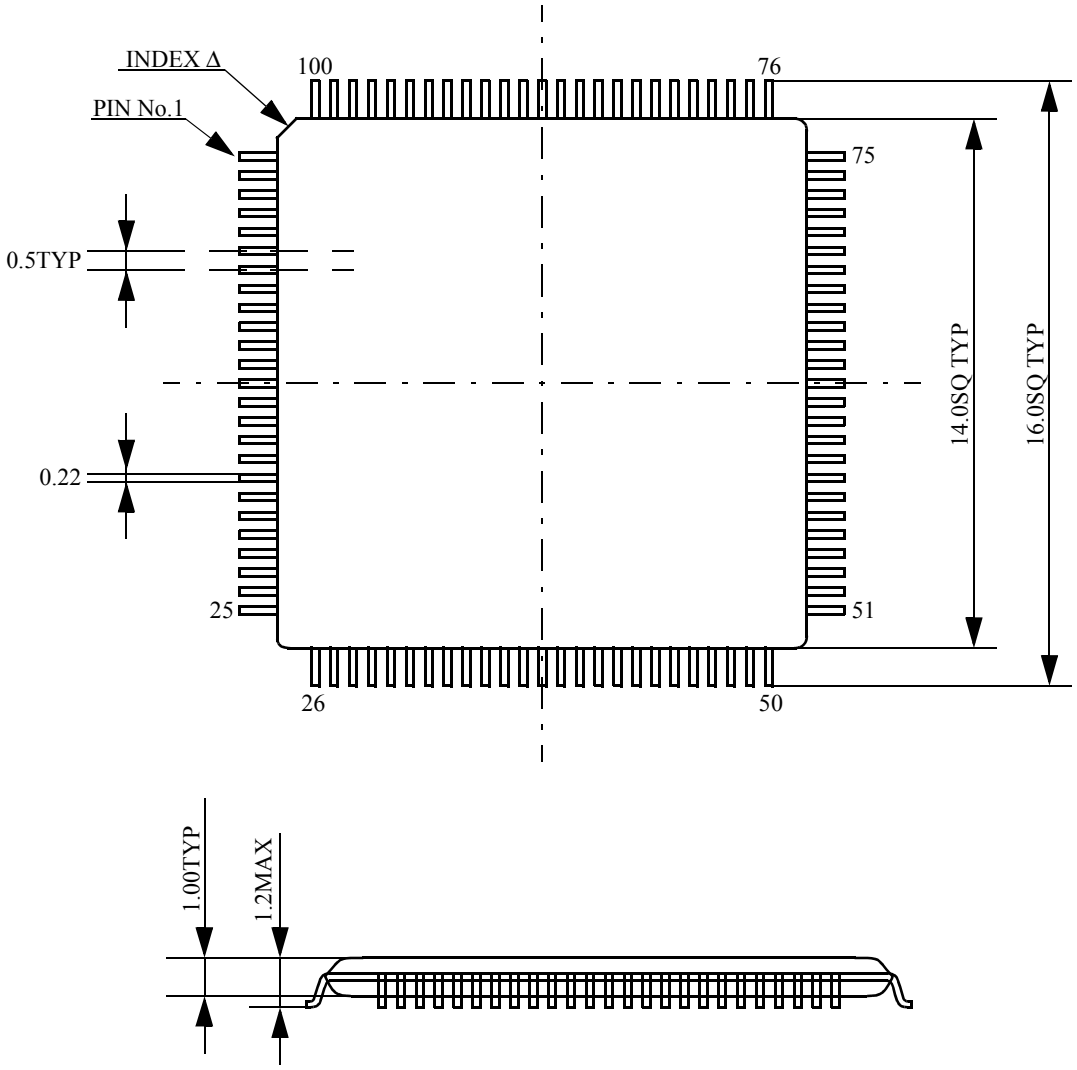
TTL Data Inputs Timing Diagrams in Dual Link
(Dual-in / Dual-out Mode)



TTL Data Inputs Timing Diagrams in Single Link (Dual-in / Single-out Mode)



Package



UNIT:mm

Notes to Users:

1. The contents of this data sheet are subject to change without prior notice.
2. Circuit diagrams shown in this data sheet are examples of application. Therefore, please pay sufficient attention when designing circuits. Even if there are incorrect descriptions, we are not responsible for any problem due to them. Please note that incorrect descriptions sometimes cannot be corrected immediately if found.
3. Our copyright and know-how are included in this data sheet. Duplication of the data sheet and disclosure to other persons are strictly prohibited without our permission.
4. We are not responsible for any problems of industrial proprietorship occurring during THC63LVD823 use, except for those directly related to THC63LVD823's structure, manufacture or functions. THC63LVD823 is designed on the premise that it should be used for ordinary electronic devices. Therefore, it shall not be used for applications that require extremely high-reliability (space equipment, nuclear control equipment, medical equipment that affects people's lives, etc.). In addition, when using THC63LVD823 for traffic signals, safety devices and control/safety units in transportation equipment, etc., appropriate measures should be taken.
5. We are making the utmost effort to improve the quality and reliability of our products. However, there is a very slight possibility of failure in semiconductor devices. To avoid damage to social or official organizations, much care should be taken to provide sufficient redundancy and fail-safe design.
6. No radiation-hardened design is incorporated in THC63LVD823.
7. Judgment on whether THC63LVD823 comes under strategic products prescribed by the Foreign Exchange and Foreign Trade Control Law is the user's responsibility.
8. This technical document was provisionally created during development of THC63LVD823, so there is a possibility of differences between it and the product's final specifications. When designing circuits using THC63LVD823, be sure to refer to the final technical documents.

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