

## LOW-NOISE, HIGH-SPEED CURRENT FEEDBACK AMPLIFIERS

### FEATURES

- **Low Noise**
  - 2.9 pA/√Hz Noninverting Current Noise
  - 10.8 pA/√Hz Inverting Current Noise
  - 2.2 nV/√Hz Voltage Noise
- **Wide Supply Voltage Range ±5 V to ±15 V**
- **Wide Output Swing**
  - 25 V<sub>PP</sub> Output Voltage, R<sub>L</sub> = 100 Ω, ±15-V Supply
- **High Output Current, 150 mA (Min)**
- **High Speed**
  - 110 MHz (–3 dB, G=1, ±15 V)
  - 1550 V/μs Slew Rate (G = 2, ±15 V)
- **Low Distortion, G = 2**
  - –78 dBc (1 MHz, 2 V<sub>PP</sub>, 100-Ω load)
- **Low Power Shutdown (THS3115)**
  - 300-μA Shutdown Quiescent Current Per Channel
- **Thermal Shutdown and Short Circuit Protection**
- **Standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ Package**
- **Evaluation Module Available**

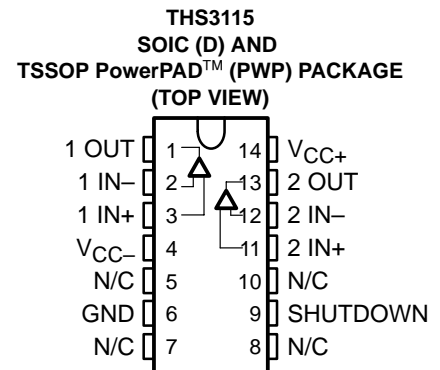
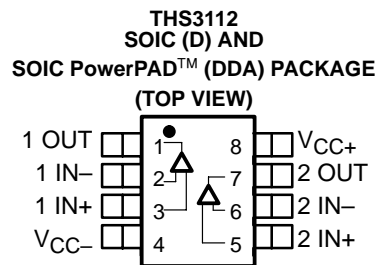
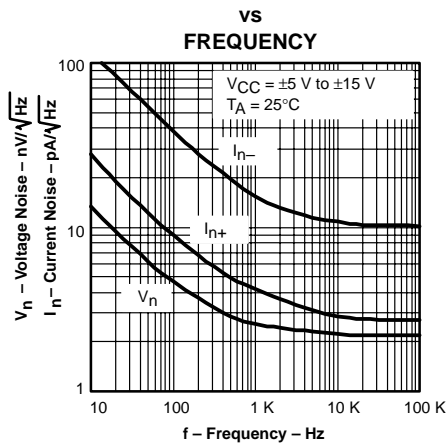
### APPLICATIONS

- **Communication Equipment**
- **Video Distribution**
- **Motor Drivers**
- **Piezo Drivers**

### DESCRIPTION

The THS3112/5 are low-noise, high-speed current feedback amplifiers, ideal for any application requiring high output current. The low noninverting current noise of 2.9 pA/√Hz and the low inverting current noise of 10.8 pA/√Hz increase signal to noise ratios for enhanced signal resolution. The THS3112/5 can operate from ±5-V to ±15-V supply voltages, while drawing as little as 4.5 mA of supply current per channel. It offers low –78-dBc total harmonic distortion driving 2 V<sub>PP</sub> into a 100-Ω load. The THS3115 features a low power shutdown mode, consuming only 300-μA shutdown quiescent current per channel. The THS3112/5 is packaged in a standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD packages.

### VOLTAGE NOISE AND CURRENT NOISE



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PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**AVAILABLE OPTIONS**

T <sub>A</sub>	PACKAGED DEVICE				EVALUATION MODULES
	SOIC-8 (D)	SOIC-8 PowerPAD (DDA)	SOIC-14 (D)	TSSOP-14 (PWP)	
0°C to 70°C	THS3112CD	THS3112CDDA	THS3115CD	THS3115CPWP	THS3112EVM
-40°C to 85°C	THS3112ID	THS3112IDDA	THS3115ID	THS3115IPWP	THS3115EVM

**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Supply voltage, V <sub>CC+</sub> to V <sub>CC-</sub>	33 V
Input voltage	± V <sub>CC</sub>
Output current (see Note 1)	275 mA
Differential input voltage	± 4 V
Maximum junction temperature	150°C
Total power dissipation at (or below) 25°C free-air temperature	See Dissipation Ratings Table
Operating free-air temperature, T <sub>A</sub> : Commercial	0°C to 70°C
Industrial	-40°C to 85°C
Storage temperature, T <sub>stg</sub> : Commercial	-65°C to 125°C
Industrial	-65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS3112 and THS3115 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

**DISSIPATION RATING TABLE**

PACKAGE	θ <sub>JA</sub>	T <sub>A</sub> = 25°C POWER RATING
D-8	95°C/W‡	1.32 W
DDA	67°C/W	1.87 W
D-14	66.6°C/W‡	1.88 W
PWP	37.5°C/W	3.3 W

‡ This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the θ<sub>JA</sub> is 168°C/W for the D-8 package and 122.3°C/W for the D-14 package.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC+</sub> to V <sub>CC-</sub>	Dual supply	±5		±15	V
	Single supply	10		30	
Operating free-air temperature, T <sub>A</sub>	C-suffix	0		70	°C
	I-suffix	-40		85	
Shutdown pin input levels, relative to the GND pin	High level (device shutdown)	2			V
	Low level (device active)			0.8	

electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  
 $V_{CC} = \pm 15\text{ V}$ ,  $R_F = 750\ \Omega$ ,  $R_L = 100\ \Omega$  (unless otherwise noted)

**dynamic performance**

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (-3 dB)	$R_L = 100\ \Omega$	$R_F = 1\ \text{k}\Omega$ , $G = 1$	$V_{CC} = \pm 5\text{ V}$	95		MHz	
				$V_{CC} = \pm 15\text{ V}$	110			
		$R_L = 100\ \Omega$	$R_F = 750\ \Omega$ , $G = 2$	$V_{CC} = \pm 5\text{ V}$	103			
				$V_{CC} = \pm 15\text{ V}$	110			
	Bandwidth (0.1 dB)		$R_F = 750\ \Omega$ , $G = 2$	$V_{CC} = \pm 5\text{ V}$	25			
				$V_{CC} = \pm 15\text{ V}$	48			
SR	Slew rate (see Note 2), $G=8$	$G = 2$ $R_F = 680\ \Omega$	$V_O = 10\text{ V}_{PP}$	$V_{CC} = \pm 15\text{ V}$	1550		$\text{V}/\mu\text{s}$	
			$V_O = 5\text{ V}_{PP}$	$V_{CC} = \pm 5\text{ V}$	820			
				$V_{CC} = \pm 15\text{ V}$	1300			
$t_s$	Settling time to 0.1%	$G = -1$	$V_O = 2\text{ V}_{PP}$	$V_{CC} = \pm 5\text{ V}$	50		ns	
			$V_O = 5\text{ V}_{PP}$	$V_{CC} = \pm 15\text{ V}$	63			

NOTE 2: Slew rate is defined from the 25% to the 75% output levels.

**noise/distortion performance**

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	$G = 2$ , $R_F = 680\ \Omega$ , $V_{CC} = \pm 15\text{ V}$ , $f = 1\ \text{MHz}$	$V_O(PP) = 2\text{ V}$	-78		dBc		
			$V_O(PP) = 8\text{ V}$	-75				
		$G = 2$ , $R_F = 680\ \Omega$ , $V_{CC} = \pm 5\text{ V}$ , $f = 1\ \text{MHz}$	$V_O(PP) = 2\text{ V}$	-76				
			$V_O(PP) = 6\text{ V}$	-74				
$V_n$	Input voltage noise	$V_{CC} = \pm 5\text{ V}, \pm 15\text{ V}$		$f = 10\ \text{kHz}$	2.2		$\text{nV}/\sqrt{\text{Hz}}$	
$I_n$	Input current noise	Noninverting Input	$V_{CC} = \pm 5\text{ V}, \pm 15\text{ V}$		$f = 10\ \text{kHz}$	2.9		$\text{pA}/\sqrt{\text{Hz}}$
		Inverting Input				10.8		
Crosstalk		$G = 2$ , $f = 1\ \text{MHz}$ , $V_O = 2\text{ V}_{pp}$	$V_{CC} = \pm 5\text{ V}$	-67		dBc		
			$V_{CC} = \pm 15\text{ V}$	-67				
Differential gain error		$G = 2$ , $R_L = 150\ \Omega$ , 40 IRE modulation	$V_{CC} = \pm 5\text{ V}$	0.01%				
			$V_{CC} = \pm 15\text{ V}$	0.01%				
Differential phase error		$\pm 100\ \text{IRE Ramp}$ NTSC and PAL	$V_{CC} = \pm 5\text{ V}$	0.011°				
			$V_{CC} = \pm 15\text{ V}$	0.011°				

electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{ V}$ ,  $R_F = 750\ \Omega$ ,  $R_L = 100\ \Omega$  (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{CC} = \pm 5\text{ V}$ , $V_{CC} = \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$		3	8	mV
			$T_A = \text{full range}$			13	
	Channel offset voltage matching		$T_A = 25^\circ\text{C}$		1	3	
			$T_A = \text{full range}$			4	
	Offset drift		$T_A = \text{full range}$		10		$\mu\text{V}/^\circ\text{C}$
$I_{IB}$	– Input bias current	$V_{CC} = \pm 5\text{ V}$ , $V_{CC} = \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$			23	$\mu\text{A}$
			$T_A = \text{full range}$			30	
	+ Input bias current		$T_A = 25^\circ\text{C}$		0.33	2	
			$T_A = \text{full range}$			3	
	Input offset current		$T_A = 25^\circ\text{C}$		4	22	
$T_A = \text{full range}$				30			
$Z_{OL}$	Open loop transimpedance	$V_{CC} = \pm 5\text{ V}$ , $V_{CC} = \pm 15\text{ V}$	$R_L = 1\text{ k}\Omega$ ,		1		$\text{M}\Omega$

input characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{ICR}$	Input common-mode voltage range	$V_{CC} = \pm 5\text{ V}$	$T_A = \text{full range}$	$\pm 2.5$	$\pm 2.7$		V
		$V_{CC} = \pm 15\text{ V}$		$\pm 12.5$	$\pm 12.7$		
$\text{CMRR}$	Common-mode rejection ratio	$V_{CC} = \pm 5\text{ V}$ , $V_I = -2.5\text{ V to } 2.5\text{ V}$	$T_A = 25^\circ\text{C}$	56	62		dB
			$T_A = \text{full range}$	54			
		$V_{CC} = \pm 15\text{ V}$ , $V_I = -12.5\text{ V to } 12.5\text{ V}$	$T_A = 25^\circ\text{C}$	63	67		
			$T_A = \text{full range}$	60			
$R_I$	Input resistance	+ Input			1.5		$\text{M}\Omega$
		– Input			15		$\Omega$
$C_i$	Input capacitance				2		pF

output characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_O$	Output voltage swing	$G = 4$ , $V_I = 1\text{ V}$ , $V_{CC} = \pm 5\text{ V}$	$R_L = 1\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$		3.9		V
			$R_L = 100\ \Omega$ ,	$T_A = 25^\circ\text{C}$	3.6	3.8	
				$T_A = \text{full range}$	3.4		
		$G = 4$ , $V_I = 3.4\text{ V}$ , $V_{CC} = \pm 15\text{ V}$	$R_L = 1\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$		13.5		
			$R_L = 100\ \Omega$ ,	$T_A = 25^\circ\text{C}$	12.2	13.3	
				$T_A = \text{full range}$	12		
$I_O$	Output current drive	$G = 4$ , $V_I = 1.025\text{ V}$ , $V_{CC} = \pm 5\text{ V}$	$R_L = 25\ \Omega$ ,	$T_A = 25^\circ\text{C}$	100	130	mA
		$G = 4$ , $V_I = 3.4\text{ V}$ , $V_{CC} = \pm 15\text{ V}$	$R_L = 25\ \Omega$ ,		175	270	
$r_o$	Output resistance	open loop			14		$\Omega$

electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{ V}$ ,  $R_F = 750\ \Omega$ ,  $R_L = 100\ \Omega$ ,  $GND = 0\text{ V}$  (unless otherwise noted) (continued)

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{CC}$	Quiescent current (per amplifier)	$V_{CC} = \pm 5\text{ V}$	$T_A = 25^\circ\text{C}$	4.4	5.5	6	mA
			$T_A = \text{full range}$				
		$V_{CC} = \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$	4.9	6.5	7.5	
			$T_A = \text{full range}$				
PSRR	Power supply rejection ratio	$V_{CC} = \pm 5\text{ V}$	$T_A = 25^\circ\text{C}$	53	60		dB
			$T_A = \text{full range}$	50			
		$V_{CC} = \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$	68	74		
			$T_A = \text{full range}$	66			

shutdown characteristics (THS3115 only)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{CC}(\text{SHDN})$	Shutdown quiescent current (per channel)	$V_{GND} = 0\text{ V}$ , $V_{CC} = \pm 5\text{ V}$ , $\pm 15\text{ V}$			0.3	0.45	mA
$t_{DIS}$	Disable time (see Note 3)	$V_{CC} = \pm 15\text{ V}$			0.1		$\mu\text{s}$
$t_{EN}$	Enable time (see Note 3)	$V_{CC} = \pm 15\text{ V}$			0.4		$\mu\text{s}$
$I_{IL}(\text{SHDN})$	Shutdown pin input bias current for power up	$V_{CC} = \pm 5\text{ V}$ , $\pm 15\text{ V}$ , $V(\text{SHDN}) = 0\text{ V}$			18	25	$\mu\text{A}$
$I_{IH}(\text{SHDN})$	Shutdown pin input bias current for power down	$V_{CC} = \pm 5\text{ V}$ , $\pm 15\text{ V}$ , $V(\text{SHDN}) = 3.3\text{ V}$			110	130	$\mu\text{A}$

NOTE 3: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Small signal closed loop gain	vs Frequency	1 – 11, 13, 14
	Gain and phase	vs Frequency	12
	Small signal closed loop noninverting gain	vs Frequency	15, 16
	Small signal closed loop inverting gain	vs Frequency	17, 18
	Small and large signal output	vs Frequency	19, 20
	Harmonic distortion	vs Frequency	21, 22
		vs Peak-to-peak output voltage	23, 24
$V_n, I_n$	Voltage noise and current noise	vs Frequency	25
CMRR	Common-mode rejection ratio	vs Frequency	26
PSRR	Power supply rejection ratio	vs Frequency	27
	Crosstalk	vs Frequency	28
$Z_o$	Output impedance	vs Frequency	29
SR	Slew rate	vs Output voltage step	30
$V_{IO}$	Input offset voltage	vs Free-air temperature	31
		vs Common-mode input voltage	32
$I_B$	Input bias current	vs Free-air temperature	33
$V_O$	Output voltage	vs Output current	34, 35
		Output voltage headroom	vs Output current
$I_{CC}$	Supply current (per channel)	vs Supply voltage	37
		Shutdown response	38

TYPICAL CHARACTERISTICS

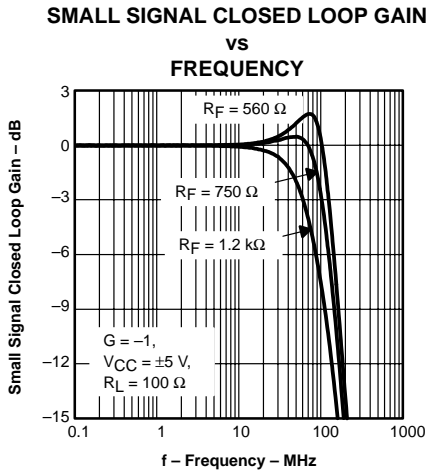


Figure 1

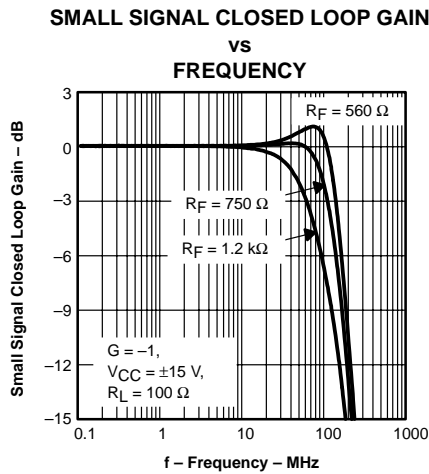


Figure 2

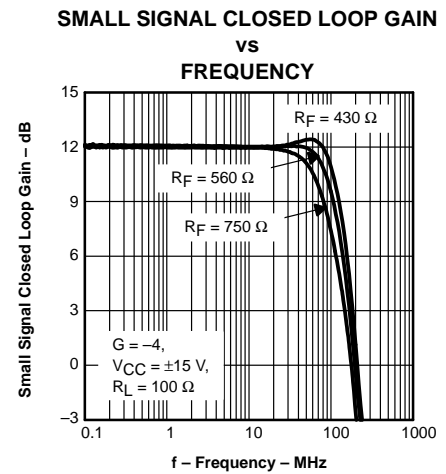


Figure 3

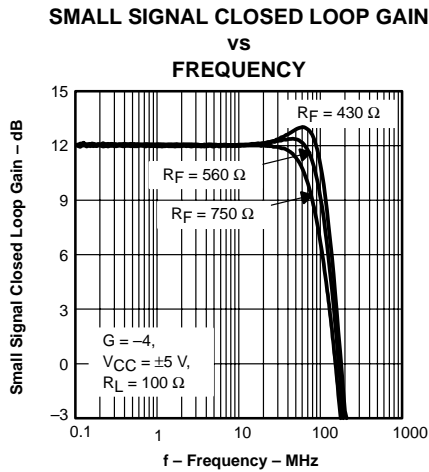


Figure 4

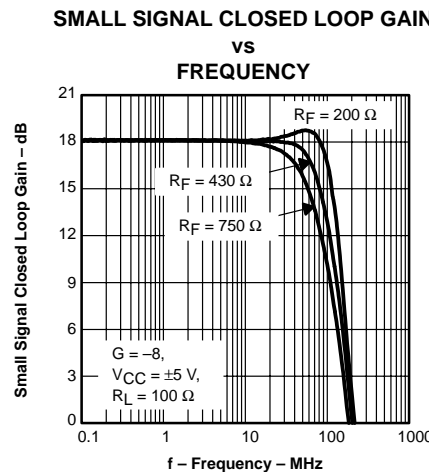


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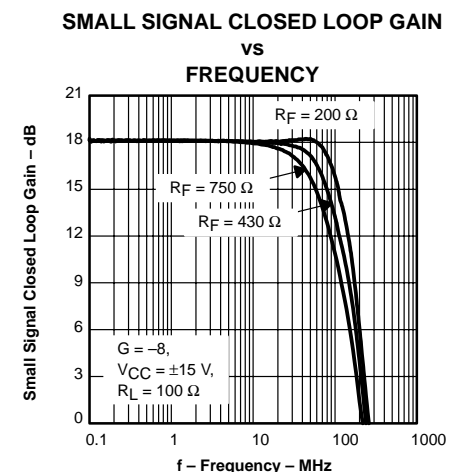


Figure 6

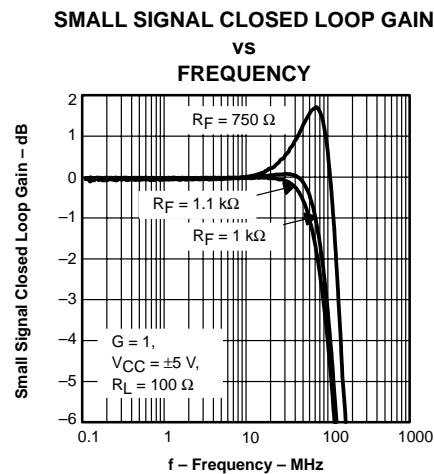


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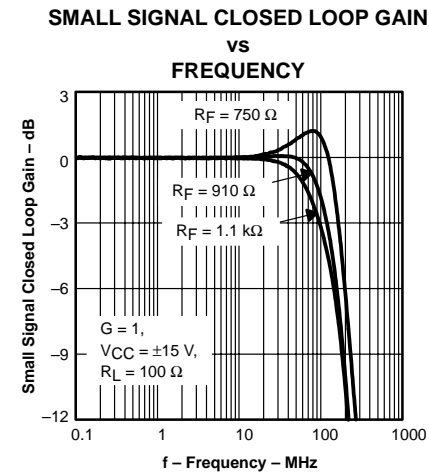


Figure 8

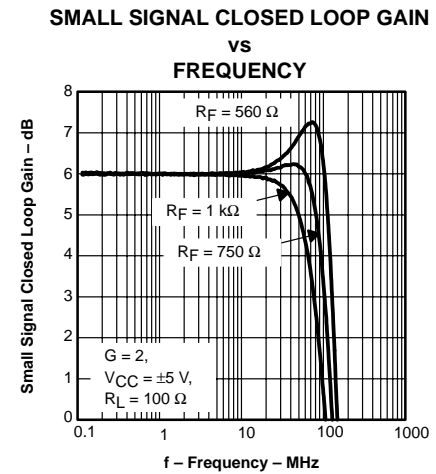


Figure 9

TYPICAL CHARACTERISTICS

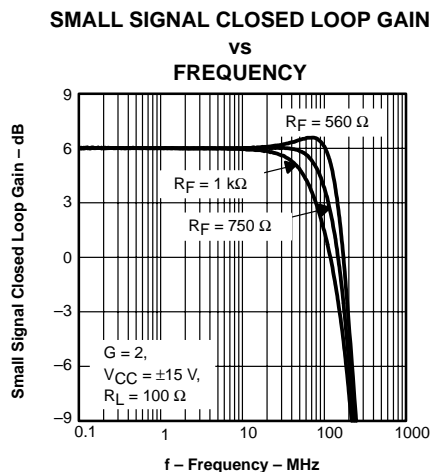


Figure 10

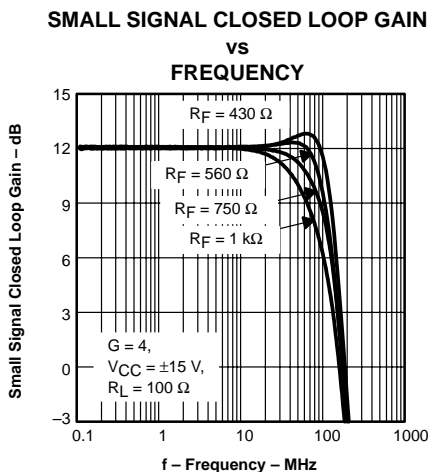


Figure 11

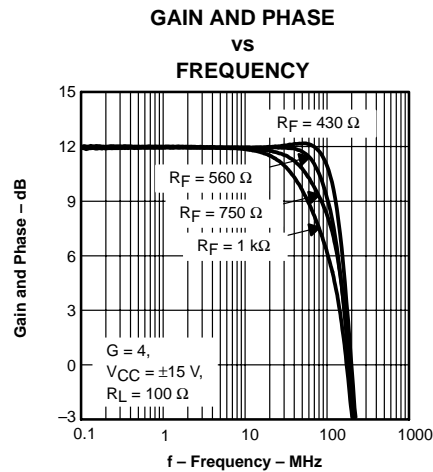


Figure 12

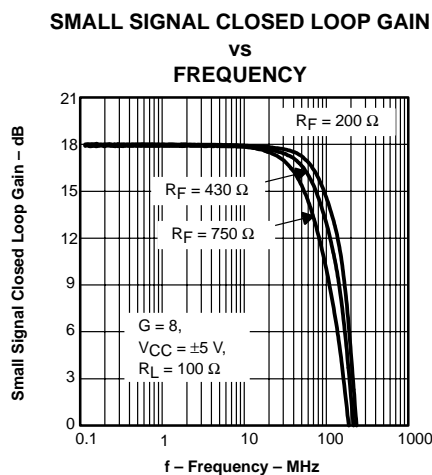


Figure 13

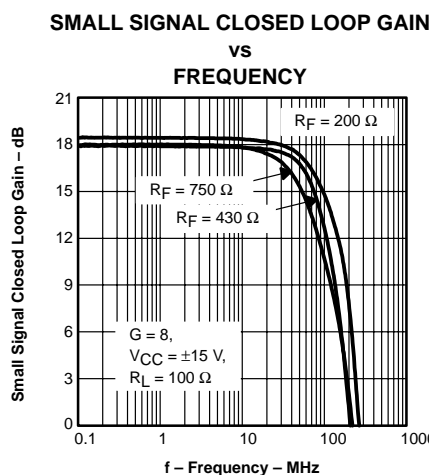


Figure 14

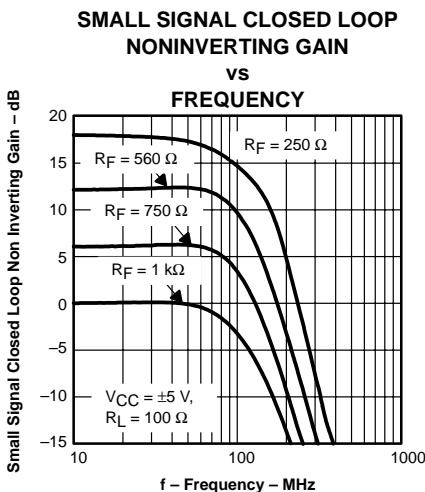


Figure 15

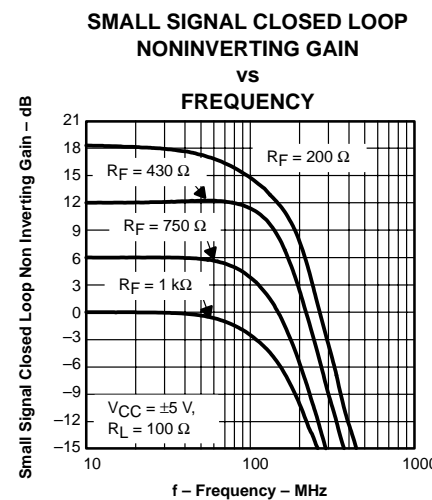


Figure 16

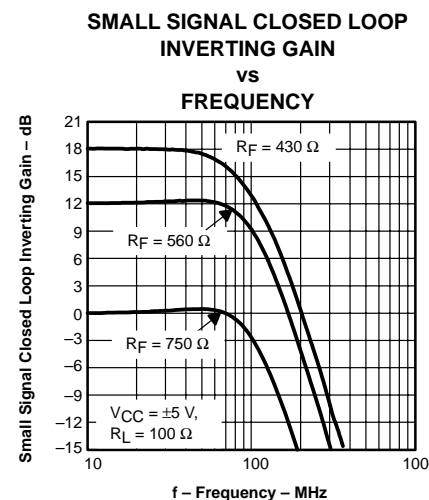


Figure 17

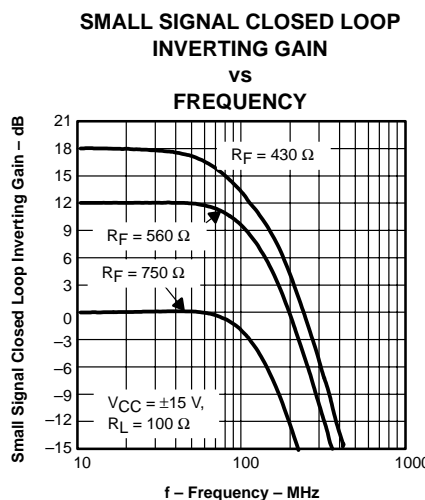


Figure 18

TYPICAL CHARACTERISTICS

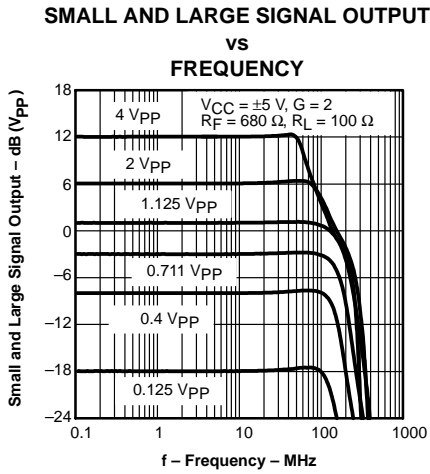


Figure 19

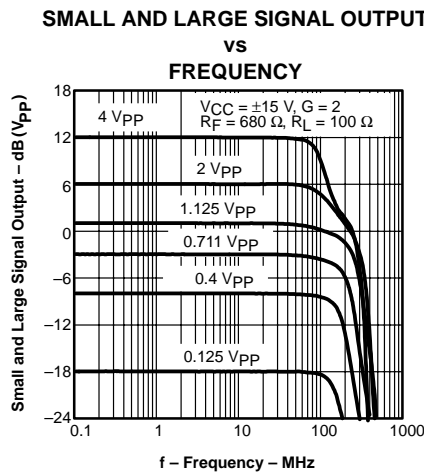


Figure 20

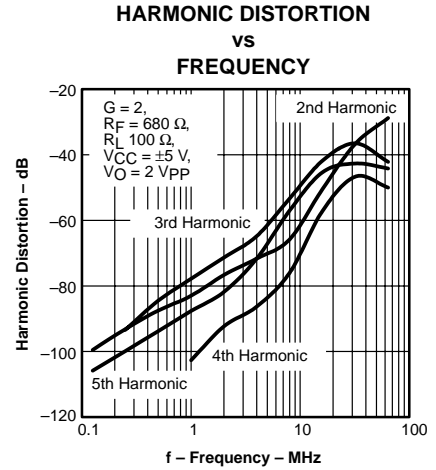


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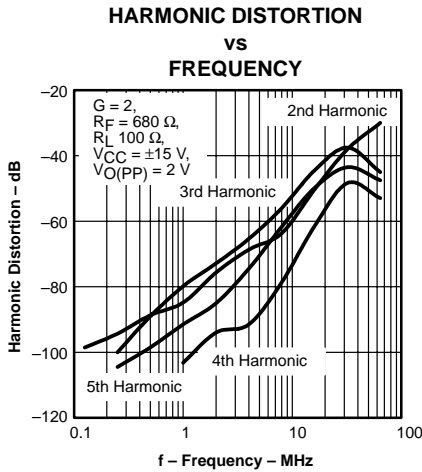


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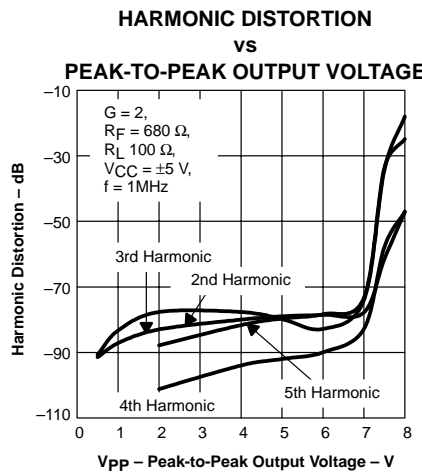


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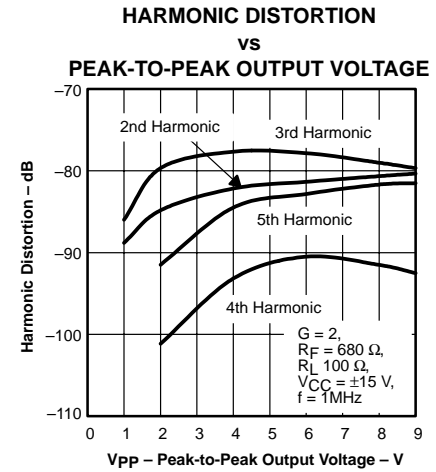


Figure 24

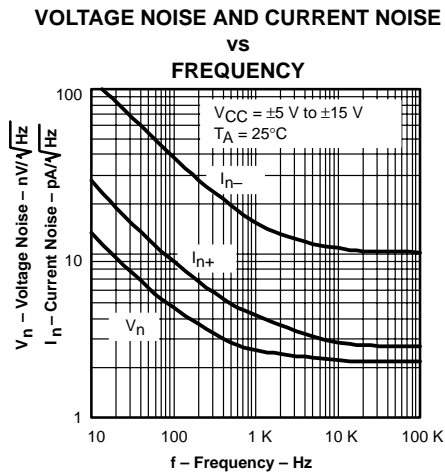


Figure 25

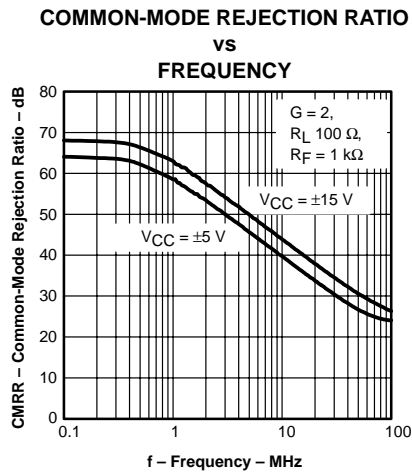


Figure 26

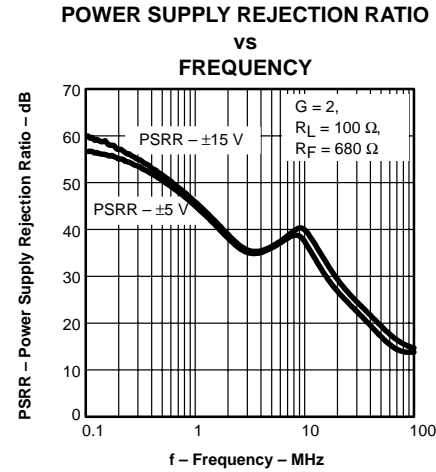


Figure 27



TYPICAL CHARACTERISTICS

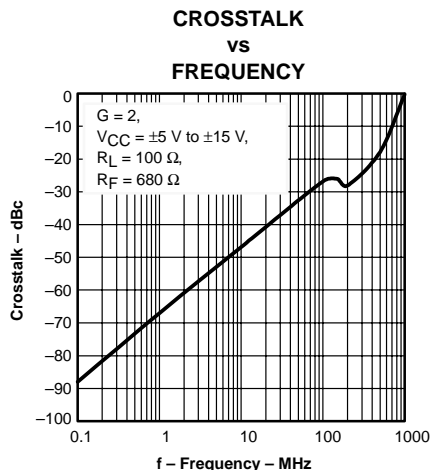


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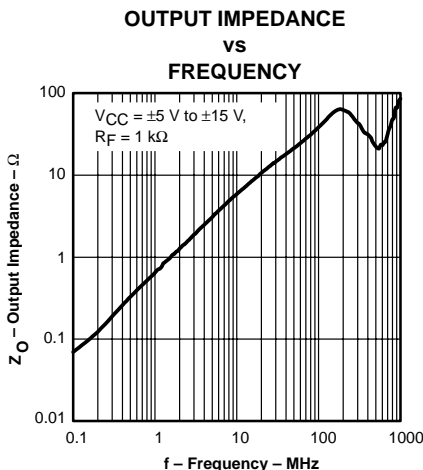


Figure 29

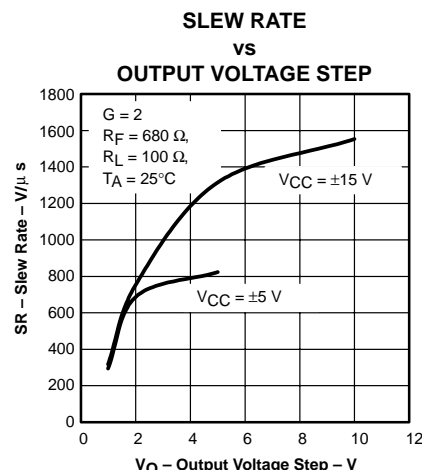


Figure 30

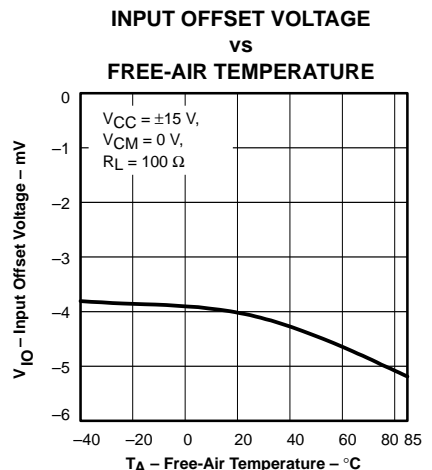


Figure 31

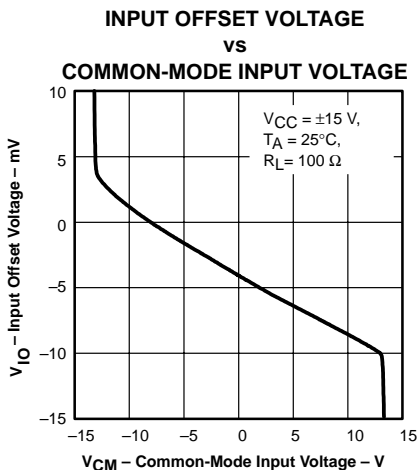


Figure 32

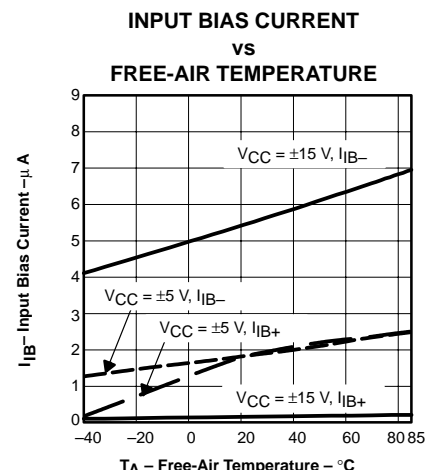


Figure 33

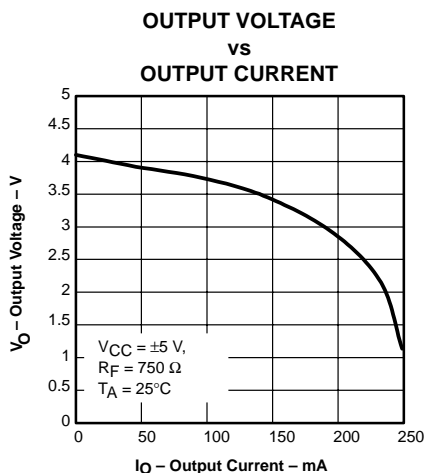


Figure 34

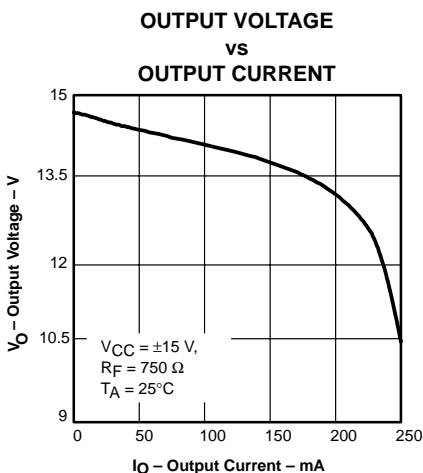


Figure 35

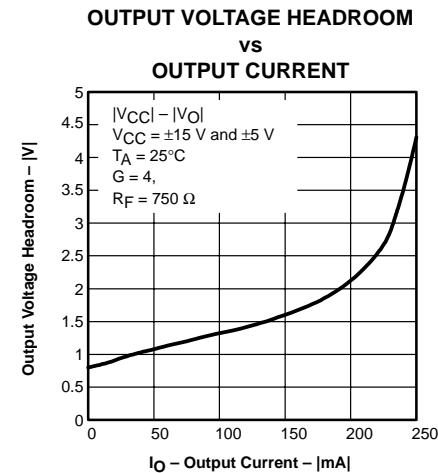


Figure 36

TYPICAL CHARACTERISTICS

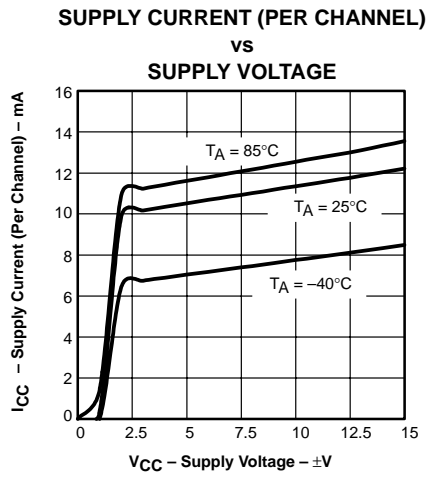


Figure 37

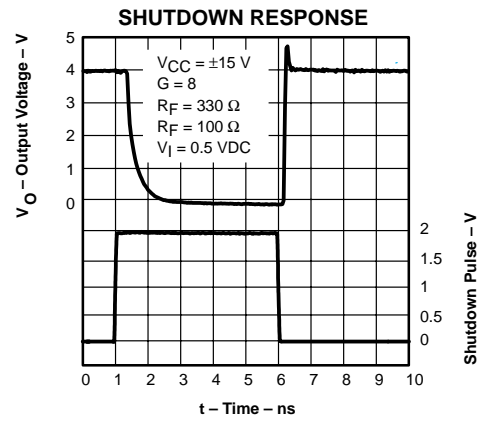


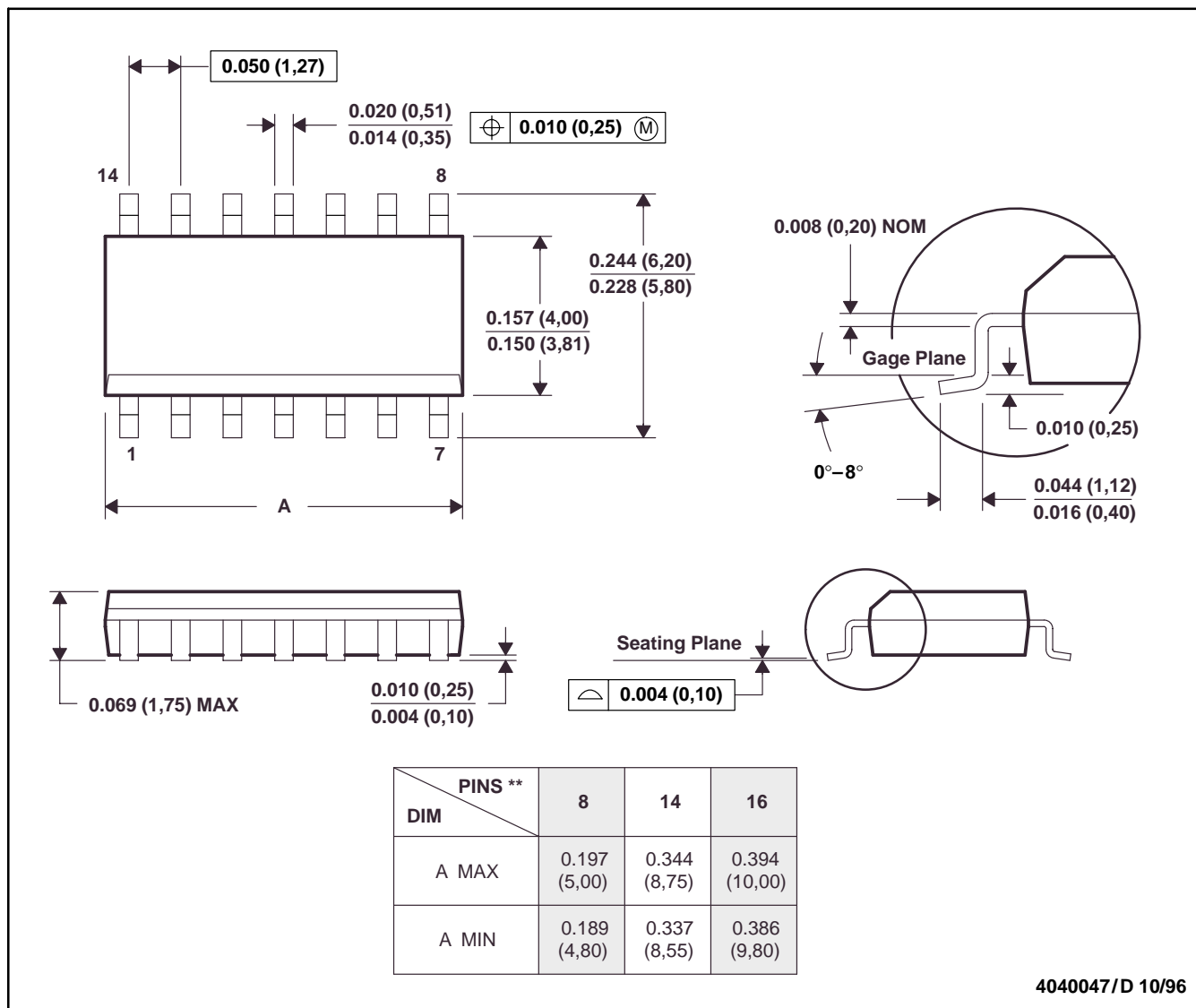
Figure 38

MECHANICAL DATA

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

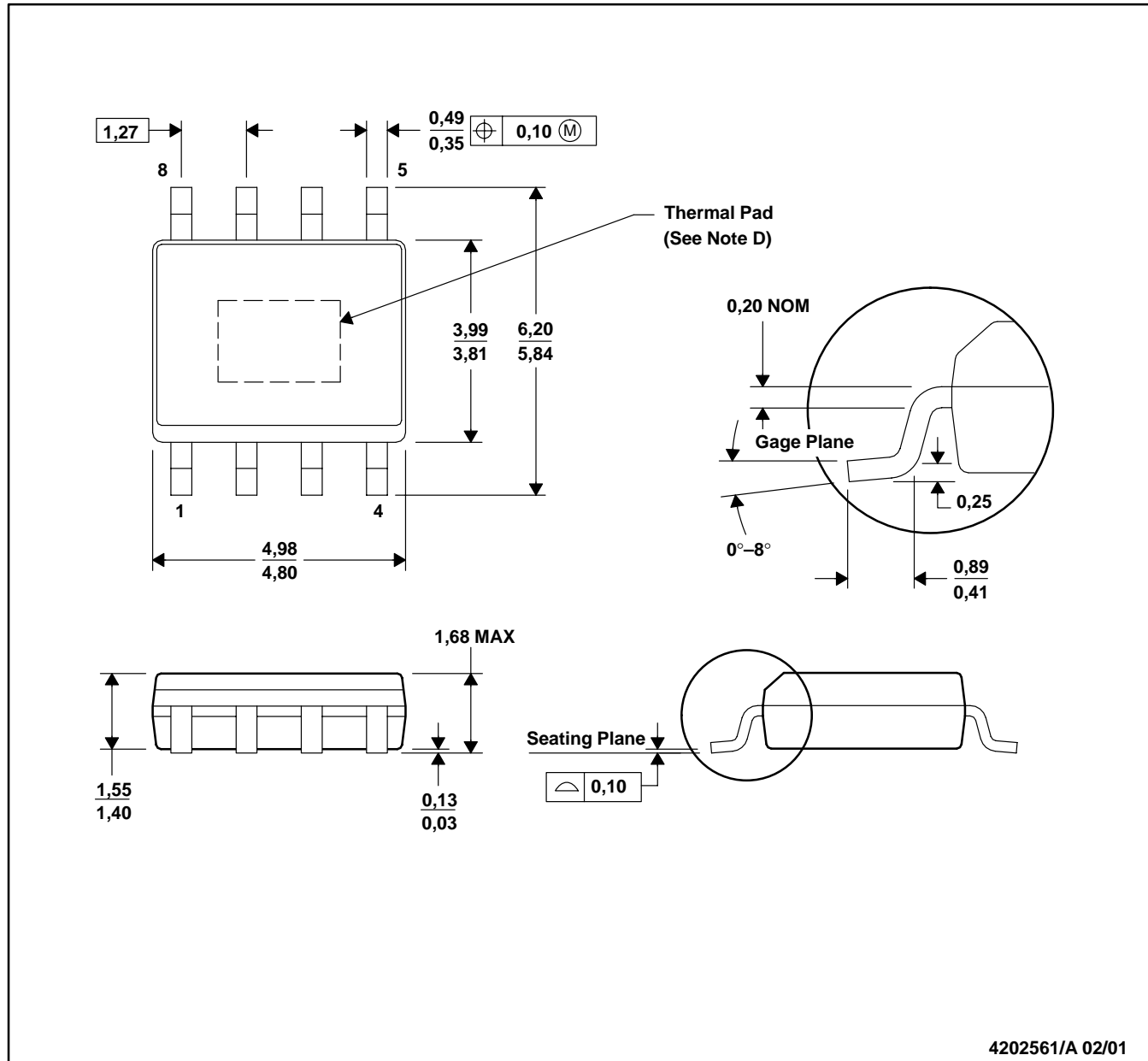


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

DDA (S-PDSO-G8)

Power PAD™ PLASTIC SMALL-OUTLINE



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.

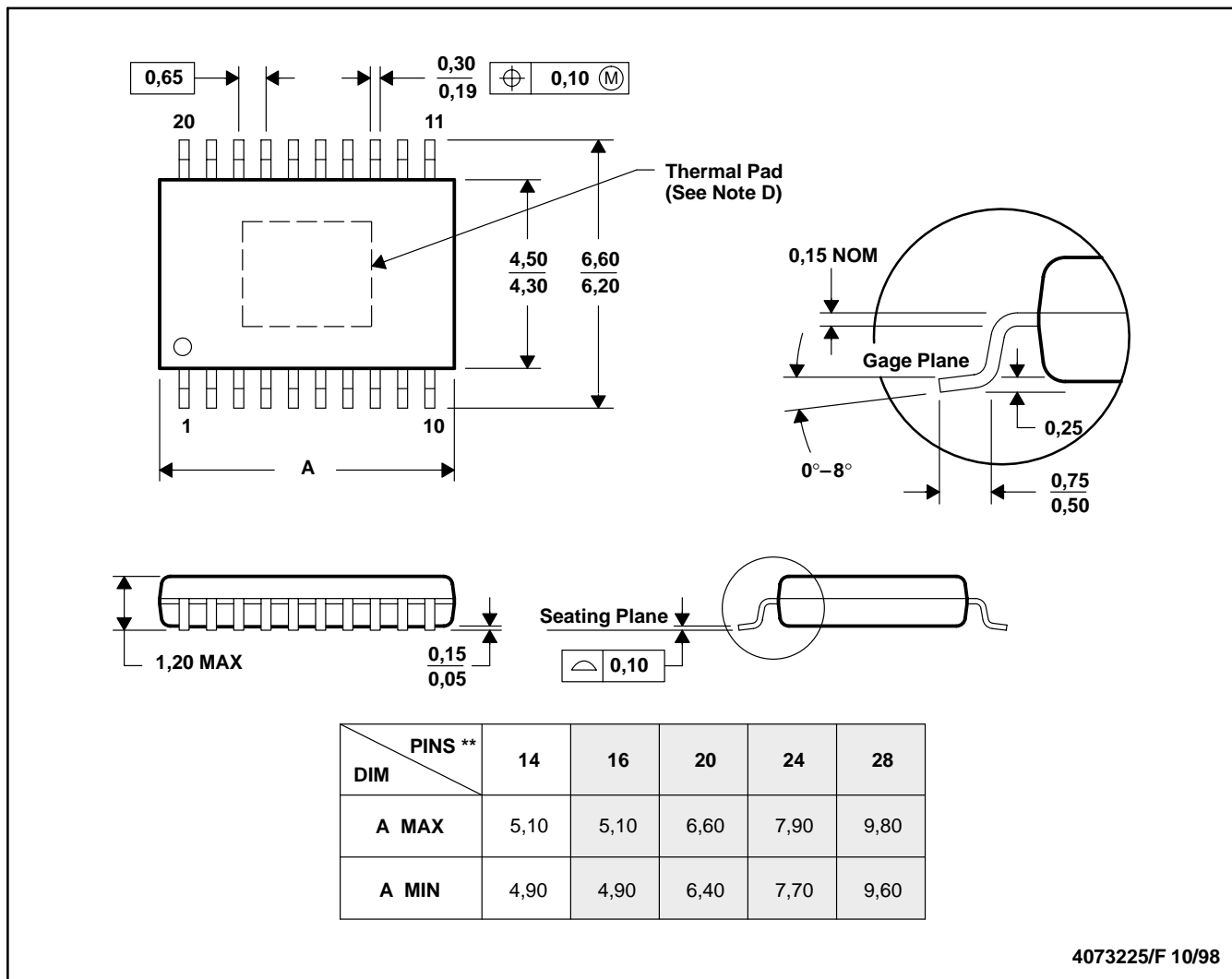
PowerPAD is a trademark of Texas Instruments.

MECHANICAL DATA

PWP (R-PDSO-G\*\*)

PowerPAD™ PLASTIC SMALL-OUTLINE

20 PINS SHOWN



4073225/F 10/98

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusions.  
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.  
 E. Falls within JEDEC MO-153

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