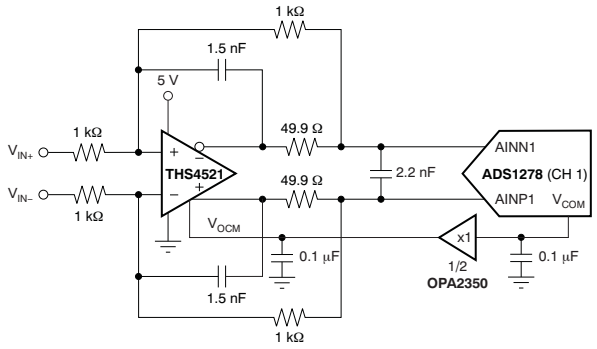
VERY LOW POWER, NEGATIVE RAIL INPUT, RAIL-TO-RAIL OUTPUT, FULLY DIFFERENTIAL AMPLIFIER

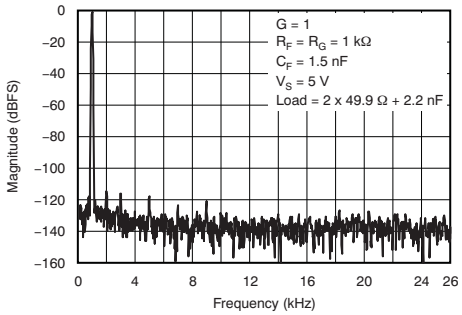
FEATURES

- **Fully Differential Architecture**
- **Bandwidth: 145 MHz**
- **Slew Rate: 490 V/μs**
- **HD_2: –133 dBc at 10 kHz (1 V_{RMS}, R_L = 1 kΩ)**
- **HD_3: –140 dBc at 10 kHz (1 V_{RMS}, R_L = 1 kΩ)**
- **Input Voltage Noise: 4.6 nV/√Hz (f = 100 kHz)**
- **NRI—Negative Rail Input**
- **RRO—Rail-to-Rail Output**
- **Output Common-Mode Control (with Low Offset and Drift)**
- **Power Supply:**
  - **Voltage: +2.5 V (±1.25 V) to +5.5 V (±2.75 V)**
  - **Current: 1.14 mA/ch**
- **Power-Down Capability: 20 μA (typ)**

THS4521 and ADS1278 Combined Performance



1-kHz FFT



Tone (Hz)	Signal (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
1 k	–0.50	109.1	–107.9	105.5	113.7

APPLICATIONS

- **Low-Power SAR and ΔΣ ADC Drivers**
- **Low-Power Differential Driver**
- **Low-Power Differential Signal Conditioning**

DESCRIPTION

The THS4521, THS4522, and THS4524 family of devices are very low-power, fully differential op amps with rail-to-rail output and an input common-mode range that includes the negative rail. These amplifiers are designed for low-power data acquisition systems and high-density applications where power dissipation is a critical parameter.

The family includes single (THS4521), dual (THS4522), and quad (THS4524) versions.

These fully differential op amps feature accurate output common-mode control that allows for dc-coupling when driving analog-to-digital converters (ADCs). This control, coupled with an input common-mode range below the negative rail as well as rail-to-rail output, allows for easy interfacing between single-ended, ground-referenced signal sources. Additionally, these devices are ideally suited for driving both successive-approximation register (SAR) and delta-sigma (ΔΣ) ADCs using only a single +3V to +5V and ground power supply.

The THS4521, THS4522, and THS4524 family of fully differential op amps is characterized for operation over the full industrial temperature range from –40°C to +85°C.

RELATED PRODUCTS

DEVICE	BW (MHz)	I_Q (mA)	THD (dBc) at 100 kHz	V_N (nV/√Hz)	RAIL-TO-RAIL
THS4520	570	15.3	–114	2	Out
THS4121	100	16	–79	5.4	In/Out
THS4130	150	16	–107	1.3	No

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
THS4521	SOIC-8	D	–40°C to +85°C	TH4521	THS4521ID	Rails, 75
					THS4521IDR	Tape and reel, 2500
	MSOP-8	DGK		4521	THS4521IDGKT	Tape and reel, 250
					THS4521IDGKR	Tape and reel, 2500
THS4522	TSSOP-16	PW	–40°C to +85°C	THS4522	THS4522IPW	Rails, 90
					THS4522IPWR	Tape and reel, 2000
THS4524	TSSOP-38	DBT	–40°C to +85°C	THS4524	THS4524IDBT	Rails, 50
					THS4524IDBTR	Tape and reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		THS4521, THS4522. THS4524	UNIT
Supply Voltage, $V_{S–}$ to V_{S+}		5.5	V
Input Voltage, V_I		$\pm V_S$	V
Differential Input Voltage, V_{ID}		1	V
Output Current, I_O		100	mA
Continuous Power Dissipation		See Thermal Characteristic Specifications	
Maximum Junction Temperature, T_J		+150	°C
Maximum Junction Temperature, T_J (continuous operation, long-term reliability)		+125	°C
Operating Free-air Temperature Range, T_A		–40 to +85	°C
Storage Temperature Range, T_{STG}		–65 to +150	°C
Lead Temperature [1,6 mm (1/16 inch) from case for 10 seconds]		300	°C
ESD Rating:	Human Body Model (HBM)	1300	V
	Charge Device Model (CDM)	1000	V
	Machine Model (MM)	50	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	THS4521, THS4522, THS4524			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
AC PERFORMANCE						
Small-Signal Bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		135		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		49		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 5		18.6		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 10		9.3		MHz	C
Gain Bandwidth Product	V_{OUT} = 100 mV_{PP}, G = 10		93		MHz	C
Large-Signal Bandwidth	V_{OUT} = 2 V_{PP}, G = 1		95		MHz	C
Bandwidth for 0.1-dB Flatness	V_{OUT} = 2 V_{PP}, G = 1		20		MHz	C
Rising Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		420		V/µs	C
Falling Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		460		V/µs	C
Overshoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		1.2		%	C
Undershoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		2.1		%	C
Rise Time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		4		ns	C
Fall Time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		3.5		ns	C
Settling Time to 1%	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		13		ns	C
Harmonic Distortion						
2nd harmonic	f = 10 kHz, V_{OUT} = 1 V_{RMS}		–133		dBc	C
	f = 1 MHz, V_{OUT} = 2 V_{PP}		–85		dBc	C
3rd harmonic	f = 10 kHz, V_{OUT} = 1 V_{RMS}		–140		dBc	C
	f = 1 MHz, V_{OUT} = 2 V_{PP}		–90		dBc	C
Second-Order Intermodulation Distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope		–83		dBc	C
Third-Order Intermodulation Distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope		–90		dBc	C
Input Voltage Noise	f > 10 kHz		4.6		nV/√Hz	C
Input Current Noise	f > 100 kHz		0.6		pA/√Hz	C
Overdrive Recovery Time	Overdrive = ±0.5 V		80		ns	C
Output Balance Error	V_{OUT} = 100 mV, f ≤ 2 MHz (differential input)		–57		dB	C
Closed-Loop Output Impedance	f = 1 MHz (differential)		0.3		Ω	C
Channel-to-Channel Crosstalk (THS4522, THS4524)	f = 10 kHz, measured differentially		–125		dB	C
DC PERFORMANCE						
Open-Loop Voltage Gain (A_{OL})		100	116		dB	A
Input-Referred Offset Voltage	T_A = +25°C		±0.2	±2	mV	A
	T_A = –40°C to +85°C		±0.5	±3.5	mV	B
Input offset voltage drift(2)	T_A = –40°C to +85°C		±2		µV/°C	C
Input Bias Current	T_A = +25°C		0.65	0.85	µA	B
	T_A = –40°C to +85°C		0.75	0.95	µA	B
Input bias current drift(2)	T_A = –40°C to +85°C		±1.75	±2	nA/°C	B
Input Offset Current	T_A = +25°C		±50	±60	pA	B
	T_A = –40°C to +85°C		±60	±70	pA	B
Input offset current drift(2)	T_A = –40°C to +85°C		±0.16	±0.25	pA/°C	B

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.

(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at –40°C and +85°C, computing the difference, and dividing by 125.

ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	THS4521, THS4522, THS4524			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
INPUT						
Common-Mode Input Voltage Low	T_A = +25°C		–0.2	–0.1	V	A
	T_A = –40°C to +85°C		–0.1	0	V	B
Common-Mode Input Voltage High	T_A = +25°C	1.9	2		V	A
	T_A = –40°C to +85°C	1.8	1.9		V	B
Common-Mode Rejection Ratio (CMRR)		80	100		dB	A
Input Resistance			110‖1.5		kΩ‖pF	C
OUTPUT						
Output Voltage Low	T_A = +25°C		0.08	0.15	V	A
	T_A = –40°C to +85°C		0.09	0.2	V	B
Output Voltage High	T_A = +25°C	3.0	3.1		V	A
	T_A = –40°C to +85°C	2.95	3.05		V	B
Output Current Drive (for linear operation)	R_L = 50 Ω		±35		mA	C
POWER SUPPLY						
Specified Operating Voltage		2.5		5.5	V	B
Quiescent Operating Current, per channel	T_A = +25°C	0.9	1.0	1.2	mA	A
	T_A = –40°C to +85°C	0.85	1.0	1.25	mA	B
Power-Supply Rejection Ratio (±PSRR)		80	100		dB	A
POWER DOWN						
Enable Voltage Threshold	Assured *on* above 2.1 V		1.6	2.1	V	A
Disable Voltage Threshold	Assured *off* below 0.7 V	0.7	1.6		V	A
Disable Pin Bias Current			1		µA	C
Power Down Quiescent Current			10		µA	C
Turn-On Time Delay	Time to V_{OUT} = 90% of final value, V_{IN}= 2 V, R_L = 200 Ω		108		ns	B
Turn-Off Time Delay	Time to V_{OUT} = 10% of original value, V_{IN}= 2 V, R_L = 200 Ω		88		ns	B
V_{OCM} VOLTAGE CONTROL						
Small-Signal Bandwidth			23		MHz	C
Slew Rate			55		V/µs	C
Gain		0.98	0.99	1.02	V/V	A
Common-Mode Offset Voltage from V_{OCM} Input	Measured at V_{OUT} with V_{OCM} input driven, V_{OCM} = 1.65 V ±0.5 V		±2.5	±4	mV	B
Input Bias Current	V_{OCM} = 1.65 V ±0.5 V		±5	±8	µA	B
V_{OCM} Voltage Range		1	0.8 to 2.5	2.3	V	A
Input Impedance			72‖1.5		kΩ‖pF	C
Default Output Common-Mode Voltage Offset from (V_{S+}– V_{S-})/2	Measured at V_{OUT} with V_{OCM} input open		±1.5	±5	mV	A
THERMAL CHARACTERISTICS						
Specified Operating Range All Packages			–40 to +85		°C	C
Thermal Resistance, θ_{JA}	Junction-to-ambient					
THS4521 D SO-8			194		°C/W	C
DGK MSOP-8			269		°C/W	C
THS4522 PW TSSOP-16			116		°C/W	C
THS4524 DBT TSSOP-38			81		°C/W	C

ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	THS4521, THS4522, THS4524			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
AC PERFORMANCE						
Small-Signal Bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		145		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		50		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 5		20		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 10		9.5		MHz	C
Gain Bandwidth Product	V_{OUT} = 100 mV_{PP}, G = 10		95		MHz	C
Large-Signal Bandwidth	V_{OUT} = 2 V_{PP}, G = 1		145		MHz	C
Bandwidth for 0.1-dB Flatness	V_{OUT} = 2 V_{PP}, G = 1		30		MHz	C
Rising Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		490		V/µs	C
Falling Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		600		V/µs	C
Overshoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		1		%	C
Undershoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		2.6		%	C
Rise Time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		3.4		ns	C
Fall Time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		3		ns	C
Settling Time to 1%	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		10		ns	C
Harmonic Distortion						
2nd harmonic	f = 10 kHz, V_{OUT} = 1 V_{RMS}		–133		dBc	C
	f = 1 MHz, V_{OUT} = 2 V_{PP}		–85		dBc	C
3rd harmonic	f = 10 kHz, V_{OUT} = 1 V_{RMS}		–140		dBc	C
	f = 1 MHz, V_{OUT} = 2 V_{PP}		–91		dBc	C
Second-Order Intermodulation Distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope		–86		dBc	C
Third-Order Intermodulation Distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope		–93		dBc	C
Input Voltage Noise	f > 10 kHz		4.6		nV/√Hz	C
Input Current Noise	f > 100 kHz		0.6		pA/√Hz	C
Overdrive Recovery Time	Overdrive = ±0.5 V		75		ns	C
Output Balance Error	V_{OUT} = 100 mV, f < 2 MHz, V_{IN} differential		–57		dB	C
Closed-Loop Output Impedance	f = 1 MHz (differential)		0.3		Ω	C
Channel-to-Channel Crosstalk (THS4522. THS4524)	f = 10 kHz, measured differentially		–125		dB	C
DC PERFORMANCE						
Open-Loop Voltage Gain (A_{OL})		100	119		dB	A
Input-Referred Offset Voltage	T_A = +25°C		±0.24	±2	mV	A
	T_A = –40°C to +85°C		±0.5	±3.5	mV	B
Input offset voltage drift(2)	T_A = –40°C to +85°C		±2		µV/°C	B
Input Bias Current	T_A = +25°C		0.7	0.9	µA	B
	T_A = –40°C to +85°C		0.9	1.1	µA	B
Input bias current drift(2)	T_A = –40°C to +85°C		±1.8	±2.2	nA/°C	B
Input Offset Current	T_A = +25°C		±50	±60	pA	B
	T_A = –40°C to +85°C		±60	±75	pA	B
Input offset current drift(2)	T_A = –40°C to +85°C		±0.16	±0.25	pA/°C	B

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.

(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at –40°C and +85°C, computing the difference, and dividing by 125.

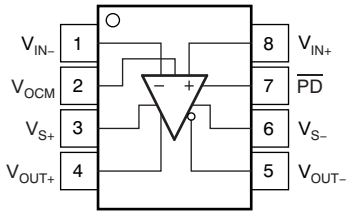
ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V (continued)

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

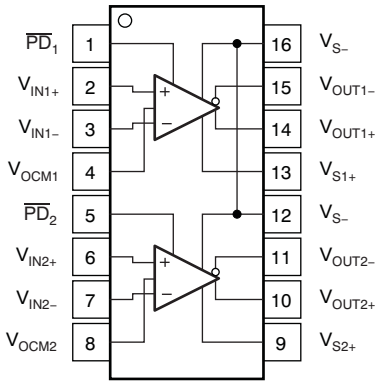
PARAMETER	CONDITIONS	THS4521, THS4522, THS4524			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
INPUT						
Common-Mode Input Voltage Low	T_A = +25°C		–0.2	–0.1	V	A
	T_A = –40°C to +85°C		–0.1	0	V	B
Common-Mode Input Voltage High	T_A = +25°C	3.6	3.7		V	A
	T_A = –40°C to +85°C	3.5	3.6		V	B
Common-Mode Rejection Ratio (CMRR)		80	102		dB	A
Input Impedance			100‖0.7		kΩ‖pF	C
OUTPUT						
Output Voltage Low	T_A = +25°C		0.10	0.15	V	A
	T_A = –40°C to +85°C		0.115	0.2	V	B
Output Voltage High	T_A = +25°C	4.7	4.75		V	A
	T_A = –40°C to +85°C	4.65	4.7		V	B
Output Current Drive (for linear operation)	R_L = 50 Ω		±55		mA	C
POWER SUPPLY						
Specified Operating Voltage		2.5		5.5	V	B
Quiescent Operating Current, per channel	T_A = +25°C	0.95	1.14	1.25	mA	A
	T_A = –40°C to +85°C	0.9	1.15	1.3	mA	B
Power-Supply Rejection Ratio (±PSRR)		80	100		dB	A
POWER DOWN						
Enable Voltage Threshold	Ensured *on* above 2.1 V		1.6	2.1	V	A
Disable Voltage Threshold	Ensured *off* below 0.7 V	0.7	1.6		V	A
Disable Pin Bias Current			1		µA	C
Power Down Quiescent Current			20		µA	C
Turn-On Time Delay	Time to V_{OUT} = 90% of final value, V_{IN}= 2 V, R_L = 200 Ω		70		ns	B
Turn-Off Time Delay	Time to V_{OUT} = 10% of original value, V_{IN}= 2 V, R_L = 200 Ω		60		ns	B
V_{OCM} VOLTAGE CONTROL						
Small-Signal Bandwidth			23		MHz	C
Slew Rate			55		V/µs	C
Gain		0.98	0.99	1.02	V/V	A
Common-Mode Offset Voltage from V_{OCM} Input	Measured at V_{OUT} with V_{OCM} input driven, V_{OCM} = 2.5V ±1 V		±5	±9	mV	B
Input Bias Current	V_{OCM} = 2.5V ±1 V		±20	±25	µA	B
V_{OCM} Voltage Range		1	0.8 to 4.2	4	V	A
Input Impedance			46‖1.5		kΩ‖pF	C
Default Output Common-Mode Voltage Offset from (V_{S+}– V_{S-})/2	Measured at V_{OUT} with V_{OCM} input open		±1	±5	mV	A
THERMAL CHARACTERISTICS						
Specified Operating Range All Packages		–40		+85	°C	C
Thermal Resistance, θ_{JA}	Junction-to-ambient					
THS4521 D SO-8			194		°C/W	C
DGK MSOP-8			269		°C/W	C
THS4522 PW TSSOP-16			116		°C/W	C
THS4524 DBT TSSOP-38			81		°C/W	C

DEVICE INFORMATION

THS4521
SOIC-8, MSOP-8 (D, DGK PACKAGES)
(TOP VIEW)



THS4522
TSSOP-16 (PW PACKAGE)
(TOP VIEW)



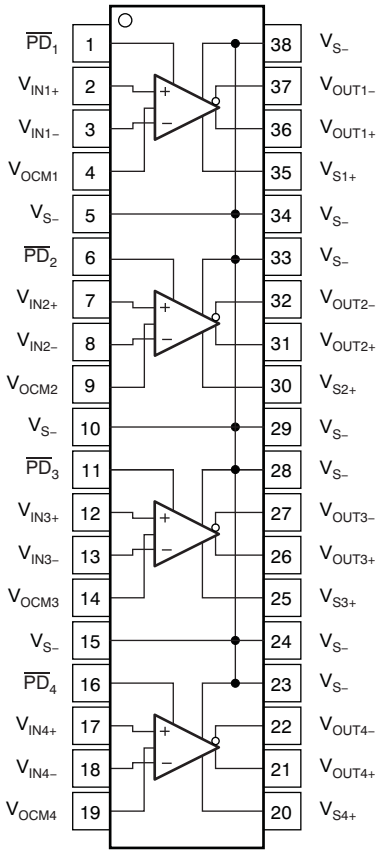
TERMINAL FUNCTIONS: THS4521

SOIC-8, MSOP-8		DESCRIPTION
PIN NO.	NAME	
1	V_{IN-}	Inverting amplifier input
2	V_{OCM}	Common-mode voltage input
3	V_{S+}	Amplifier positive power-supply input
4	V_{OUT+}	Noninverting amplifier output
5	V_{OUT-}	Inverting amplifier output
6	V_{S-}	Amplifier negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
7	$\overline{PD}$	Power down. $\overline{PD}$ = logic low puts device into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
8	V_{IN+}	Noninverting amplifier input

TERMINAL FUNCTIONS: THS4522

TSSOP-16		DESCRIPTION
PIN NO.	NAME	
1	$\overline{PD}_1$	Power down 1. $\overline{PD}$ = logic low puts device into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
2	V_{IN1+}	Noninverting amplifier 1 input
3	V_{IN1-}	Inverting amplifier 1 input
4	V_{OCM1}	Common-mode voltage input 1
5	$\overline{PD}_2$	Power down 2. $\overline{PD}$ = logic low puts device into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
6	V_{IN2+}	Noninverting amplifier 2 input
7	V_{IN2-}	Inverting amplifier 2 input
8	V_{OCM2}	Common-mode voltage input 2
9	V_{S+2}	Amplifier 2 positive power-supply input
10	V_{OUT2+}	Noninverting amplifier 2 output
11	V_{OUT2-}	Inverting amplifier 2 output
12	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
13	V_{S+1}	Amplifier 1 positive power-supply input
14	V_{OUT1+}	Noninverting amplifier 1 output
15	V_{OUT1-}	Inverting amplifier 1 output
16	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.

THS4524
TSSOP-38 (DBT PACKAGE)
(TOP VIEW)



TERMINAL FUNCTIONS: THS4524

TSSOP-38		DESCRIPTION
PIN NO.	NAME	
1	$\overline{PD}_1$	Power down 1. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
2	V_{IN1+}	Noninverting amplifier 1 input
3	V_{IN1-}	Inverting amplifier 1 input
4	V_{OCM1}	Common-mode voltage input 1
5	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
6	$\overline{PD}_2$	Power down 2. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
7	V_{IN2+}	Noninverting amplifier 2 input
8	V_{IN2-}	Inverting amplifier 2 input
9	V_{OCM2}	Common-mode voltage input 2
10	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
11	$\overline{PD}_3$	Power down 3. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
12	V_{IN3+}	Noninverting amplifier 3 input
13	V_{IN3-}	Inverting amplifier 3 input
14	V_{OCM3}	Common-mode voltage input 3
15	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
16	$\overline{PD}_4$	Power down 4. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
17	V_{IN4+}	Noninverting amplifier 4 input
18	V_{IN4-}	Inverting amplifier 4 input
19	V_{OCM4}	Common-mode voltage input 4
20	V_{S4+}	Amplifier 4 positive power-supply input
21	V_{OUT4+}	Noninverting amplifier 4 output
22	V_{OUT4-}	Inverting amplifier 4 output
23	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
24	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
25	V_{S3+}	Amplifier 3 positive power-supply input
26	V_{OUT3+}	Noninverting amplifier3 output
27	V_{OUT3-}	Inverting amplifier3 output
28	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
29	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
30	V_{S2+}	Amplifier 2 positive power-supply input
31	V_{OUT2+}	Noninverting amplifier 2 output
32	V_{OUT2-}	Inverting amplifier 2 output
33	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
34	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
35	V_{S1+}	Amplifier 1 positive power-supply input
36	V_{OUT1+}	Noninverting amplifier 1 output
37	V_{OUT1-}	Inverting amplifier 1 output
38	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.

TYPICAL CHARACTERISTICS

Table of Graphs: $V_{S+} - V_{S-} = 3.3$ V

TITLE	FIGURE
Small-Signal Frequency Response	Figure 1
Large-Signal Frequency Response	Figure 2
Large- and Small-Signal Pulse Response	Figure 3
Slew Rate vs V_{OUT} Step	Figure 4
Overdrive Recovery	Figure 5
10-kHz Output Spectrum on AP Analyzer	Figure 6
Harmonic Distortion vs Frequency	Figure 7
Harmonic Distortion vs Output Voltage at 1 MHz	Figure 8
Harmonic Distortion vs Gain at 1 MHz	Figure 9
Harmonic Distortion vs Load at 1 MHz	Figure 10
Harmonic Distortion vs V_{OCM} at 1 MHz	Figure 11
Two-Tone, Second- and Third-Order Intermodulation Distortion vs Frequency	Figure 12
Single-Ended Output Voltage Swing vs Load Resistance	Figure 13
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Turn-on Time	Figure 19
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Input-Referred Voltage Noise and Current Noise Spectral Density	Figure 21
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Output Balance Error vs Frequency	Figure 23
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V_{OCM} Input Impedance vs Frequency	Figure 26

Table of Graphs: $V_{S+} - V_{S-} = 5$ V

TITLE	FIGURE
Small-Signal Frequency Response	Figure 27
Large-Signal Frequency Response	Figure 28
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Slew Rate vs V_{OUT} Step	Figure 30
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Harmonic Distortion vs Output Voltage at 1 MHz	Figure 34
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Single-Ended Output Voltage Swing vs Load Resistance	Figure 39
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Frequency Response vs C_{LOAD} (R_{LOAD} = 1 kΩ)	Figure 41
R_O vs C_{LOAD} (R_{LOAD} = 1 kΩ)	Figure 42
Rejection Ratio vs Frequency	Figure 43
THS4522, THS4524 Crosstalk (Measured Differentially)	Figure 44
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Output Balance Error vs Frequency	Figure 49
V_{OCM} Small-Signal Frequency Response	Figure 50
V_{OCM} Large-Signal Frequency Response	Figure 51
V_{OCM} Input Impedance vs Frequency	Figure 52

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

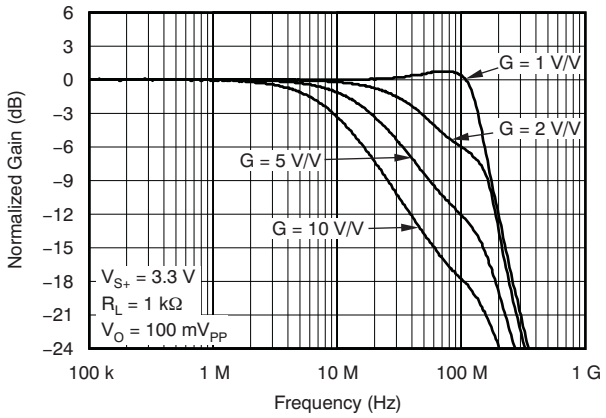

Figure 1.

LARGE-SIGNAL FREQUENCY RESPONSE

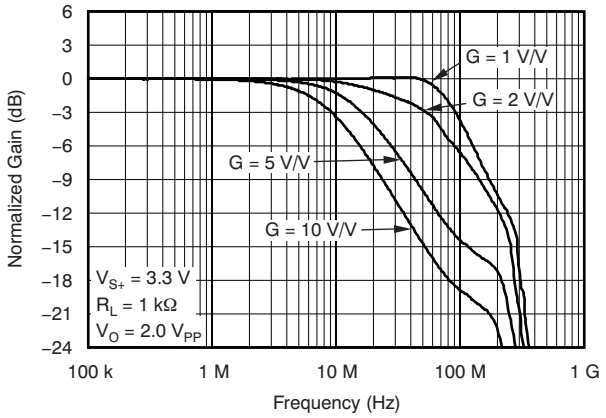

Figure 2.

LARGE- AND SMALL-SIGNAL PULSE RESPONSE

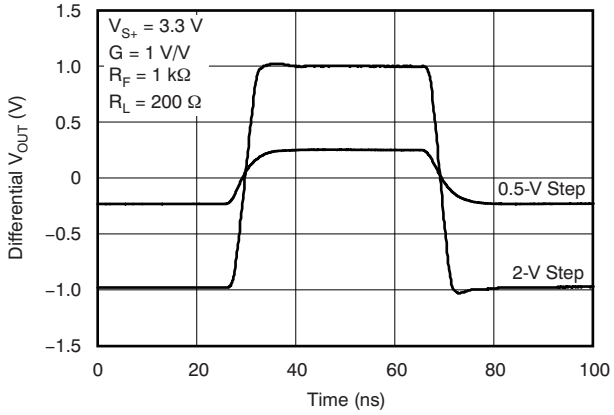

Figure 3.

SLEW RATE vs V_{OUT}

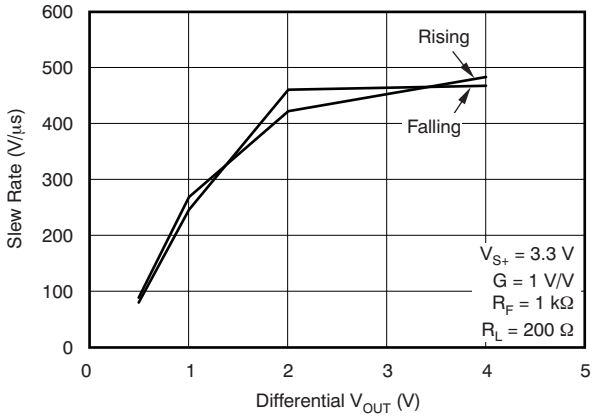

Figure 4.

OVERDRIVE RECOVERY

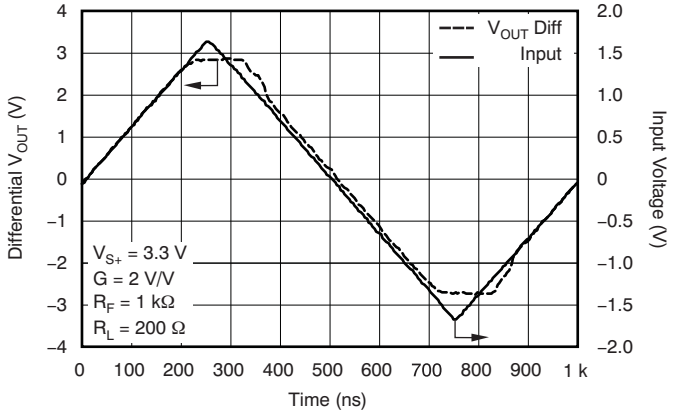

Figure 5.

10-kHz OUTPUT SPECTRUM ON AP ANALYZER

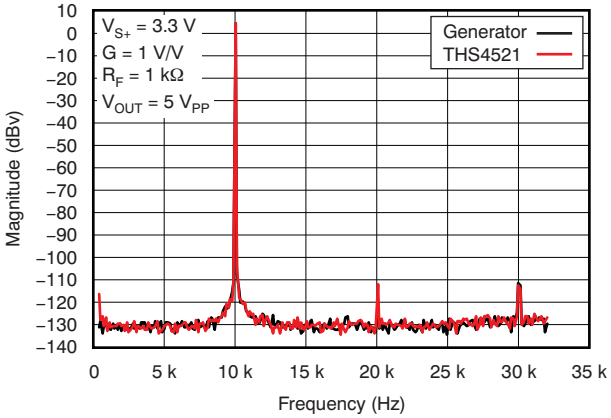

Figure 6.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

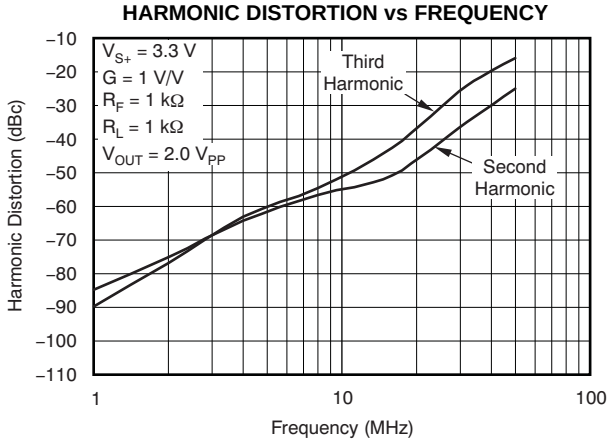

Figure 7.

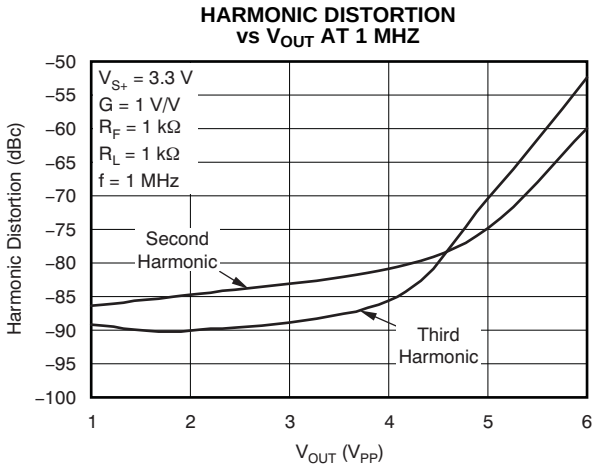

Figure 8.

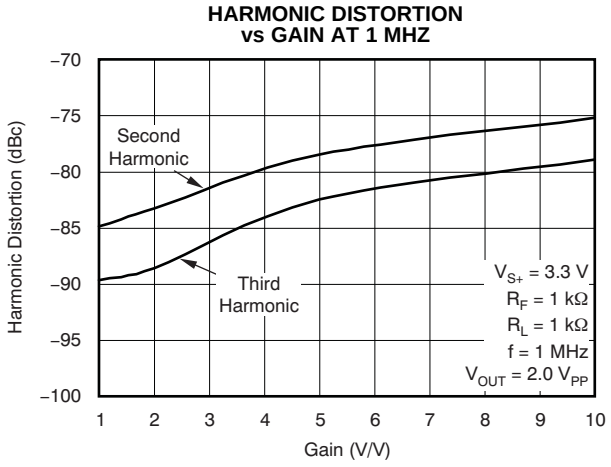

Figure 9.

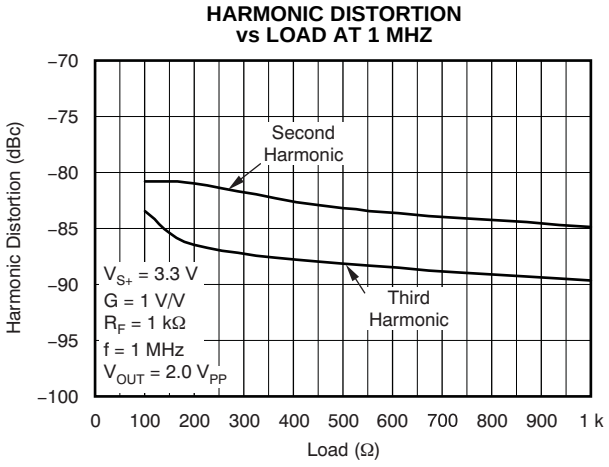

Figure 10.

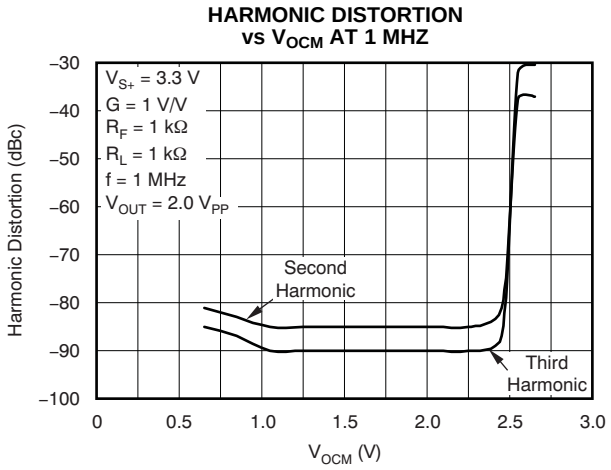

Figure 11.

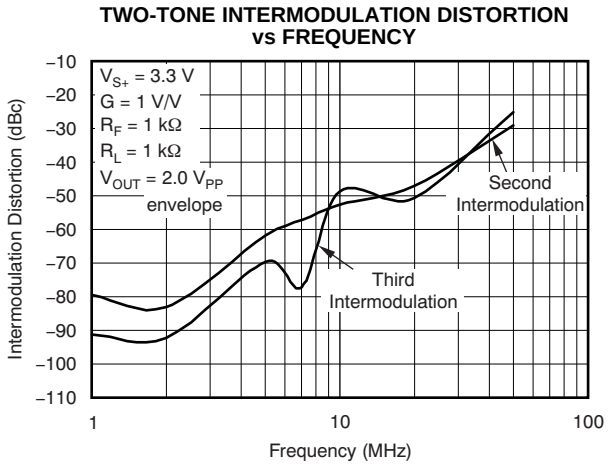

Figure 12.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

SINGLE-ENDED OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

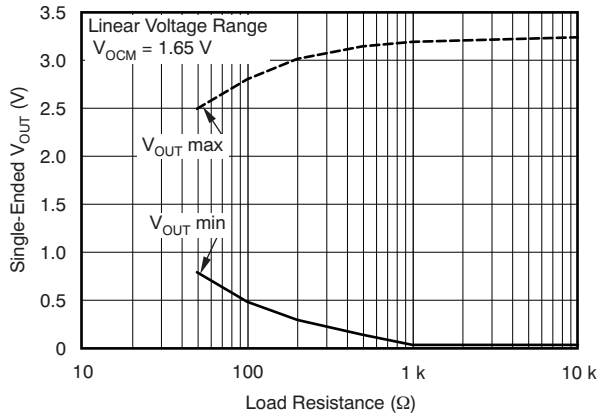

Figure 13.

MAIN AMPLIFIER DIFFERENTIAL OUTPUT IMPEDANCE vs FREQUENCY

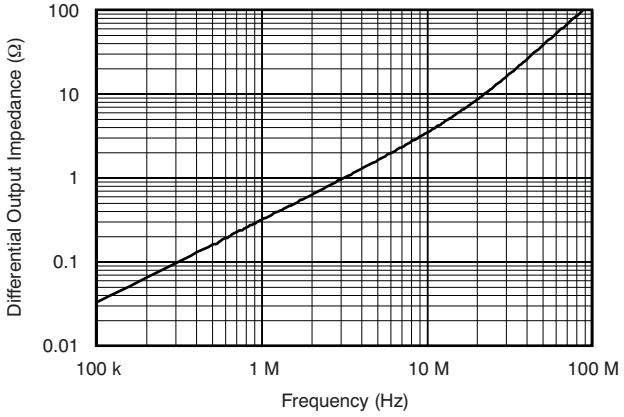

Figure 14.

FREQUENCY RESPONSE vs C_{LOAD} R_{LOAD} = 1 kΩ

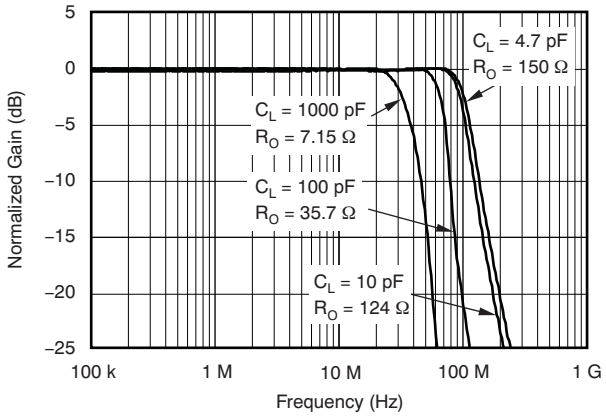

Figure 15.

R_O vs C_{LOAD} R_{LOAD} = 1 kΩ

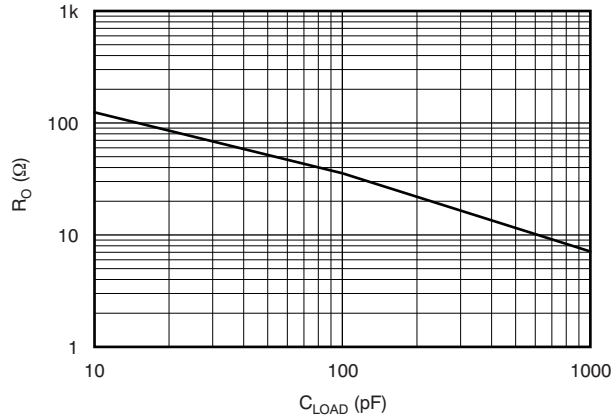

Figure 16.

REJECTION RATIO vs FREQUENCY

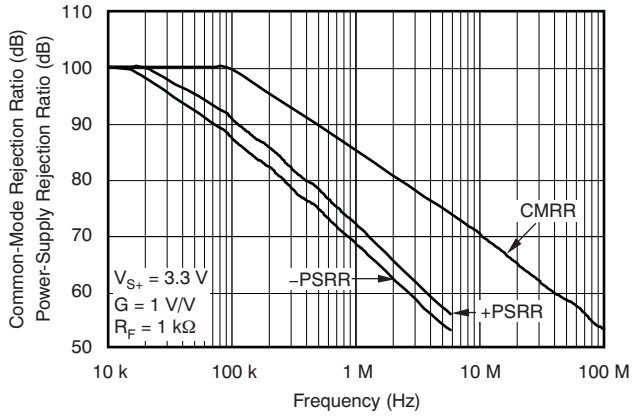

Figure 17.

THS4522, THS4524 CROSSTALK (MEASURED DIFFERENTIALLY)

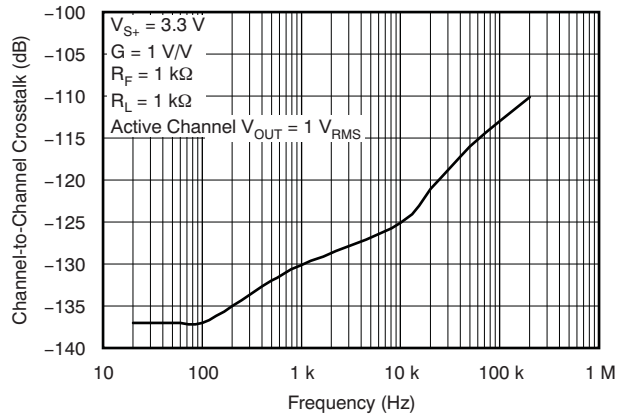

Figure 18.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

TURN-ON TIME

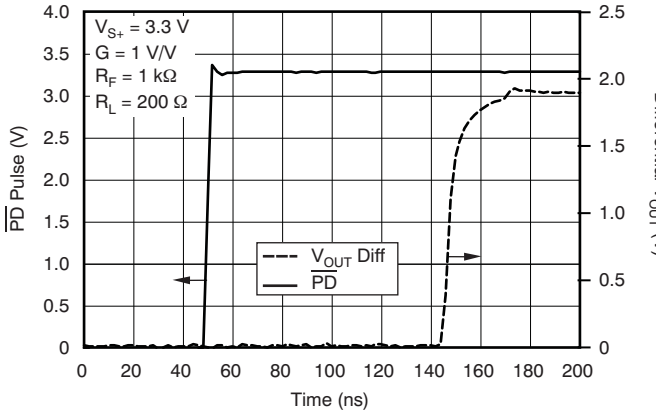

Figure 19.

TURN-OFF TIME

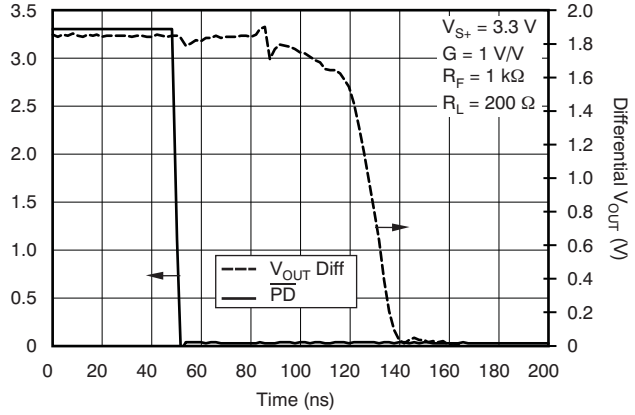

Figure 20.

INPUT-REFERRED VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY

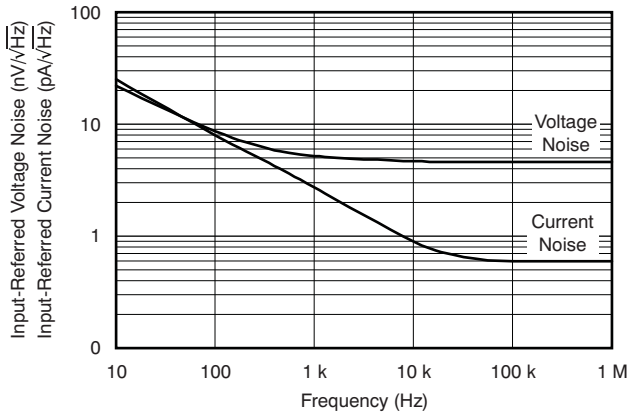

Figure 21.

MAIN AMPLIFIER DIFFERENTIAL OPEN-LOOP GAIN AND PHASE

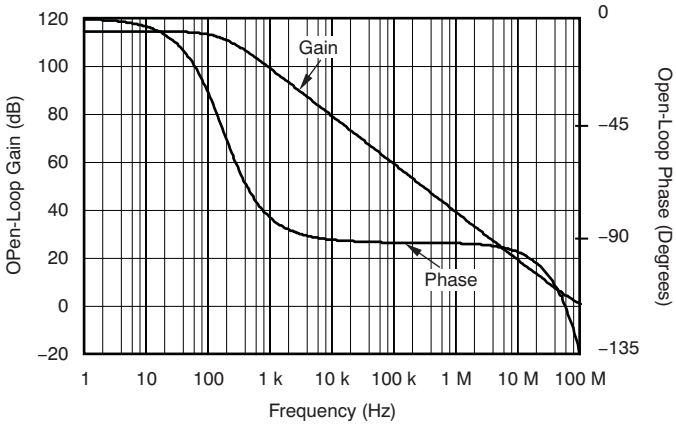

Figure 22.

OUTPUT BALANCE ERROR vs FREQUENCY

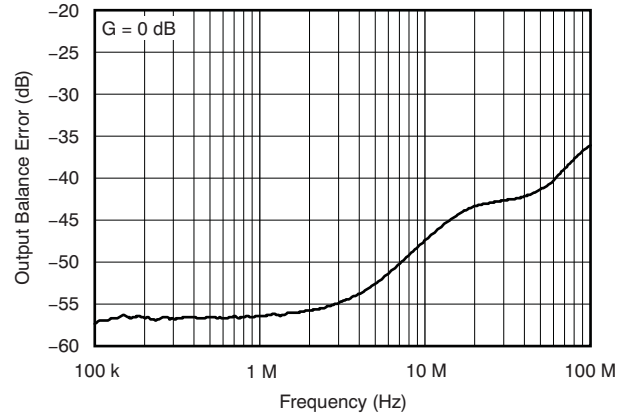

Figure 23.

V_{OCM} SMALL-SIGNAL FREQUENCY RESPONSE

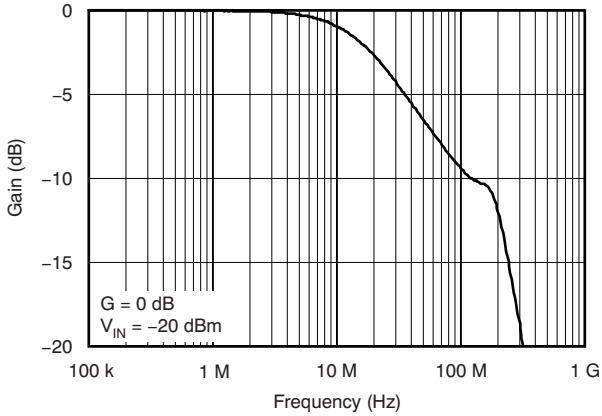

Figure 24.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

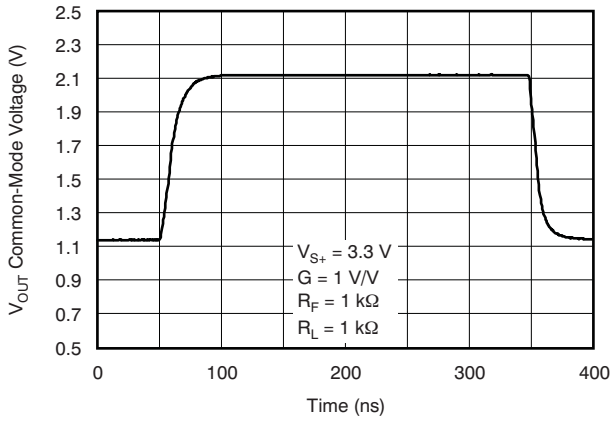

Figure 25.

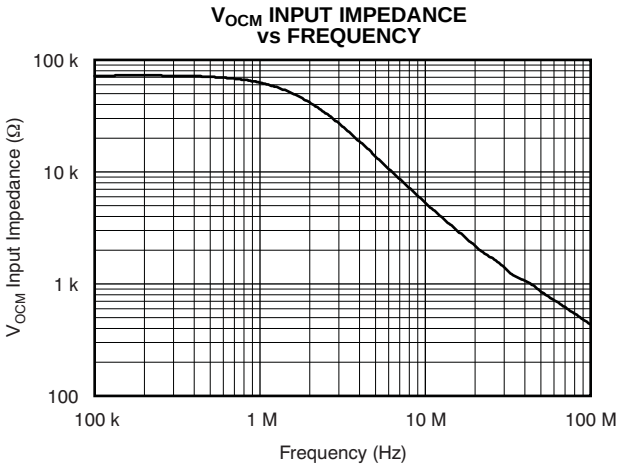

Figure 26.

TYPICAL CHARACTERISTICS: 5 V

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

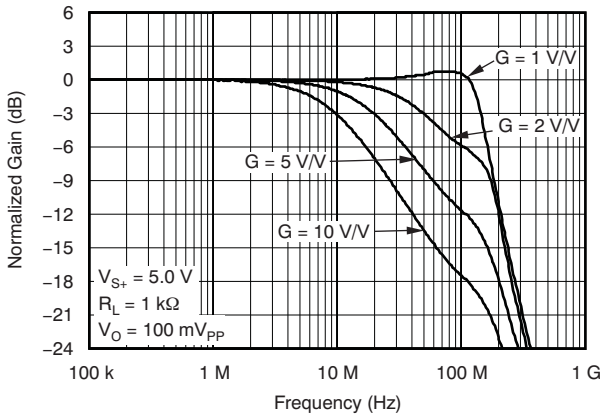

Figure 27.

LARGE-SIGNAL FREQUENCY RESPONSE

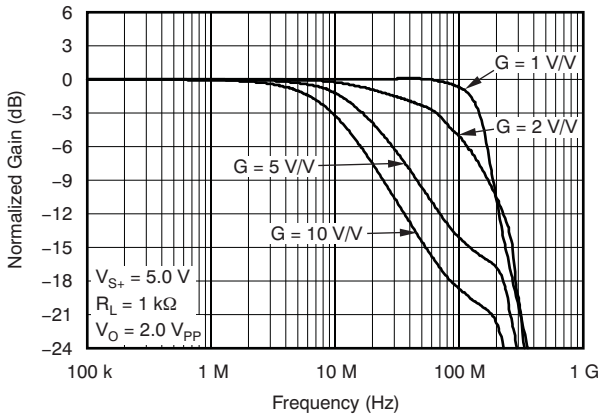

Figure 28.

LARGE- AND SMALL-SIGNAL PULSE RESPONSE

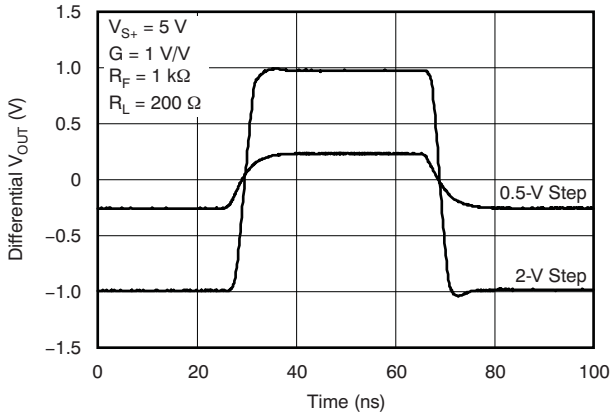

Figure 29.

SLEW RATE vs V_{OUT}

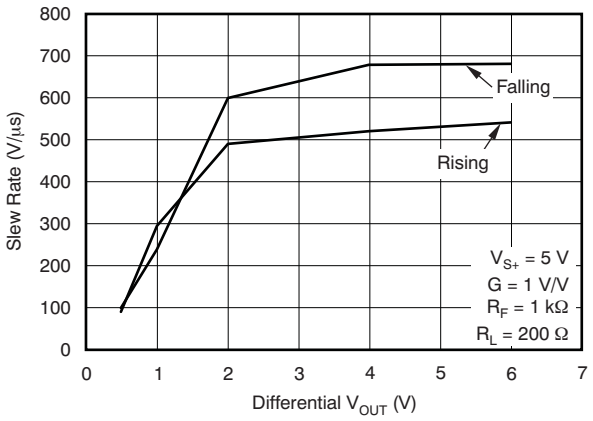

Figure 30.

OVERDRIVE RECOVERY

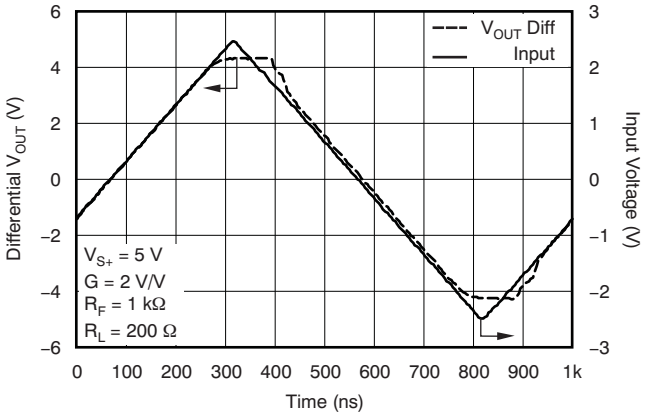

Figure 31.

10-kHz OUTPUT SPECTRUM ON AP ANALYZER AT V_{OUT} = 8 V_{PP}

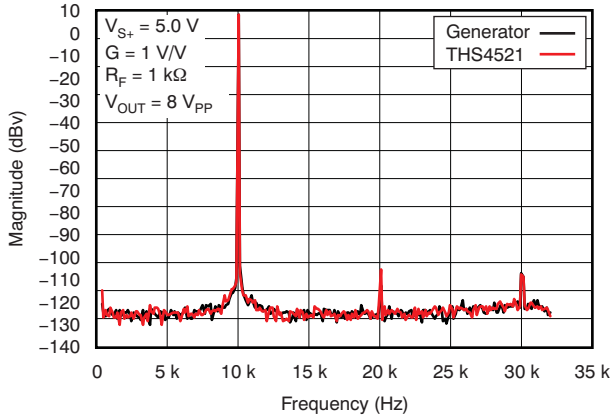

Figure 32.

TYPICAL CHARACTERISTICS: 5 V (continued)

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

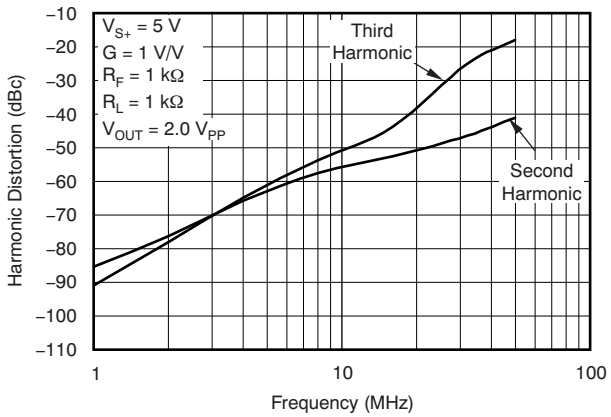

Figure 33.

HARMONIC DISTORTION vs V_{OUT} AT 1 MHZ

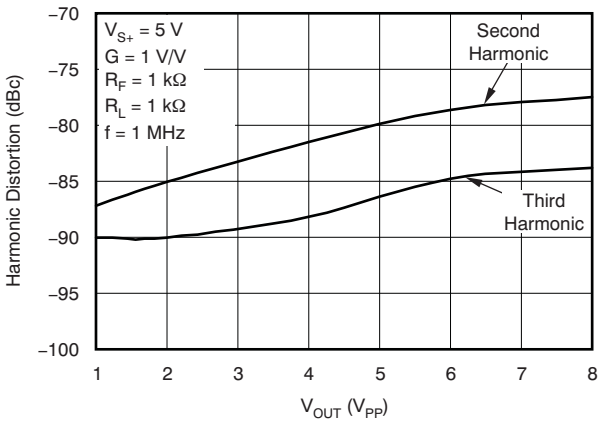

Figure 34.

HARMONIC DISTORTION vs GAIN AT 1 MHZ

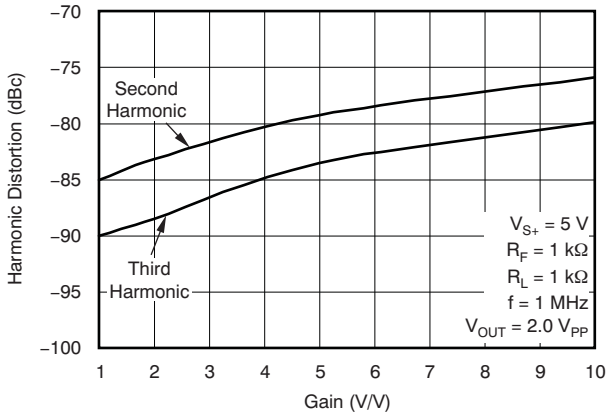

Figure 35.

HARMONIC DISTORTION vs LOAD AT 1 MHZ

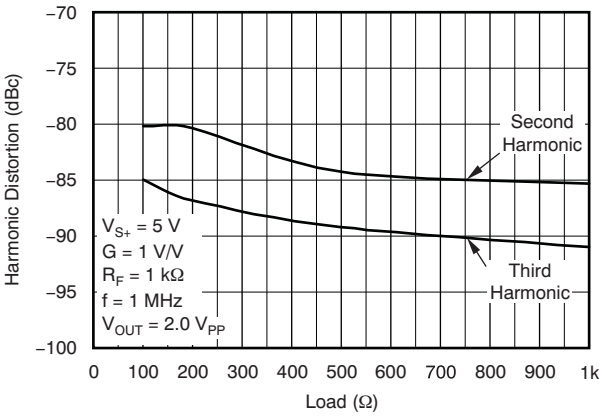

Figure 36.

HARMONIC DISTORTION vs V_{OCM} AT 1 MHZ

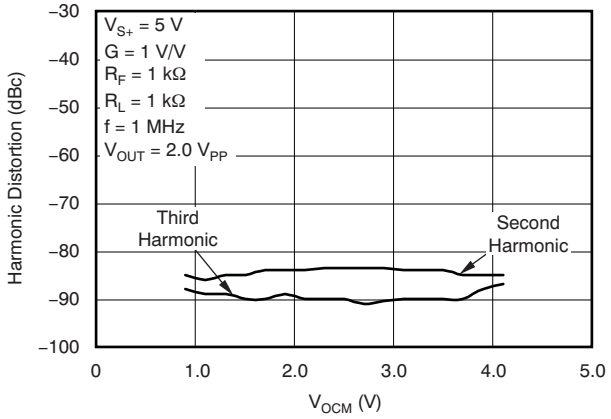

Figure 37.

TWO-TONE INTERMODULATION DISTORTION vs FREQUENCY

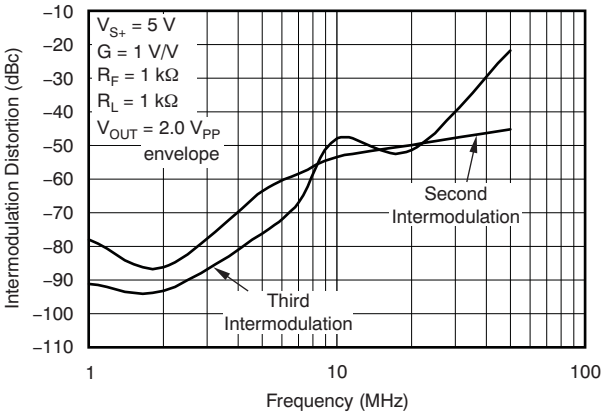

Figure 38.

TYPICAL CHARACTERISTICS: 5 V (continued)

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

SINGLE-ENDED OUTPUT VOLTAGE SWING vs DIFFERENTIAL LOAD RESISTANCE

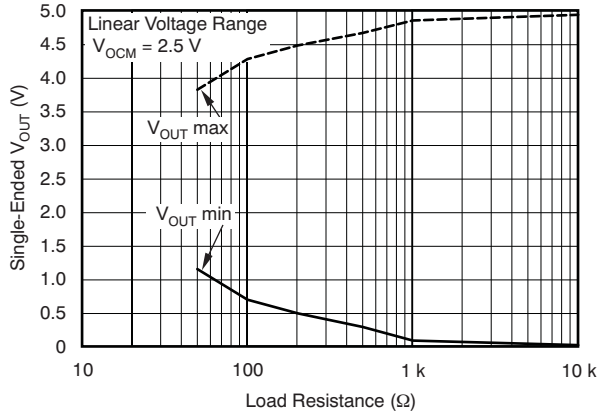

Figure 39.

MAIN AMPLIFIER DIFFERENTIAL OUTPUT IMPEDANCE vs FREQUENCY

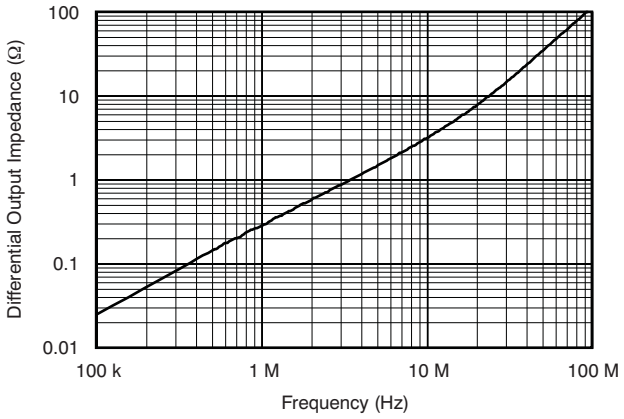

Figure 40.

FREQUENCY RESPONSE vs C_{LOAD} R_{LOAD} = 1 kΩ

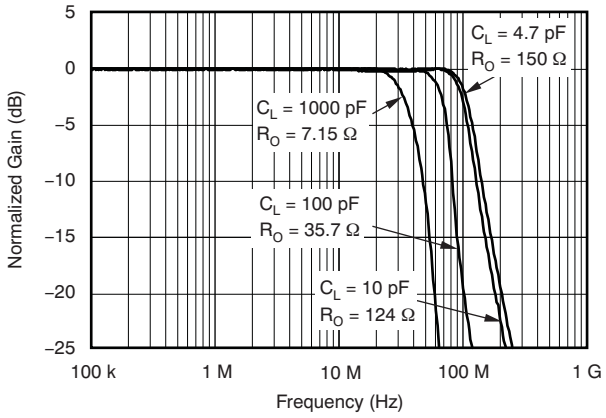

Figure 41.

R_O vs C_{LOAD} R_{LOAD} = 1 kΩ

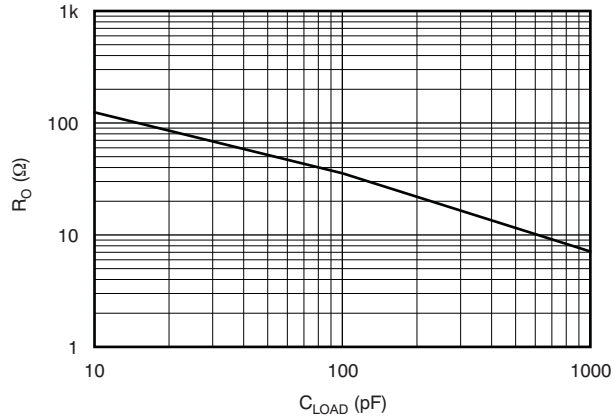

Figure 42.

REJECTION RATIO vs FREQUENCY

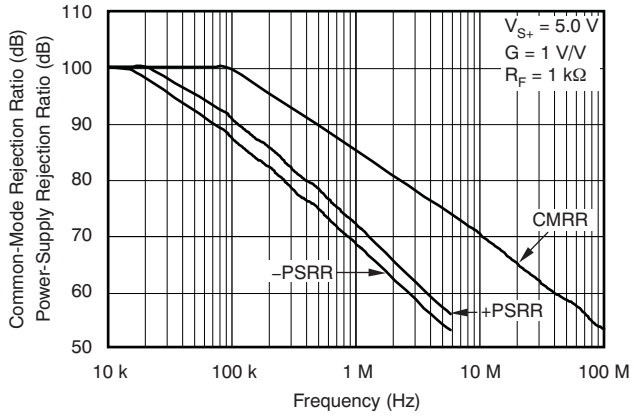

Figure 43.

THS4522, THS4524 CROSSTALK (MEASURED DIFFERENTIALLY)

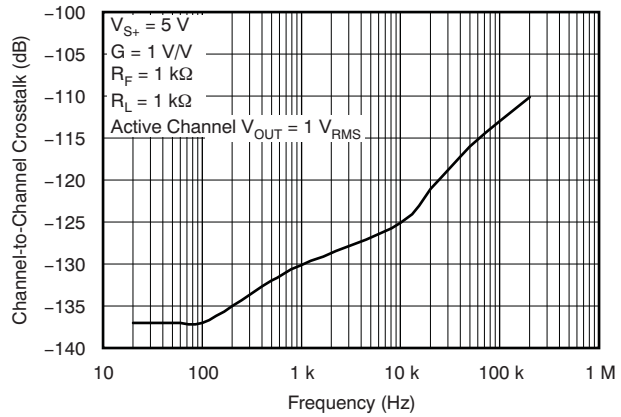

Figure 44.

TYPICAL CHARACTERISTICS: 5 V (continued)

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

TURN-ON TIME

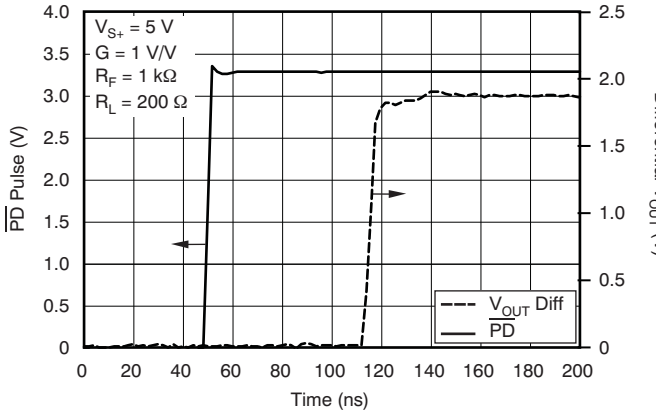

Figure 45.

TURN-OFF TIME

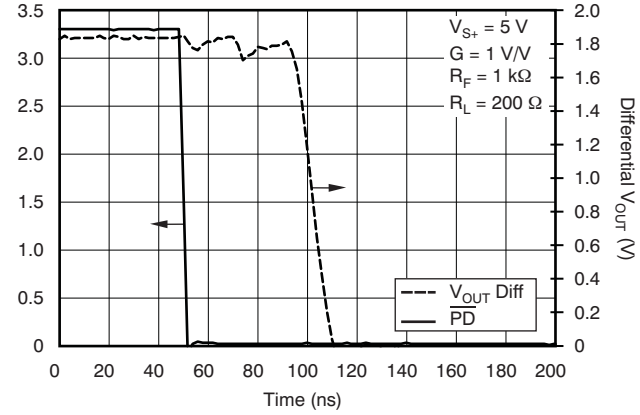

Figure 46.

INPUT-REFERRED VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY

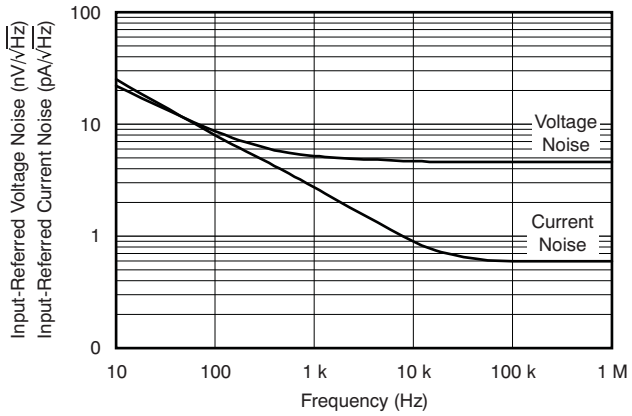

Figure 47.

MAIN AMPLIFIER DIFFERENTIAL OPEN-LOOP GAIN AND PHASE

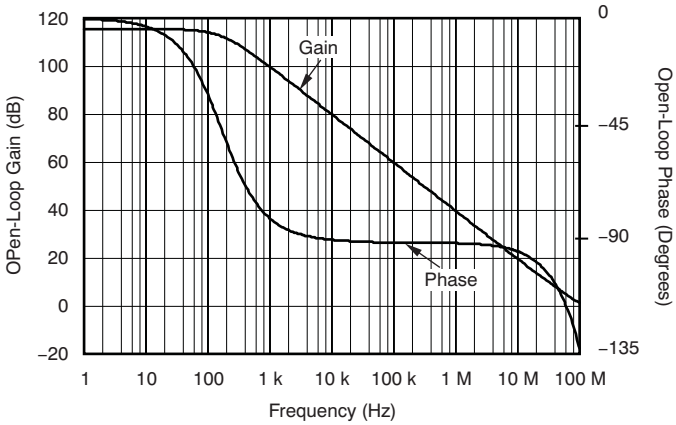

Figure 48.

OUTPUT BALANCE ERROR vs FREQUENCY

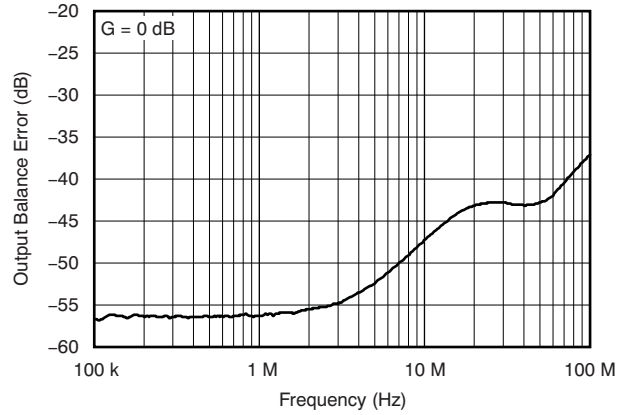

Figure 49.

V_{OCM} SMALL-SIGNAL FREQUENCY RESPONSE

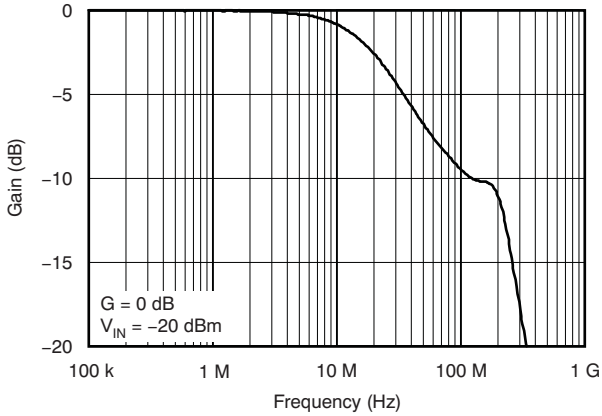

Figure 50.

TYPICAL CHARACTERISTICS: 5 V (continued)

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

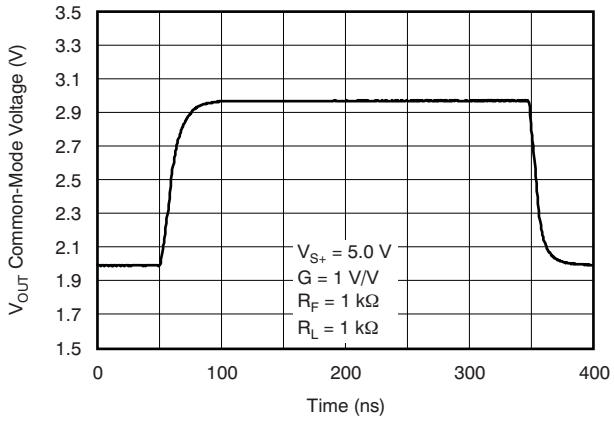

Figure 51.

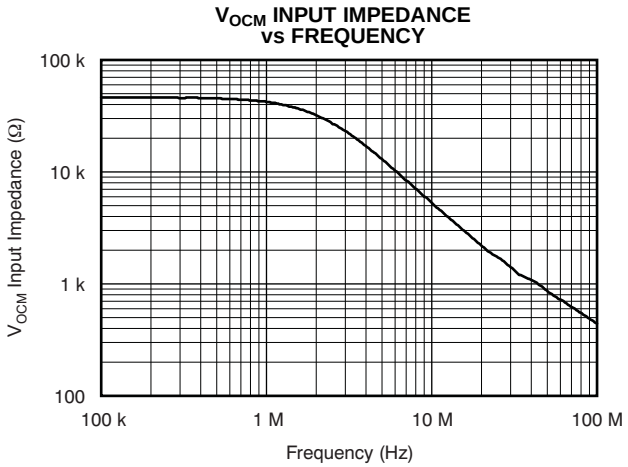

Figure 52.

TEST CIRCUITS

Overview

The THS4521, THS4522, and THS4524 family is tested with the test circuits shown in this section; all circuits are built using the available THS4521 evaluation module (EVM). For simplicity, power-supply decoupling is not shown; see the layout in the *Applications* section for recommendations. Depending on the test conditions, component values change in accordance with Table 1 and Table 2, or as otherwise noted. In some cases the signal generators used are ac-coupled and in others they dc-coupled 50-Ω sources. To balance the amplifier when ac-coupled, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input; when dc-coupled, only the 49.9-Ω resistor to ground is added across R_{IT}. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated in a single-supply configuration as described in the *Applications* section with no impact on performance. Also, for most of the tests, except as noted, the devices are tested with single-ended inputs and a transformer on the output to convert the differential output to single-ended because common lab test equipment has single-ended inputs and outputs. Similar or better performance can be expected with differential inputs and outputs.

As a result of the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The ***Atten*** column in Table 2 shows the attenuation expected from the resistor divider. When using a transformer at the output (as shown in Figure 54), the signal sees slightly more loss because of transformer and line loss; these numbers are approximate.

Table 1. Gain Component Values for Single-Ended Input(1)

Gain	R_F	R_G	R_{IT}
1 V/V	1 kΩ	1 kΩ	52.3 Ω
2 V/V	1 kΩ	487 Ω	53.6 Ω
5 V/V	1 kΩ	187 Ω	59.0 Ω
10 V/V	1 kΩ	86.6 Ω	69.8 Ω

1. Gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-Ω input termination.

Table 2. Load Component Values For 1:1 Differential to Single-Ended Output Transformer(1)

R_L	R_O	R_{OT}	Atten
100 Ω	24.9 Ω	Open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1 kΩ	487 Ω	52.3 Ω	31.8 dB

1. Total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

Frequency Response

The circuit shown in Figure 53 is used to measure the frequency response of the circuit.

An HP network analyzer is used as the signal source and the measurement device. The output impedance of the HP network analyzer is is dc-coupled and is 50 Ω. R_{IT} and R_G are chosen to impedance-match to 50 Ω and maintain the proper gain. To balance the amplifier, a 49.9-Ω resistor to ground is inserted across R_{IT} on the alternate input.

The output is probed using a Tektronix high-impedance differential probe across the 953-Ω resistor and referred to the amplifier output by adding back the 0.42-dB because of the voltage divider on the output.

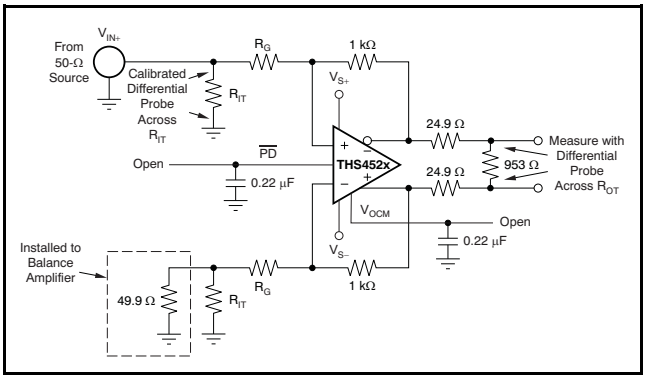

Figure 53. Frequency Response Test Circuit

Distortion

The circuit shown in Figure 54 is used to measure harmonic and intermodulation distortion of the amplifier.

An HP signal generator is used as the signal source and the output is measured with a Rhode and Schwarz spectrum analyzer. The output impedance of the HP signal generator is ac-coupled and is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω and maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured and then a high-pass filter is inserted at the output to reduce the fundamental so it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single-ended is an ADT1–1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

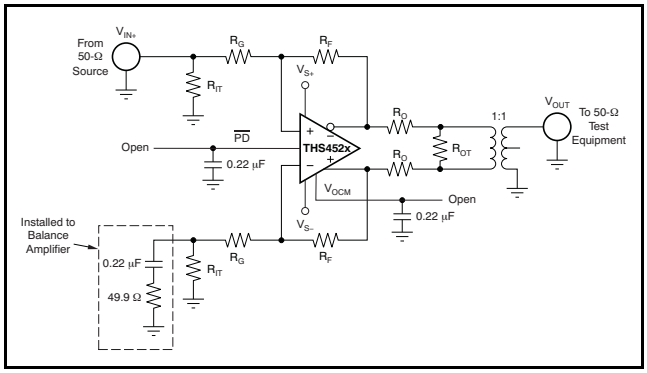

Figure 54. Distortion Test Circuit

Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Turn-Off Time

The circuit shown in Figure 55 is used to measure slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and ampliifer turn-on/turn-off time. Turn-on and turn-off time are measured with the same circuit modified for 50-Ω input impedance on the $\overline{PD}$ input by replacing the 0.22-µF capacitor with a 49.9-Ω resistor. For output impedance, the signal is injected at V_{OUT} with V_{IN} open; the drop across the 2x 49.9-Ω resistors is then used to calculate the impedance seen looking into the amplifier output.

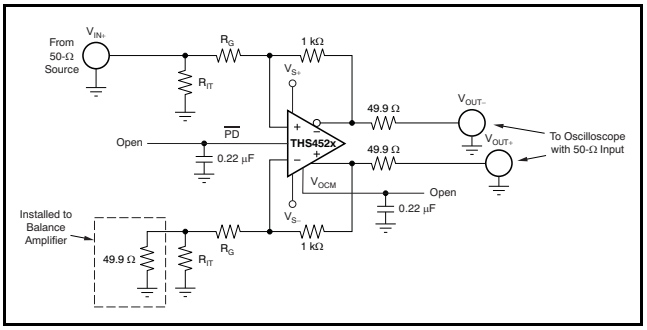

Figure 55. Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive Recovery, V_{OUT} Swing, and Turn-On/Turn-Off Test Circuit

Common-Mode and Power-Supply Rejection

The circuit shown in Figure 56 is used to measure the CMRR. The signal from the network analyzer is applied common-mode to the input. Figure 57 is used to measure the PSRR of V_{S+} and V_{S-}. The power supply under test is applied to the network analyzer dc offset input. For both CMRR and PSRR, the output is probed using a Tektronix high-impedance differential probe across the 953-Ω resistor and referred to the amplifier output by adding back the 0.42-dB as a result of the voltage divider on the output. For these tests, the resistors are matched for best results.

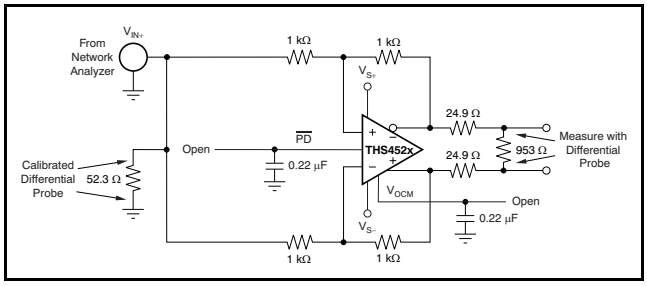

Figure 56. CMRR Test Circuit

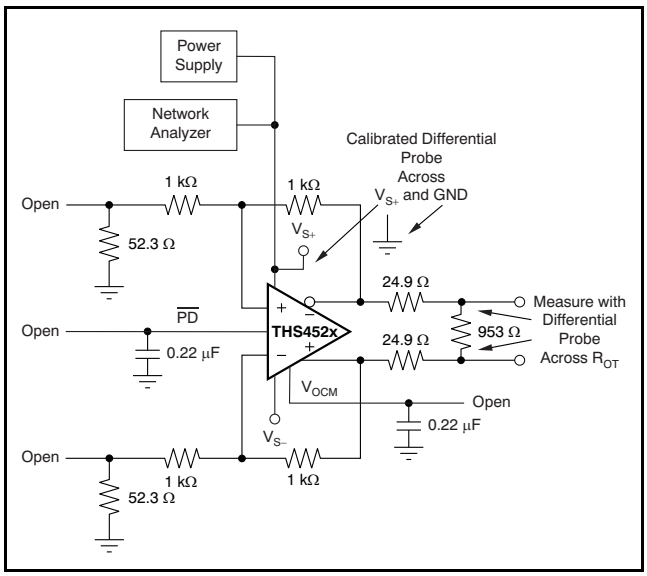

Figure 57. PSRR Test Circuit

V_{OCM} Input

The circuit illustrated in Figure 58 is used to measure the frequency response and input impedance of the V_{OCM} input. Frequency response is measured using a Tektronix high-impedance differential probe, with R_{CM} = 0 Ω at the common point of V_{OUT+} and V_{OUT-}, formed at the summing junction of the two matched 499-Ω resistors, with respect to ground. The input impedance is measured using a Tektronix high-impedance differential probe at the V_{OCM} input with R_{CM} = 10 kΩ and the drop across the 10-kΩ resistor is used to calculate the impedance seen looking into the amplifier V_{OCM} input.

The circuit shown in Figure 59 measures the transient response and slew rate of the V_{OCM} input. A 1-V step input is applied to the V_{OCM} input and the output is measured using a 50-Ω oscilloscope input referenced back to the amplifier output.

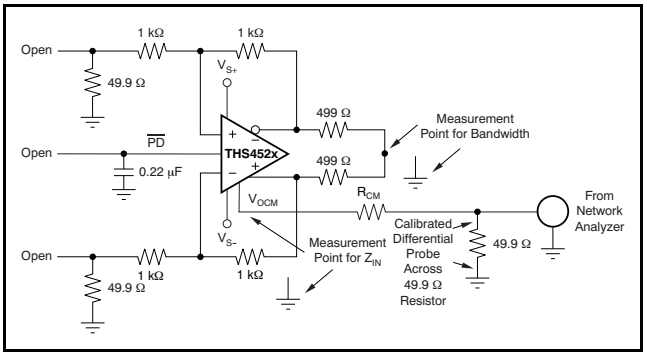

Figure 58. V_{OCM} Input Test Circuit

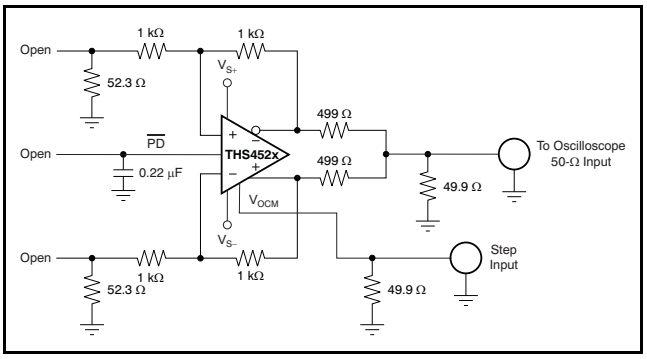

Figure 59. V_{OCM} Transient Response and Slew Rate Test Circuit

APPLICATION INFORMATION

The following circuits show application information for the THS4521, THS4522, and THS4524 family. For simplicity, power-supply decoupling capacitors are not shown in these diagrams; see the *EVM and Layout Recommendations* section for suggested guidelines. For more details on the use and operation of fully differential op amps, refer to the Application Report Fully-Differential Amplifiers (SLOA054), available for download from the TI web site at www.ti.com.

Differential Input to Differential Output Amplifier

The THS4521, THS4522, and THS4524 family are fully-differential operational amplifiers that can be used to amplify differential input signals to differential output signals. Figure 60 shows a basic block diagram of the circuit (V_{OCM} and $\overline{PD}$ inputs not shown). The gain of the circuit is set by R_F divided by R_G.

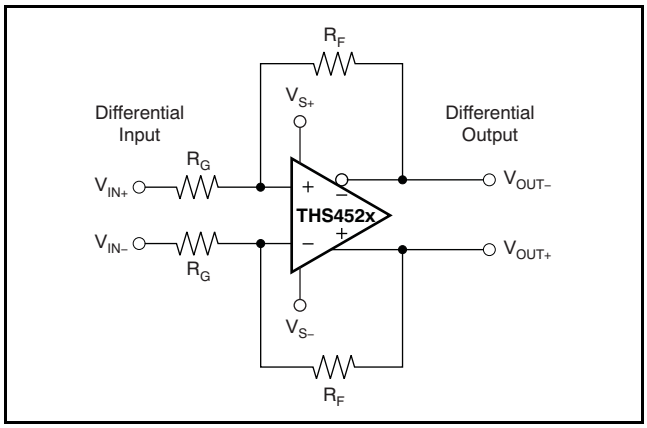

Figure 60. Differential Input to Differential Output Amplifier

Single-Ended Input to Differential Output Amplifier

The THS4521, THS4522, and THS4524 family can also amplify and convert single-ended input signals to differential output signals. Figure 61 illustrates a basic block diagram of the circuit (V_{OCM} and $\overline{PD}$ inputs not shown). The gain of the circuit is again set by R_F divided by R_G.

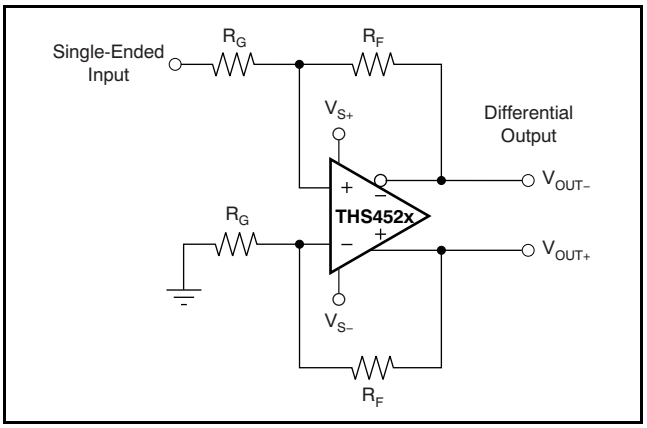

Figure 61. Single-Ended Input to Differential Output Amplifier

Input Common-Mode Voltage Range

The input common-mode voltage of a fully-differential op amp is the voltage at the **+** and **–** input pins of the device.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming the op amp is in linear operation, the voltage across the input pins is only a few millivolts at most. Therefore, finding the voltage at one input pin determines the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$\left(V_{OUT+} \times \frac{R_G}{R_G + R_F}\right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F}\right) \quad (1)$$

To determine the V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}. As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

Setting the Output Common-Mode Voltage

The output common-model voltage is set by the voltage at the V_{OCM} pin. The internal common-mode control circuit maintains the output common-mode voltage within 5-mV offset (typ) from the set voltage. If left unconnected, the common-mode set point is set to midsupply by internal circuitry, which may be overdriven from an external source. Figure 62 represents the V_{OCM} input. The internal V_{OCM} circuit has typically 23 MHz of –3 dB bandwidth, which is required for best performance, but it is intended to be a dc bias input pin. A 0.22-µF bypass capacitor is recommended on this pin to reduce noise. The external current required to overdrive the internal resistor divider is given approximately by the formula in Equation 2:

$$I_{EXT} = \frac{2V_{OCM} - (V_{S+} - V_{S-})}{50\ k\Omega} \quad (2)$$

where:

- V_{OCM} is the voltage applied to the V_{OCM} pin

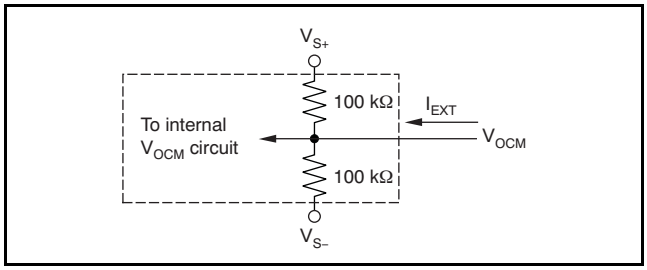

Figure 62. V_{OCM} Input Circuit

Typical Performance Variation with Supply Voltage

The THS4521, THS4522, and THS4524 family of devices provide excellent performance across the specified power-supply range of 2.5 V to 5.5 V with only minor variations. The input and output voltage compliance ranges track with the power supply in nearly a 1:1 correlation. Other changes can be observed in slew rate, output current drive, open-loop gain, bandwidth, and distortion. Table 3 shows the typical variation to be expected in these key performance parameters.

Single-Supply Operation

To facilitate testing with common lab equipment, the THS4521EVM allows for split-supply operation; most of the characterization data presented in this data sheet is measured using split-supply power inputs. The device can easily be used with a single-supply power input without degrading performance.

Figure 63 shows a dc-coupled single-supply circuit with single-ended inputs. This circuit can also be applied to differential input sources.

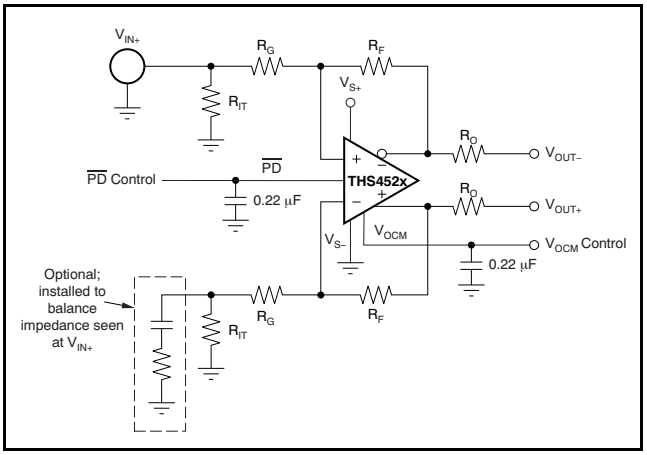

Figure 63. THS4521 DC-Coupled Single-Supply with Single-Ended Inputs

The input common-mode voltage range of the THS4521, THS4522, and THS4524 family is designed to include the negative supply voltage. in the circuit shown in Figure 63, the signal source is referenced to ground. V_{OCM} is set by an external control source or, if left unconnected, the internal circuit defaults to midsupply. Together with the input impedance of the amplifier circuit, R_{IT} provides input termination, which is also referenced to ground.

Note that R_{IT} and optional matching components are added to the alternate input to balance the impedance at signal input.

Table 3. Typical Performance Variation versus Power-Supply Voltage

PARAMETER	V_S = 5 V	V_S = 3.3 V	V_S = 2.5 V
–3-dB Small-signal bandwidth	145 MHz	135 MHz	125 MHz
Slew rate (2-V step)	490 V/µs	420 V/µs	210 V/µs
Harmonic distortion at 1 MHz, 2 V_{PP}, R_L = 1 kΩ			
Second harmonic	–85 dBc	–85 dBc	–84 dBc
Third harmonic	–91 dBc	–90 dBc	–88 dBc
Open-loop gain	119 dB	116 dB	115 dB
Linear output current drive	55 mA	35 mA	24 mA

Low-Power Applications and the Effects of Resistor Values on Bandwidth

For low-power operation, it may be necessary to increase the gain setting resistors values to limit current consumption and not load the source. Using larger value resistors lowers the bandwidth of the THS4521, THS4522, and THS4524 family as a result of the interactions between the resistors, the device parasitic capacitance, and printed circuit board (PCB) parasitic capacitance. Figure 64 shows the small-signal frequency response with 1-kΩ, 10-kΩ, and 100-kΩ resistors for R_F, R_G, and R_L (impedance is assumed to typically increase for all three resistors in low-power applications).

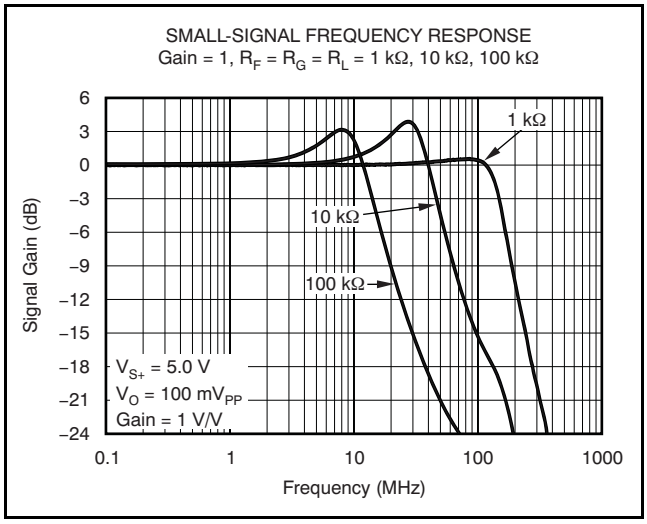

Figure 64. THS4521 Frequency Response with Various Gain Setting and Load Resistor Values

Frequency Response Variation due to Package Options

Users can see variations in the small-signal (V_{OUT} = 100 mV_{PP}) frequency response between the available package options for the THS4521, THS4522, and THS4524 family as a result of parasitic elements associated with each package and board layout changes. Figure 65 shows the variance measured in the lab; this variance is to be expected even when using a good layout.

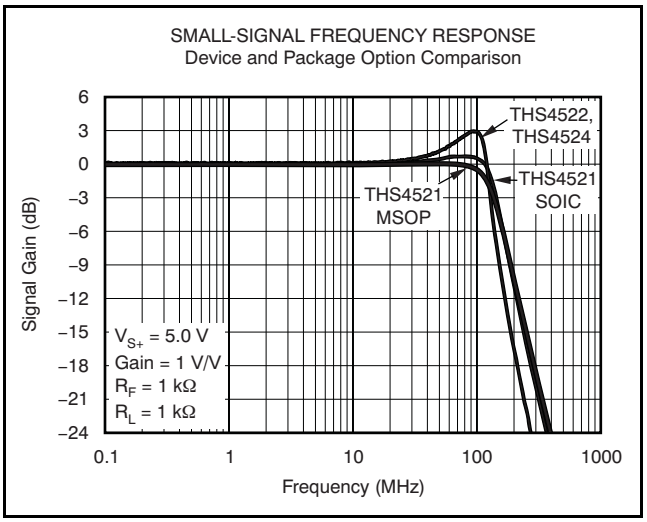

Figure 65. Small-Signal Frequency Response: Package Variations

Driving Capacitive Loads

The THS4521, THS4522, and THS4524 family is designed for a nominal capacitive load of 1 pF on each output to ground. When driving capacitive loads greater than 1 pF, it is recommended to use small resistors (R_O) in series with the output, placed as close to the device as possible. Without R_O, capacitance on the output interacts with the output impedance of the amplifier and causes phase shift in the loop gain of the amplifier that reduces the phase margin.

This reduction in phase margin results in frequency response peaking; overshoot, undershoot, and/or ringing when a step or square-wave signal is applied; and may lead to instability or oscillation. Inserting R_O isolates the phase shift from the loop gain path and restores the phase margin, but it also limits bandwidth. Figure 66 shows the recommended values of R_O versus capacitive loads (C_L). Figure 67 shows the frequency response with various values.

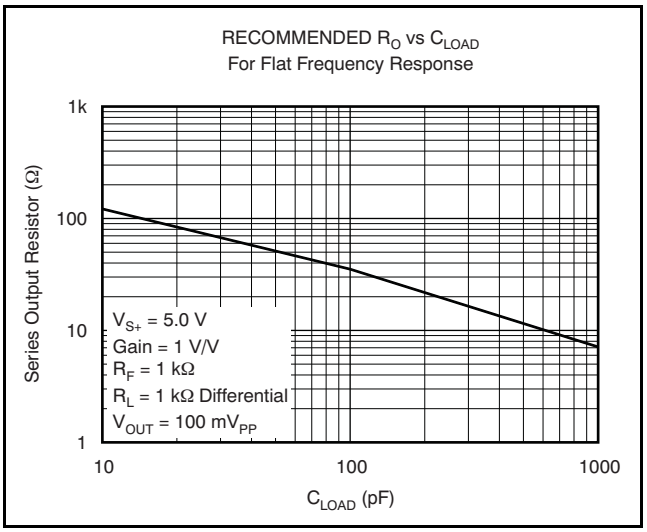

Figure 66. Recommended Series Output Resistor versus Capacitive Load for Flat Frequency Response, with R_{LOAD} = 1 kΩ

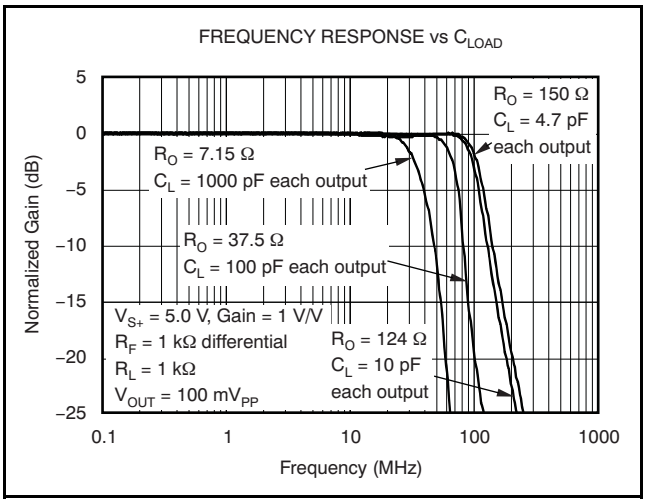

Figure 67. Frequency Response for Various R_O and C_L Values, with R_{LOAD} = 1 kΩ

Audio Performance

The THS4521, THS4522, and THS4524 family provide excellent audio performance with very low quiescent power. To show performance in the audio band, the device was tested with a SYS-2722 audio analyzer from Audio Precision. THD+N and FFT tests were performed at 1-V_{RMS} output voltage. Performance is the same on both 3.3-V and 5-V supplies. Figure 68 shows the test circuit used; Figure 69 and Figure 70 show the performance of the analyzer using internal loopback mode (generator) together with the THS4521. Note that the harmonic distortion performance is very close to the same with and without the device meaning the THS4521 performance is actually much better than can be directly measured by this meathod. Using these measurements and simuation, we estimate the second-order harmonic distortion to be –133 dBc and the third-order harmonic distortion to be –140 dBc at 10 kHz. Note that the circuit of Figure 68 is also used to measure crosstalk between channels on the THS4522 and THS4524 using the crosstalk meter function of the AP audio analyzer.

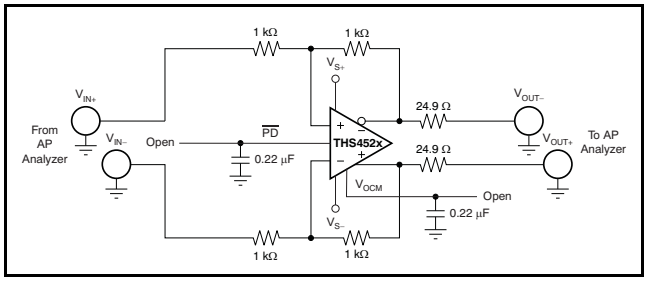

Figure 68. THS4521 AP Analyzer Test Circuit

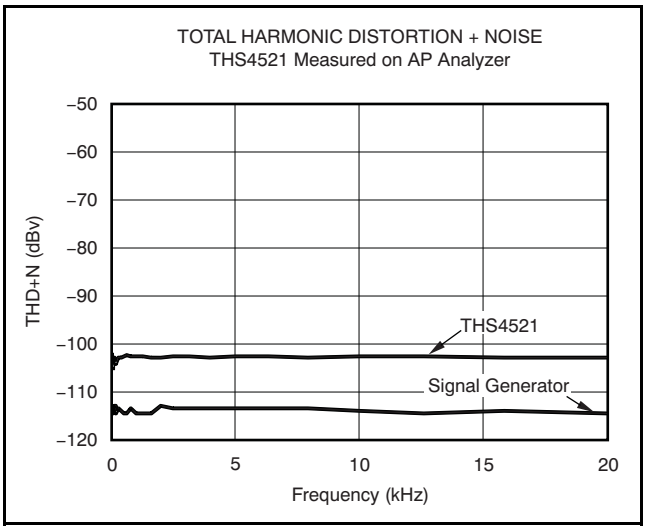

Figure 69. THS4521 1-V_{RMS} 20-Hz to 20-kHz THD+N

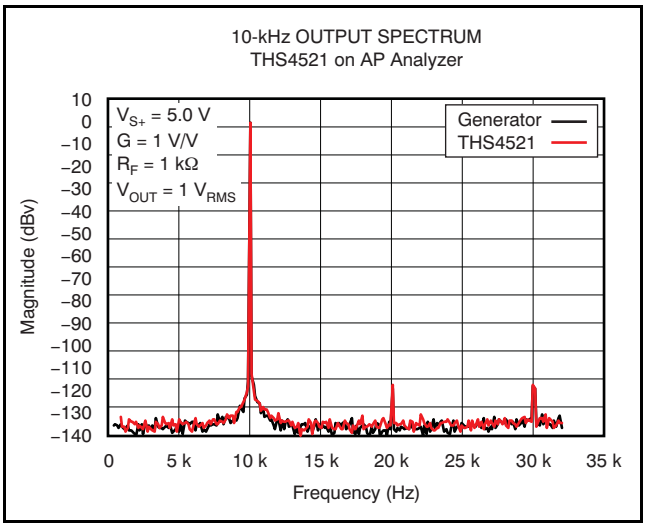

Figure 70. THS4521 1-V_{RMS} 10-kHz FFT Plot

ADC Driver Performance: THS4521 and ADS1278 Combined Performance

The THS4521 provides excellent performance when driving high-performance delta-sigma (ΔΣ) and successive approximation register (SAR) ADCs in audio and industrial applications using a single 3-V to 5-V power supply. To show achievable performance, the THS4521 is tested as the drive amplifier for the ADS1278 24-bit ADC. The ADS1278 offers excellent ac and dc performance, with four selectable operating modes from 10 kSPS to 128 kSPS to enable the user to fine-tune performance and power for specific application needs. The circuit shown in Figure 71 was used to test the performance. Data were taken using the High-Resolution mode (52 kSPS) of the ADS1278 with input frequencies at 1 kHz and 10 kHz and signal levels 1/2 dB below full-scale (–0.5 dBFS). FFT plots showing the spectral performance are given in Figure 72 and Figure 73; tabulated ac analysis results are shown in Table 4.

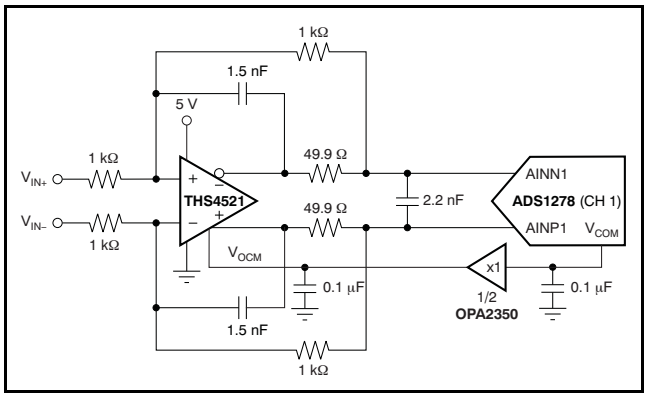

Figure 71. THS4521 and ADS1278 (Ch 1) Test Circuit

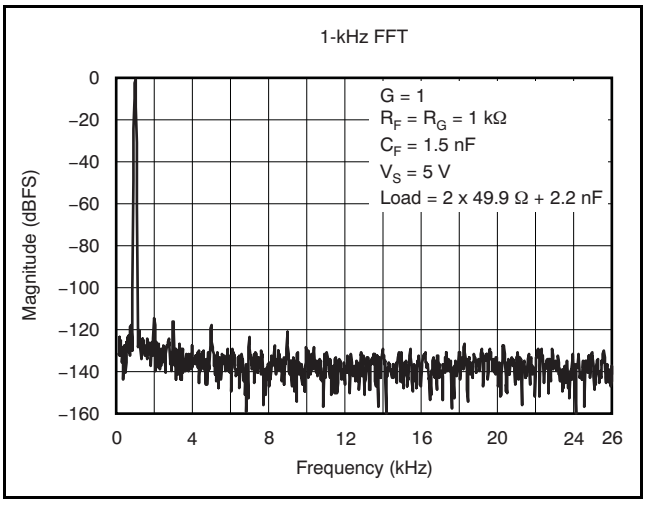

Figure 72. 1-kHz FFT

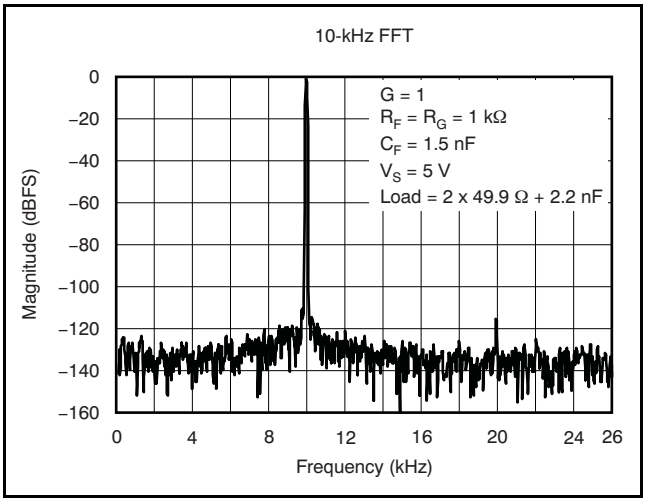

Figure 73. 10-kHz FFT

Table 4. AC Analysis

Tone (Hz)	Signal (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
1 k	–0.50	109.1	–107.9	105.5	113.7
10 k	–0.50	101.8	–109.8	101.1	109.8

ADC Driver Performance: THS4521 and ADS8321 Combined Performance

To demonstrate achievable performance, the THS4521 is tested as the drive amplifier for the ADS8321 16-bit SAR ADC. The ADS8321 offers excellent ac and dc performance, with ultra-low power and small size. The circuit shown in Figure 74 was used to test the performance. Data were taken using the ADS8321 at 100 kSPS with input frequencies of 2 kHz and 10 kHz and signal levels that were -0.5 dBFS. FFT plots that illustrate the spectral performance are given in Figure 75 and Figure 76. Tabulated ac analysis results are listed in Table 5.

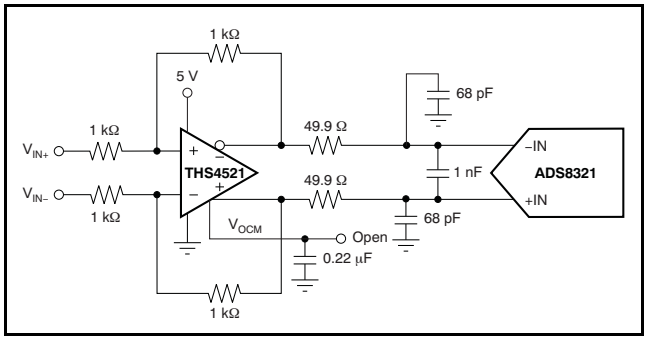

Figure 74. THS4521 and ADS8321 Test Circuit

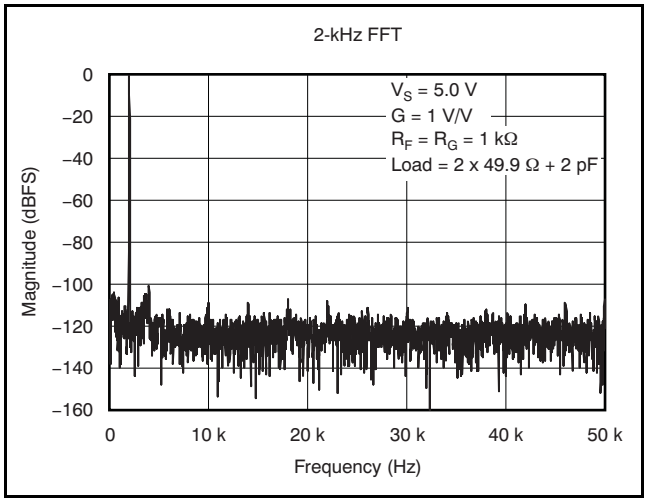

Figure 75. 2-kHZ FFT

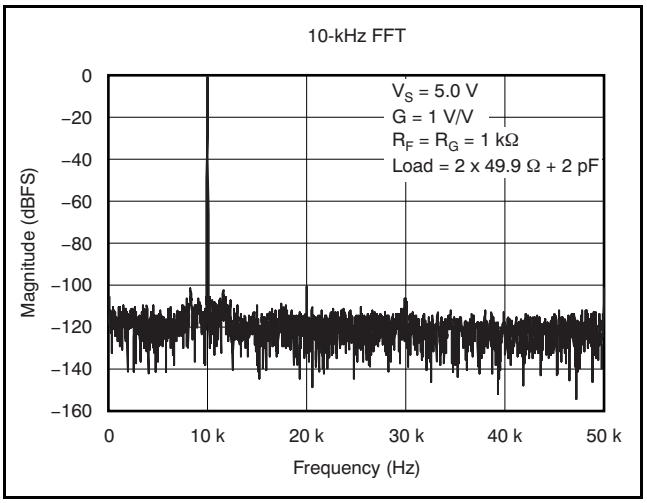

Figure 76. 10-kHz FFT

Table 5. AC Analysis

Tone (Hz)	Signal (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
2 k	–0.5	86.7	–97.8	86.4	100.7
10 k	–0.6	85.2	–98.1	85.2	102.2

EVM AND LAYOUT RECOMMENDATIONS

Figure 77 shows the THS4521EVM schematic. PCB layers 1 through 4 are shown in Figure 78; Table 6 lists the bill of materials for the THS4521EVM as supplied from TI. It is recommended to follow the layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. Follow these general guidelines:

1. Signal routing should be direct and as short as possible into and out of the op amp circuit.
2. The feedback path should be short and direct.
3. Ground or power planes should be removed from directly under the amplifier input and output pins.
4. An output resistor is recommended in each output lead, placed as near to the output pins as possible.
5. Two 0.1-µF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 10-µF power-supply decoupling capacitors should be placed within 1 inch of the device and can be shared among multple analog devices.
7. A 0.22-µF capacitor should be placed between the V_{OCM} input pin and ground near to the pin. This capacitor limits noise coupled into the pin.
8. The $\overline{PD}$ pin uses TTL logic levels; a bypass capacitor is not necessary if actively driven, but can be used for robustness in noisy environments whether driven or not.
9. If input termination resistors R_{10} and R_{11} are used, a single point connection to ground on L2 is recommended.

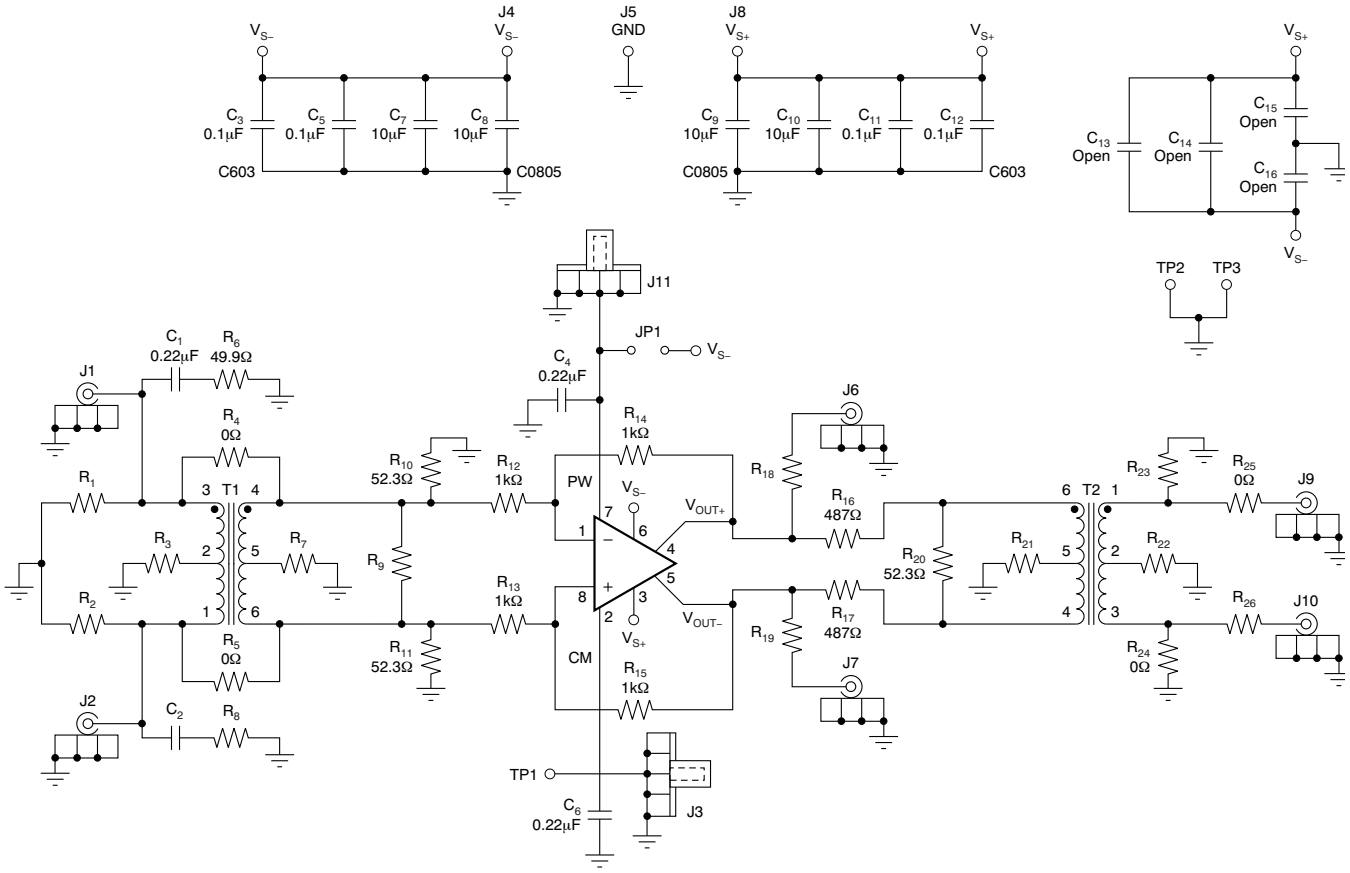

Figure 77. THS4521EVM: Schematic

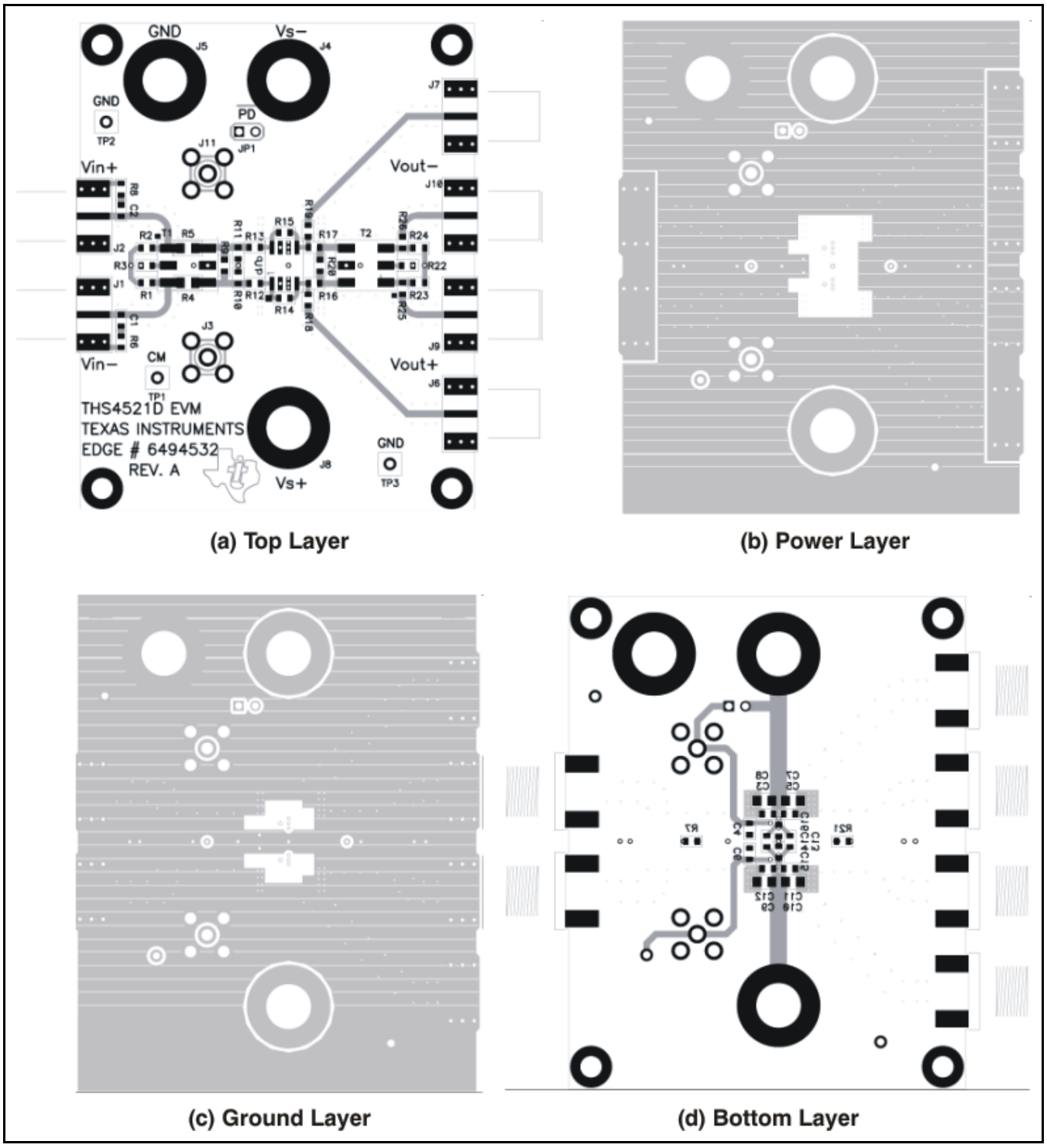

Figure 78. THS4521EVM: Layer 1 to Layer 4 Images

Table 6. THS4521EVM Parts List

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	QTY	MANUFACTURER PART NUMBER
1	Capacitor, 10.0 µF, ceramic, X5R, 6.3 V	0805	C7, C8, C9, C10	4	(AVX) 08056D106KAT2A
2	Capacitor, 0.1 µF, ceramic, X7R, 16 V	0603	C3, C5, C11, C12	4	(AVX) 0603YC104KAT2A
3	Capacitor, 0.22 µF, ceramic, X7R, 10 V	0603	C1, C4, C6	3	(AVX) 0603ZC224KAT2A
4	Open	0603	C2, C13, C14, C15, C16	5	
5	Open	0603	R1, R2, R3, R7, R8, R9, R18, R19, R21, R22, R23, R26	12	
6	Resistor, 0 Ω	0603	R24, R25	2	(ROHM) MCR03EZPJ000
7	Resistor, 49.9 Ω, 1/10W, 1%	0603	R6	1	(ROHM) MCR03EZPFX49R9
8	Resistor, 52.3 Ω, 1/10W, 1%	0603	R10, R11, R20	3	(ROHM) MCR03EZPFX52R3
9	Resistor, 487 Ω, 1/10W, 1%	0603	R16, R17	2	(ROHM) MCR03EZPFX4870
10	Resistor, 1k Ω, 1/10W, 1%	0603	R12, R13, R14, R15	4	(ROHM) MCR03EZPFX1001
11	Resistor, 0 Ω	0805	R4, R5	2	(ROHM) MCR10EZPJ000
12	Open		T1	1	
13	Transformer, RF		T2	1	(MINI-CIRCUITS) ADT1-1WT
14	Jack, Banana receptance, 0.25-in dia. hole		J4, J5, J8	3	(SPC) 813
15	Open		J1, J3, J6, J7, J10, J11	6	
16	Connector, edge, SMA PCB jack		J2, J9	2	(JOHNSON) 142-0701-801
17	Header, 0.1 in CTRS, 0.025-in sq. pins	2 POS.	JP1	1	(SULLINS) PBC36SAAN
18	Shunts		JP1	1	(SULLINS) SSC02SYAN
19	Test point, Red		TP1	1	(KEYSTONE) 5000
20	Test point, Black		TP2, TP3	2	(KEYSTONE) 5001
21	IC, THS4521		U1	1	(TI) THS4521D
22	Standoff, 4-40 hex, 0.625 in length			4	(KEYSTONE) 1808
23	Screw, Phillips, 4-40, .250 in			4	SHR-0440-016-SN
24	Board, printed circuit			1	(TI) EDGE# 6494532

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Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3 V to 5.5 V and the output voltage range of 3 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March, 2009) to Revision B **Page**

- Corrected ordering number for THS4522 large tape and reel 2

Changes from Original (December, 2008) to Revision A **Page**

- Changed device status of THS4524 from product preview to production data 1
- Changed power-supply voltage range from +3 V (1.5 V) to +2.5 V (1.25 V) 1
- Revised channel-to-channel crosstalk specifications (3.3 V) 3
- Changed specified operating voltage (3.3 V) from 3 V (minimum) to 2.5 V (minimum) 4
- Revised channel-to-channel crosstalk specifications (5 V) 5
- Changed specified operating voltage (5 V) from 3 V (minimum) to 2.5 V (minimum) 6
- Updated Figure 18 (THS4522, THS4524 Crosstalk) 14
- Updated Figure 44 (THS4522, THS4524 Crosstalk) 19
- Added *Typical Performance Variation with Supply Voltage* section 26
- Changed title of *Single-Supply Operation* section 26
- Added sentence regarding use of Figure 68 to measure crosstalk between channels of THS4522 and THS4524 to *Audio Performance* section 29
- Corrected device name error in EVM schematic 32

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
THS4521ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4521IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4521IDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4521IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4522IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4522IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4524IDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4524IDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

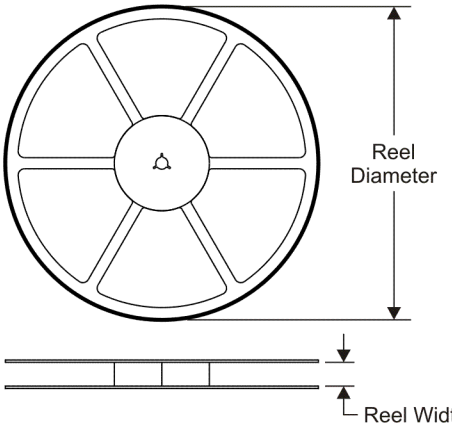
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

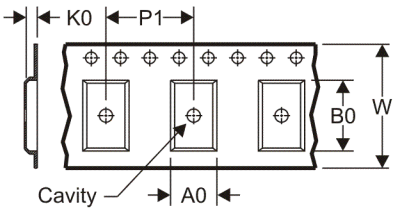
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

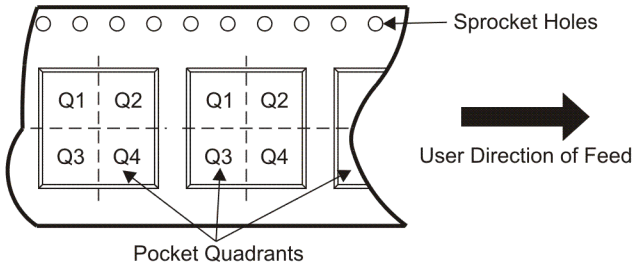


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

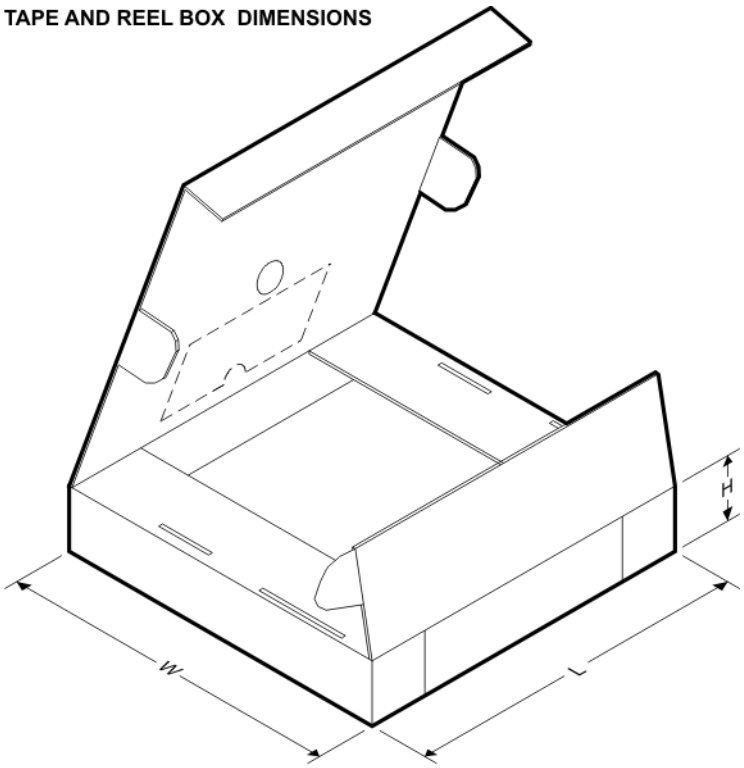
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4521IDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4521IDGKT	MSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4521IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4522IPWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
THS4524IDBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

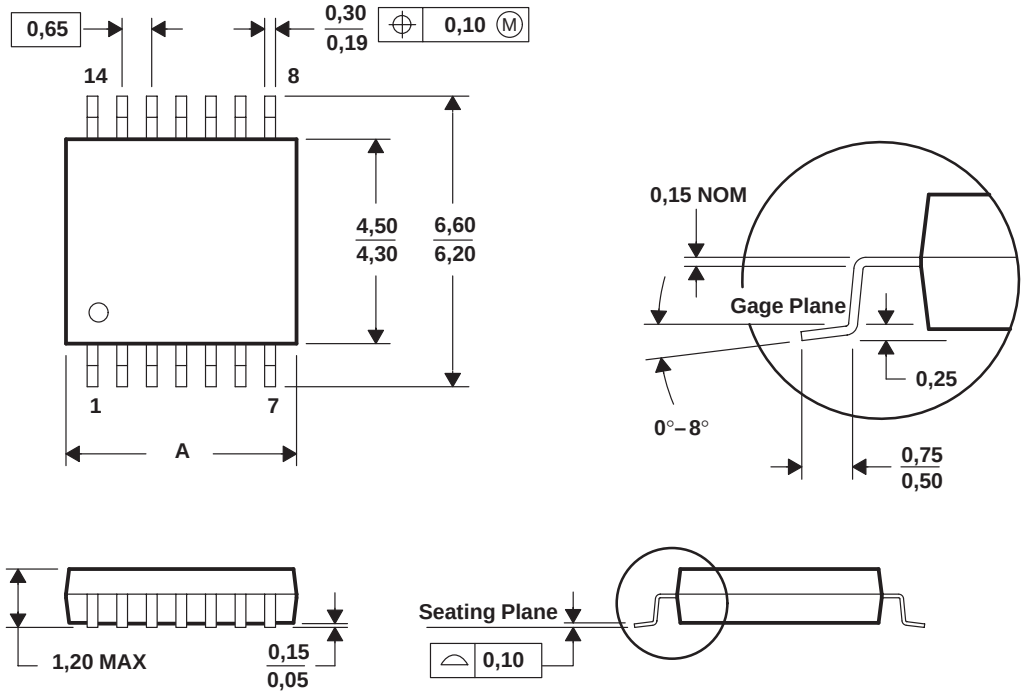


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4521IDGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
THS4521IDGKT	MSOP	DGK	8	250	190.5	212.7	31.8
THS4521IDR	SOIC	D	8	2500	346.0	346.0	29.0
THS4522IPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
THS4524IDBTR	TSSOP	DBT	38	2000	346.0	346.0	33.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

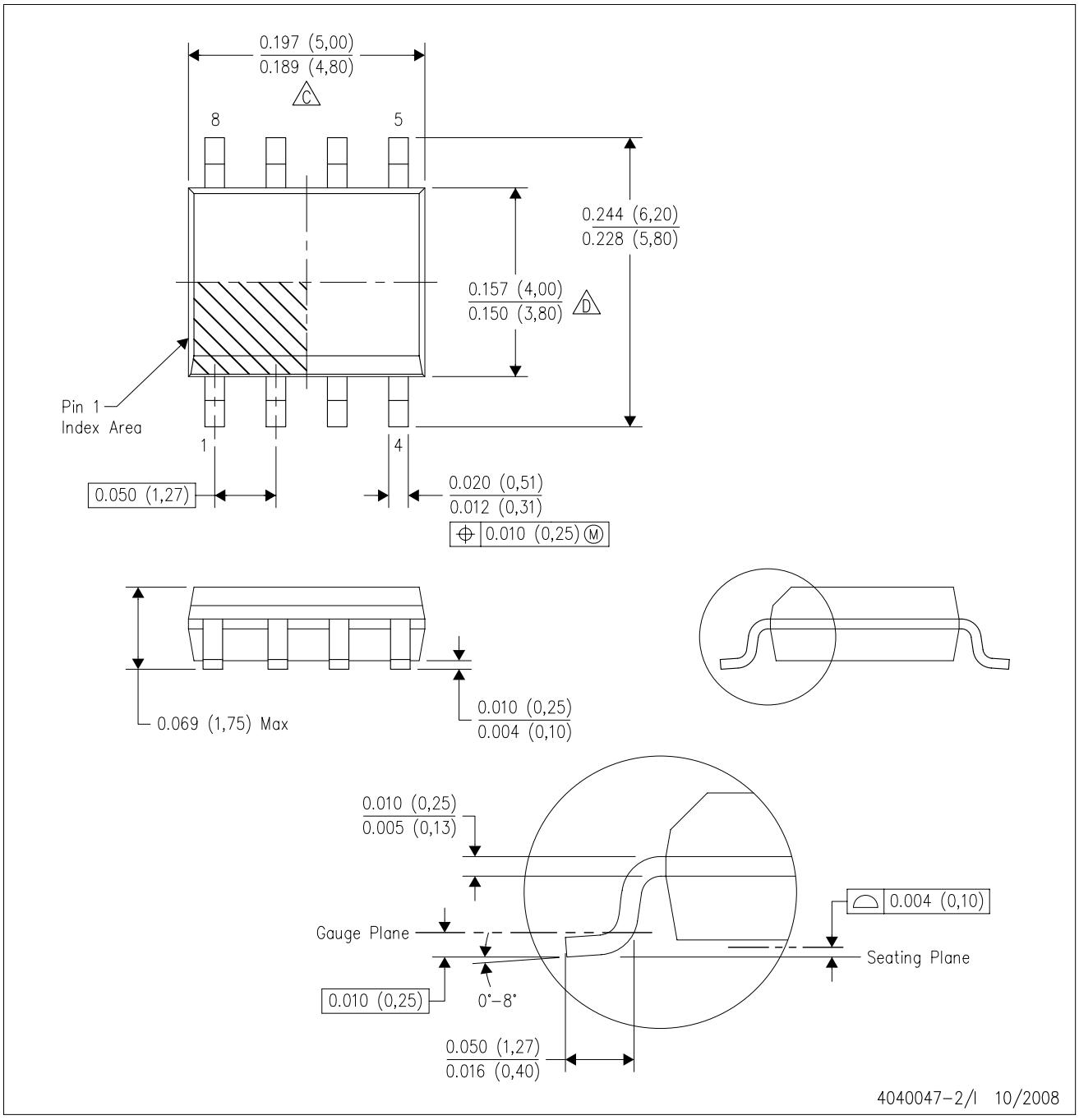


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

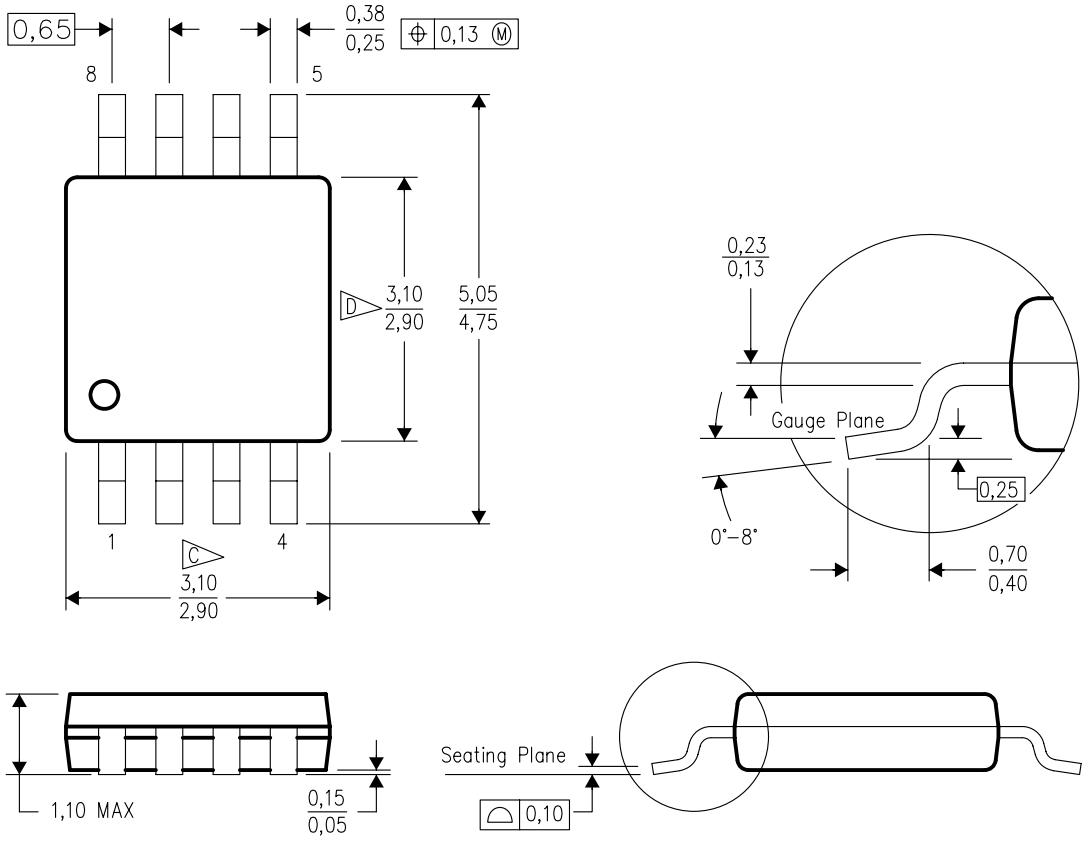
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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