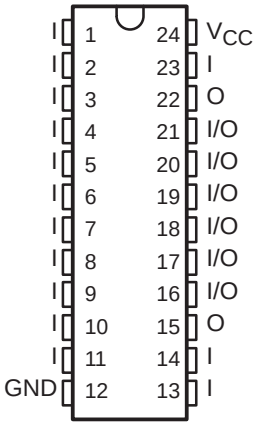
TIBPAL20L8-25C, TIBPAL20R4-25C, TIBPAL20R6-25C, TIBPAL20R8-25C
LOW-POWER HIGH-PERFORMANCE *IMPACT* ™ *PAL*® CIRCUITS

SRPS022 – D2920, MAY 1987 – REVISED MARCH 1992

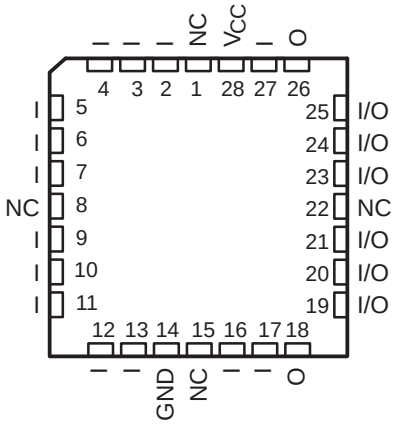
- **Low-Power, High-Performance**
  - **Reduced I_{CC} of 105 mA Max**
  - **f_{max}:**
    - **Without Feedback . . . 33 MHz Min**
    - **With Feedback . . . 25 MHz Min**
  - **t_{pd} . . . 25 ns Max**
- **Direct Replacement for PAL20L8A, PAL20R4A, PAL20R6A, PAL20L8A, with at Least 50% Reduction in Power**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Plastic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORT S
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L8'
FN PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

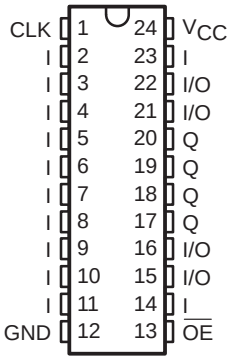
These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest AdvancedLow-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows forquick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20' C series is characterized from 0°C to 75°C.

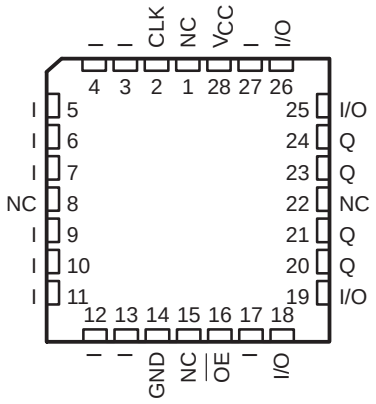
TIBPAL20R4'
JT OR NT PACKAGE

(TOP VIEW)



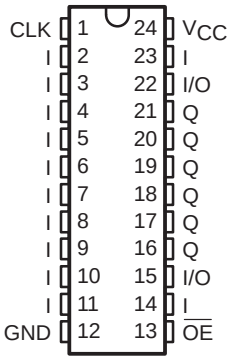
TIBPAL20R4'
FN PACKAGE

(TOP VIEW)



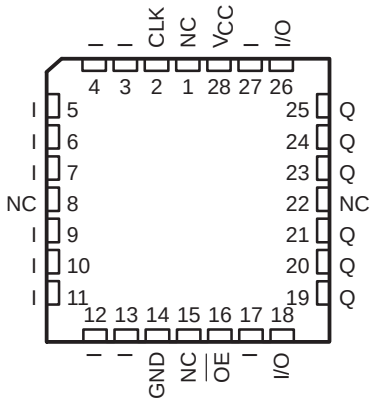
TIBPAL20R6'
JT OR NT PACKAGE

(TOP VIEW)



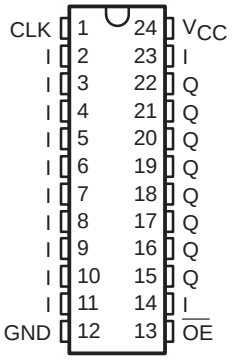
TIBPAL20R6'
FN PACKAGE

(TOP VIEW)



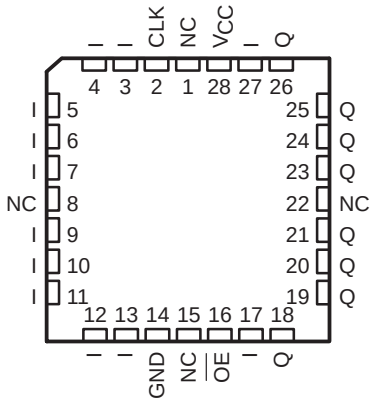
TIBPAL20R8'
JT OR NT PACKAGE

(TOP VIEW)



TIBPAL20R8'
FN PACKAGE

(TOP VIEW)

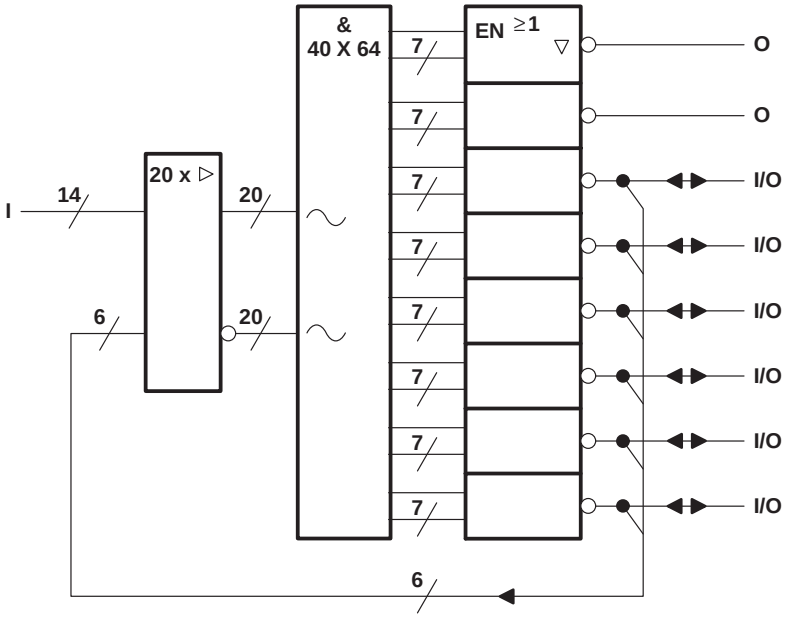


Pin assignments in operating mode

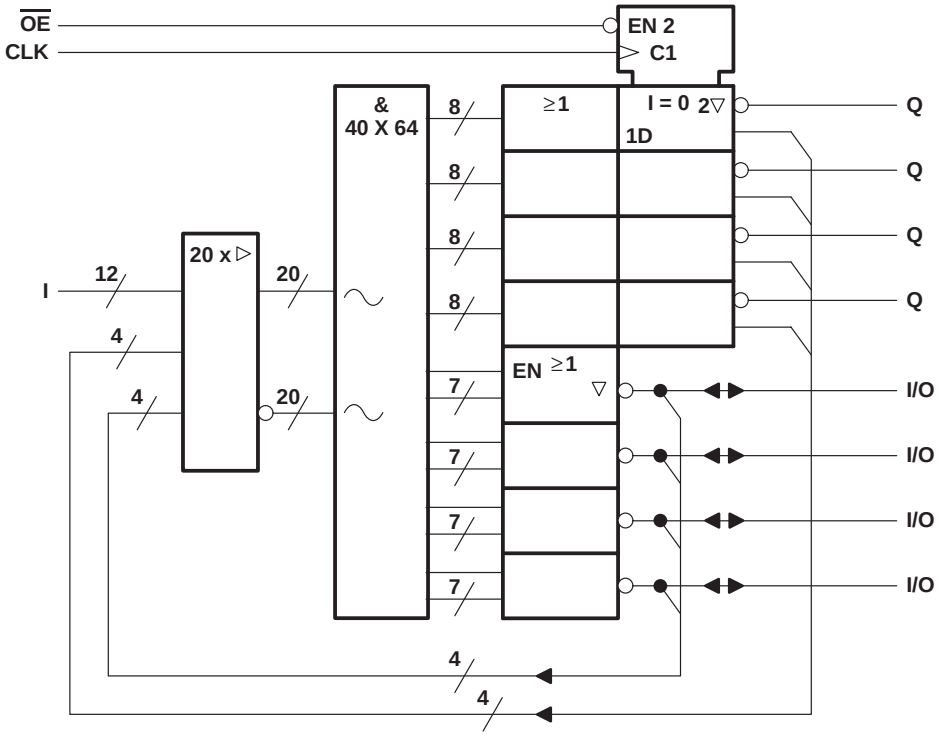
NC — No internal connection

functional block diagrams (positive logic)

TIBPAL20L8'



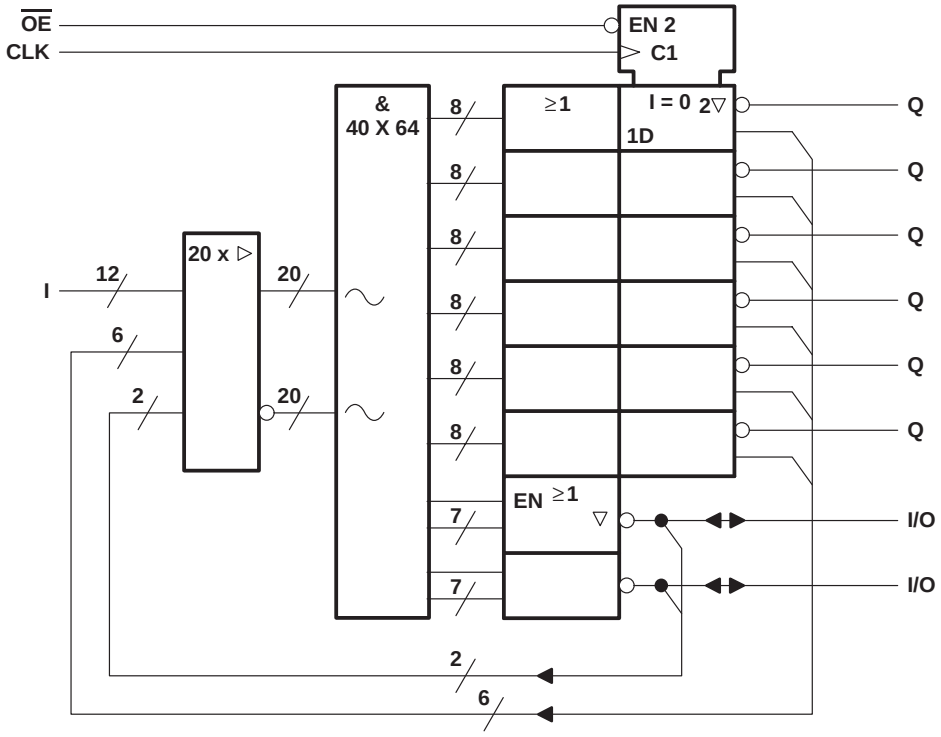
TIBPAL20R4'



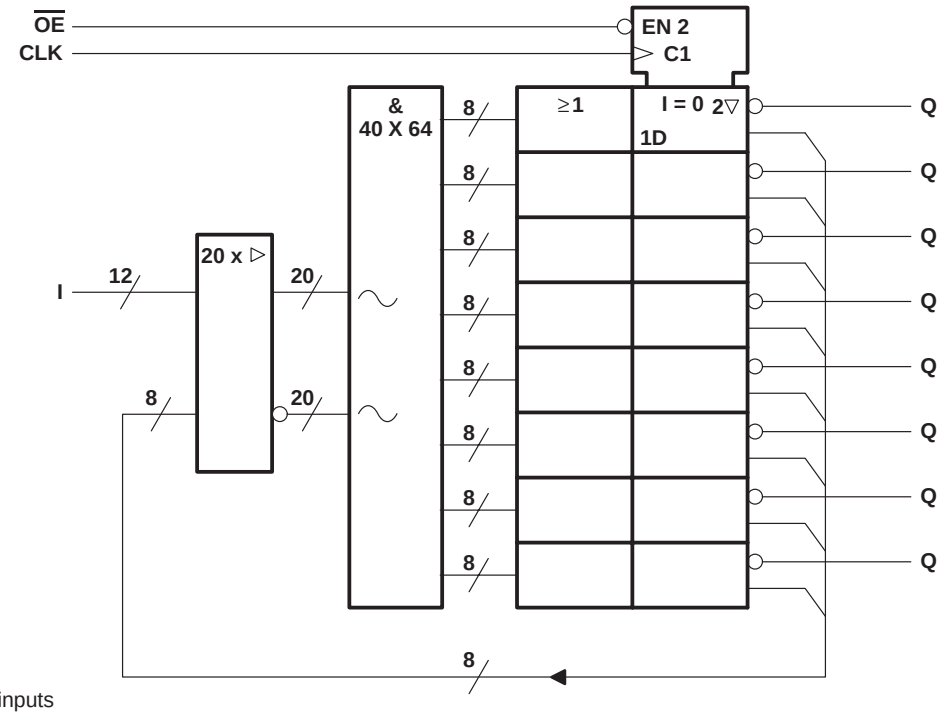
denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'

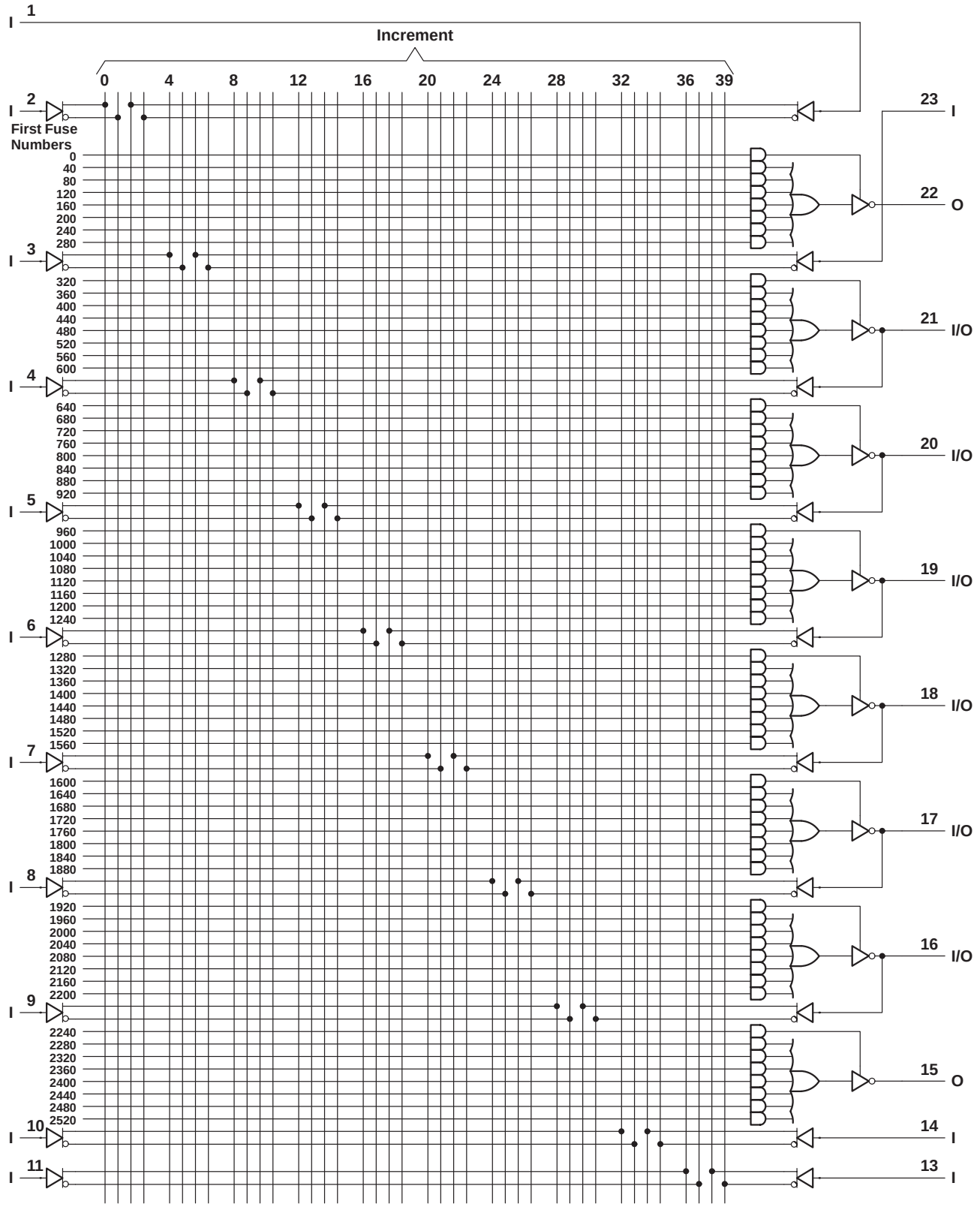


TIBPAL20R8'



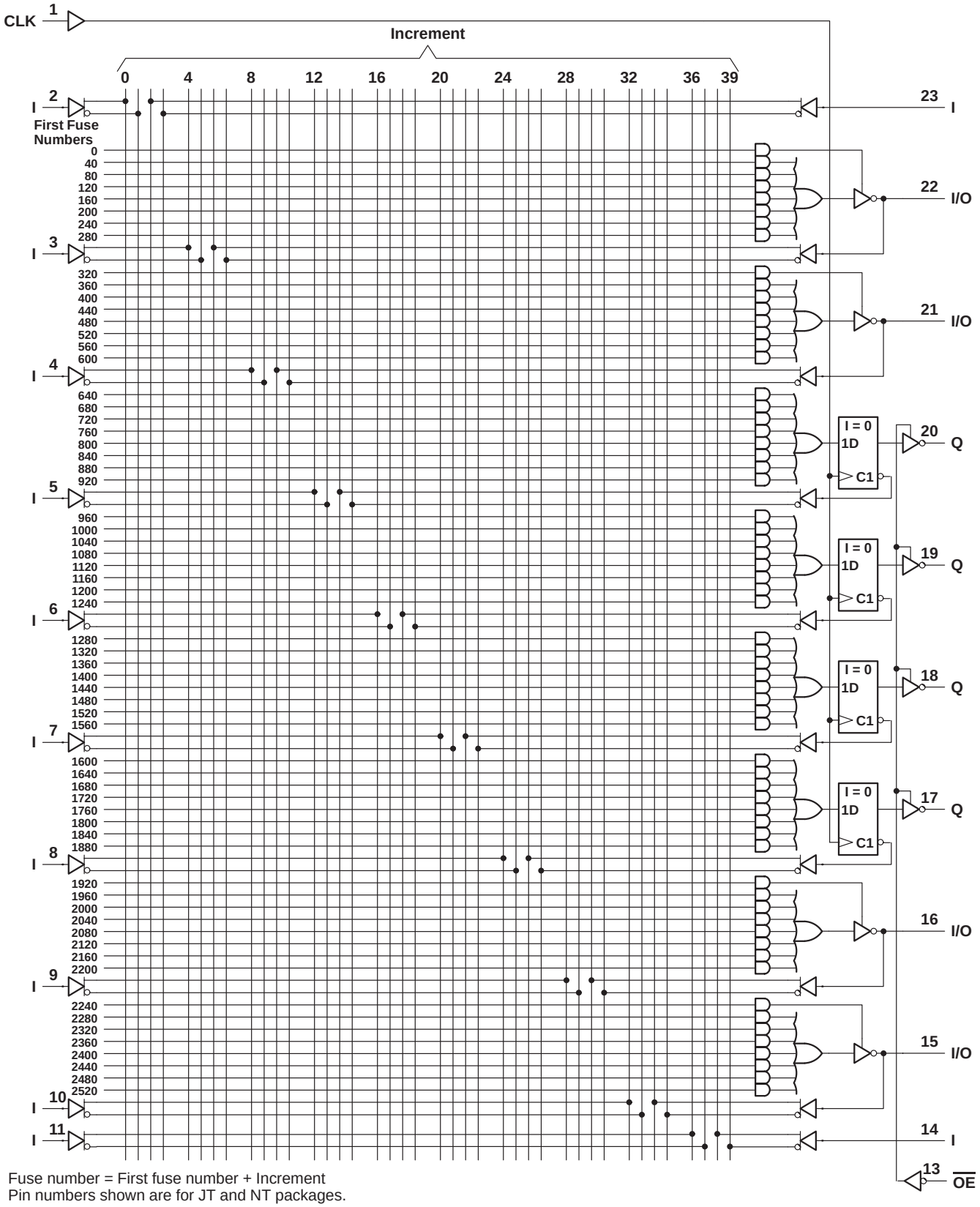
denotes fused inputs

logic diagram (positive logic)



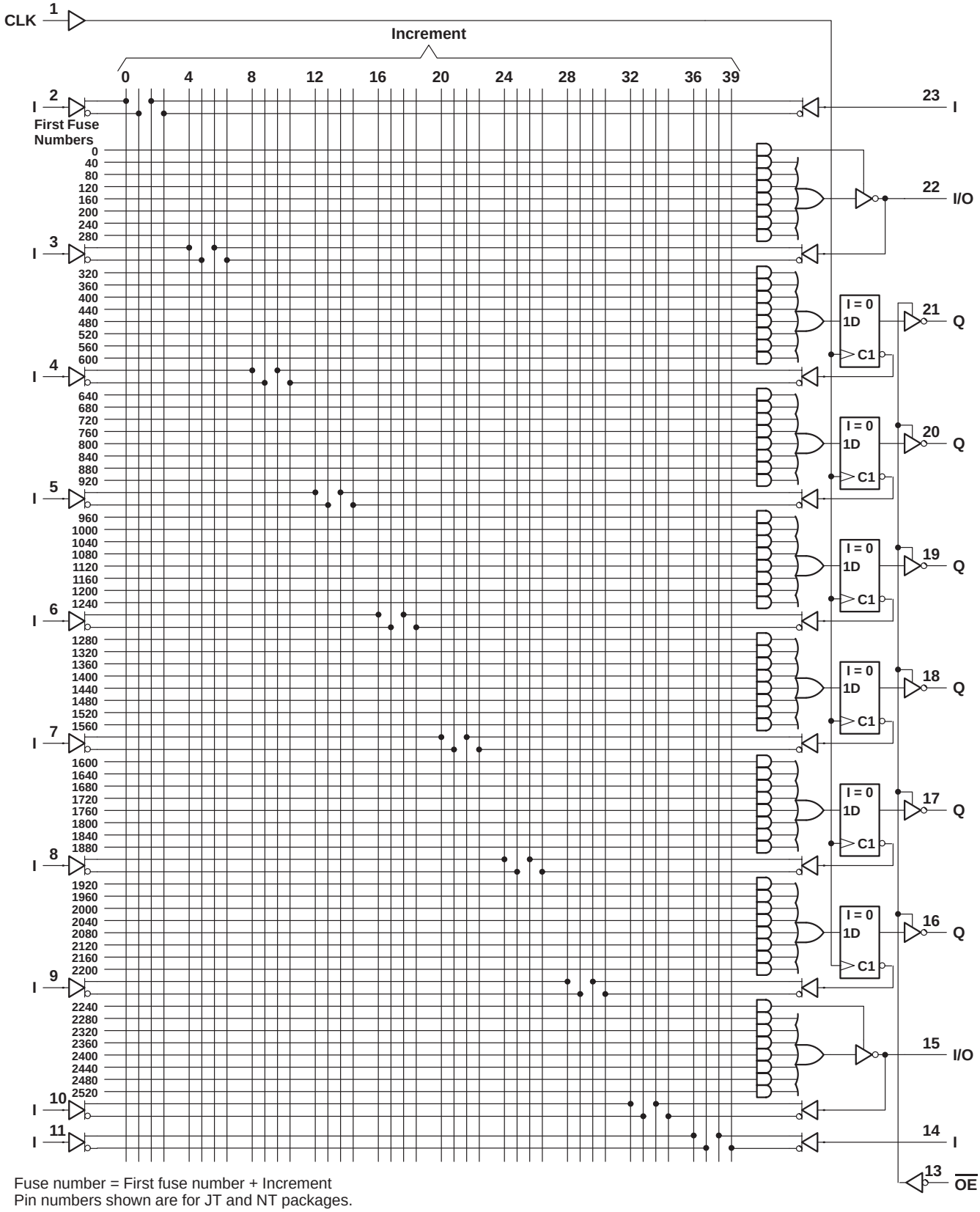
Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



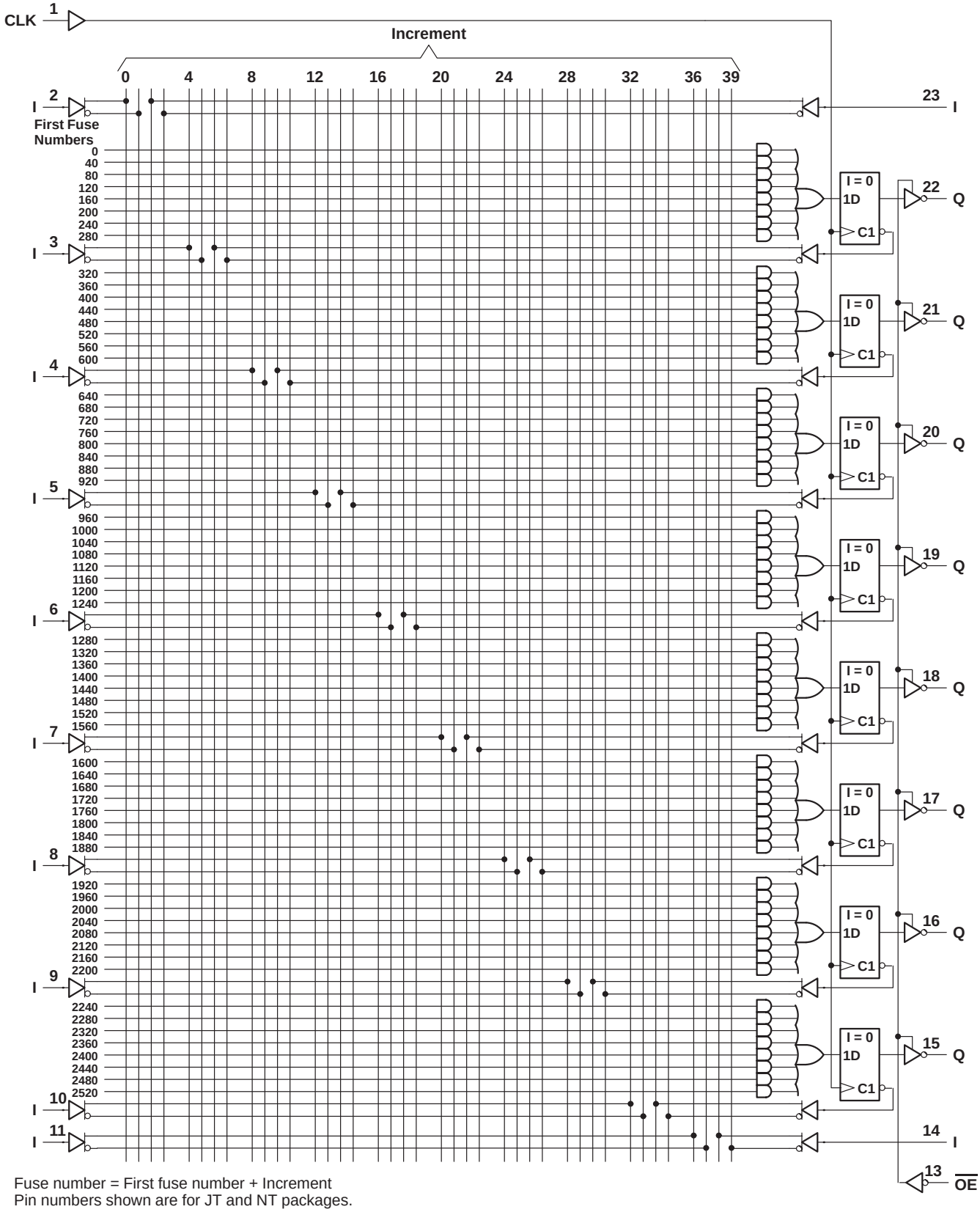
Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}†	Clock frequency		0		33	MHz
t_w†	Pulse duration, clock	High	15			ns
		Low	15			
t_{su}†	Setup time, input or feedback before clock↑		25			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

† f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA		–0.8	–1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA	2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V,	V_O = 2.7 V			20	μA
	I/O ports					100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V,	V_O = 0.4 V			–20	μA
	I/O ports					–250	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}‡		V_{CC} = 5.25 V,	V_I = 0.4 V			–0.25	mA
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0	–30	–70	–130	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open,	V_I = 0, $\overline{OE}$ at V_{IH}		75	105	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}¶	With feedback			25	40		MHz
	Without feedback			33	50		
t_{pd}	I, I/O	O, I/O	R1 = 200 Ω,	3	14	25	ns
t_{pd}	CLK↑	Q	R2 = 390 Ω,	2	10	15	ns
t_{en}	$\overline{OE}$	Q	See Figure 3	2	8	15	ns
t_{dis}	$\overline{OE}$↑	Q		2	8	15	ns
t_{en}	I, I/O	O, I/O		3	15	25	ns
t_{dis}	I, I/O	O, I/O		3	15	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
¶ $f_{max}(\text{with feedback}) = \frac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, $f_{max}(\text{without feedback}) = \frac{1}{t_w\ \text{high} + t_w\ \text{low}}$,
f_{max} does not apply for TIBPAL20L8,.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

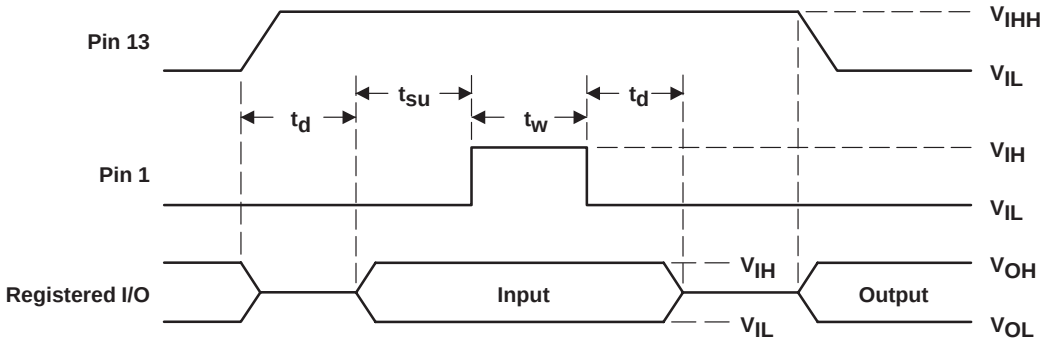
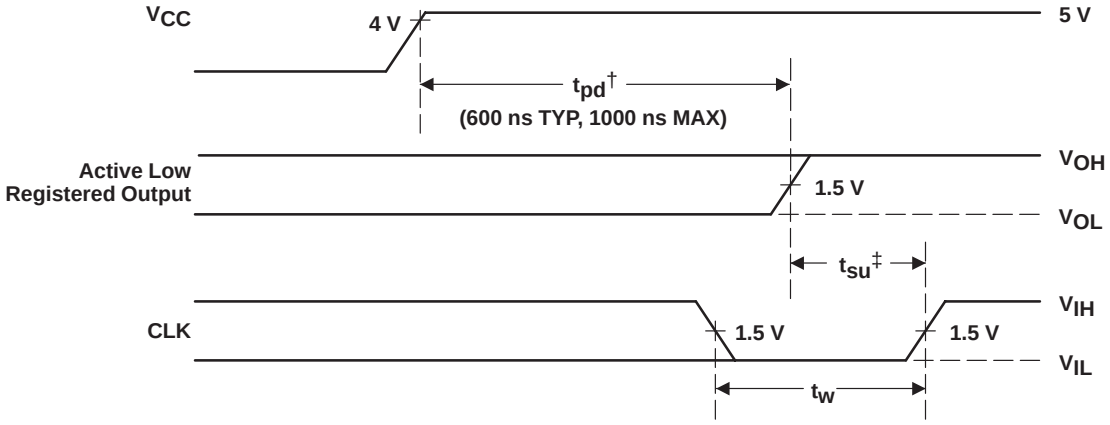


Figure 1. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

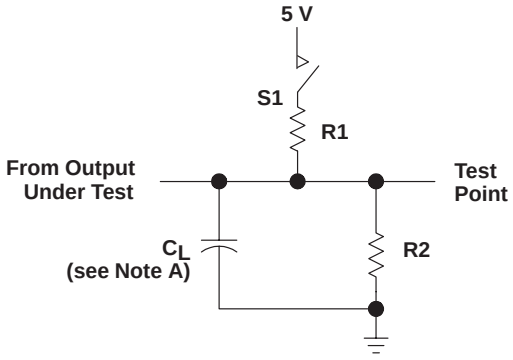
Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



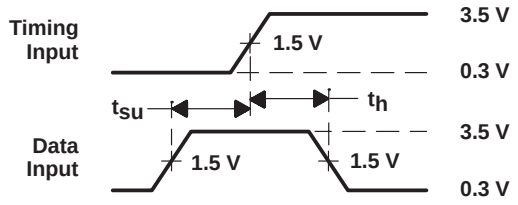
† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

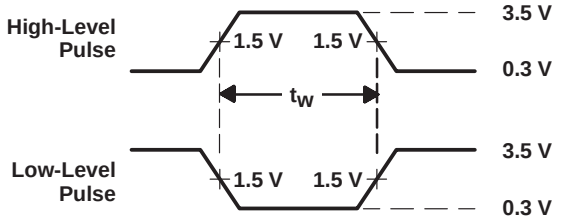
PARAMETER MEASUREMENT INFORMATION



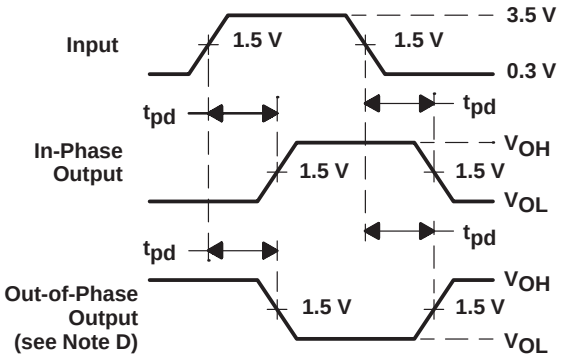
LOAD CIRCUIT FOR 3-STATE OUTPUTS



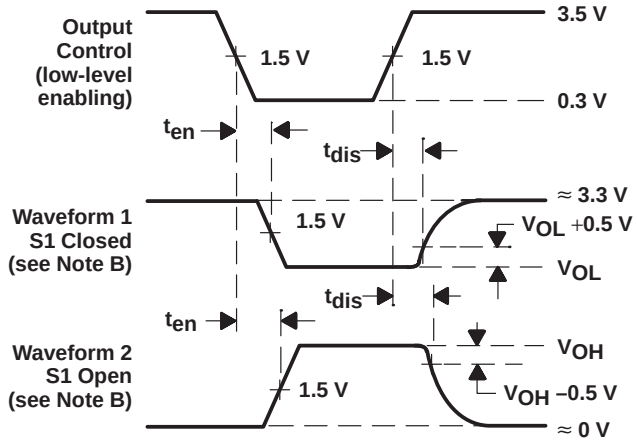
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

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