查询TISP1082供应商 捷多邦，专业PCB打样工厂，24小时加急出货

TISP1082
DUAL ASYMMETRICAL TRANSIENT VOLTAGE SUPPRESSORS

Copyright © 1997, Power Innovations Limited, UK

NOVEMBER 1986 - REVISED SEPTEMBER 1997

TELECOMMUNICATION SYSTEM SECONDARY PROTECTION

- **Ion-Implanted Breakdown Region**
  Precise and Stable Voltage
  Low Voltage Overshoot under Surge

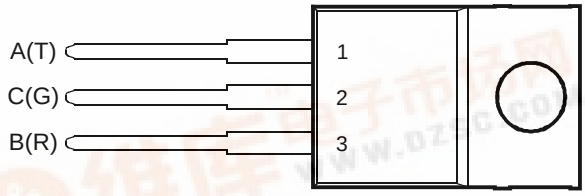
DEVICE	$V_{(Z)}$ V	$V_{(BO)}$ V
'1082	- 58	- 82

- **Planar Passivated Junctions**
  Low Off-State Current < 10 µA
- **Rated for International Surge Wave Shapes**

WAVE SHAPE	STANDARD	I_{TSP} A
8/20 µs	ANSI C62.41	150
10/160 µs	FCC Part 68	60
10/560 µs	FCC Part 68	45
0.2/310 µs	RLM 88	38
10/700 µs	FTZ R12	50
	VDE 0433	50
	CCITT IX K17/K20	50
10/1000 µs	REA PE-60	50

- **UL Recognized, E132482**

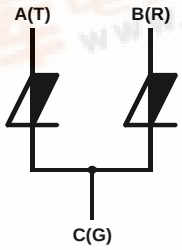
TO-220 PACKAGE
(TOP VIEW)



Pin 2 is in electrical contact with the mounting base.

MDXXANA

device symbol



description

The TISP1082 is designed specifically for telephone line card protection against lightning and transients induced by a.c. power lines. These devices will supress voltage transients between terminals A and C, B and C, and A and B.

Negative transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents d.c. latchup as the transient subsides. Positive transients are clipped by diode action.

These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and matched breakover control and are virtually transparent to the system in normal operation.

Information is current as of publication date. Products conform to specifications in accordance with the terms of Power Innovations standard warranty. Production processing does not necessarily include testing of all parameters.

Power INNOVATIONS

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Non-repetitive peak on-state pulse current (see Notes 1, 2 and 3)			
8/20 µs (ANSI C62.41, open-circuit voltage wave shape 1.2/50 µs)		150	
10/160 µs (FCC Part 68, open-circuit voltage wave shape 10/160 µs)		60	
5/200 µs (VDE 0433, open-circuit voltage wave shape 2 kV, 10/700 µs)		50	
0.2/310 µs (RLM 88, open-circuit voltage wave shape 1.5 kV, 0.5/700 µs)	I_{TSP}	38	A
5/310 µs (CCITT IX K17/K20, open-circuit voltage wave shape 2 kV, 10/700 µs)		50	
5/310 µs (FTZ R12, open-circuit voltage wave shape 2 kV, 10/700 µs)		50	
10/560 µs (FCC Part 68, open-circuit voltage wave shape 10/560 µs)		45	
10/1000 µs (REA PE-60, open-circuit voltage wave shape 10/1000 µs)		50	
Non-repetitive peak on-state current, 50 Hz, 2.5 s (see Notes 1 and 2)	I_{TSM}	10	A rms
Initial rate of rise of on-state current, Linear current ramp, Maximum ramp value < 38 A	di_T/dt	250	A/µs
Junction temperature	T_J	150	°C
Operating free - air temperature range		0 to 70	°C
Storage temperature range	T_{stg}	-40 to +150	°C
Lead temperature 1.5 mm from case for 10 s	T_{lead}	260	°C

NOTES: 1. Above 70°C, derate linearly to zero at 150°C case temperature
2. This value applies when the initial case temperature is at (or below) 70°C. The surge may be repeated after the device has returned to thermal equilibrium.
3. Most PTT's quote an unloaded voltage waveform. In operation the TISP essentially shorts the generator output. The resulting loaded current waveform is specified.

.

electrical characteristics for the A and B terminals, T_J = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_Z	Reference zener voltage	$I_Z = \pm 1$mA			± 58			V
I_D	Off-state leakage current	$V_D = \pm 50$ V					± 10	µA
C_{off}	Off-state capacitance	$V_D = 0$	f = 1 kHz	(see Note 4)		1	5	pF

NOTE 4: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The third terminal is connected to the guard terminal of the bridge.

electrical characteristics for the A and C or the B and C terminals, T_J = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_Z	Reference zener voltage	I_Z = - 1mA			- 58			V
α_{V_Z}	Temperature coefficient of reference voltage					0.1		%/°C
$V_{(BO)}$	Breakover voltage	(see Notes 5 and 6)					- 82	V
$I_{(BO)}$	Breakover current	(see Note 5)			- 0.15		- 0.6	A
V_F	Forward voltage	I_F = 5 A	(see Notes 5 and 6)				3	V
V_{TM}	Peak on-state voltage	I_T = - 5 A	(see Notes 5 and 6)			- 2.2	- 3	V
I_H	Holding current	(see Note 5)			- 150			mA
dv/dt	Critical rate of rise of off-state voltage	(see Note 7)					- 5	kV/µs
I_D	Off-state leakage current	V_D = - 50 V					- 10	µA
C_{off}	Off-state capacitance	V_D = 0	f = 1 kHz	(see Note 4)		300	500	pF

NOTES: 5. These parameters must be measured using pulse techniques, t_w = 100 µs, duty cycle ≤ 2%.
6. These parameters are measured with voltage sensing contacts seperate from the current carrying contacts located within 3.2 mm (0.125 inch) from the device body.
7. Linear rate of rise, maximum voltage limited to 80 % V_Z (minimum)..

PARAMETER MEASUREMENT INFORMATION

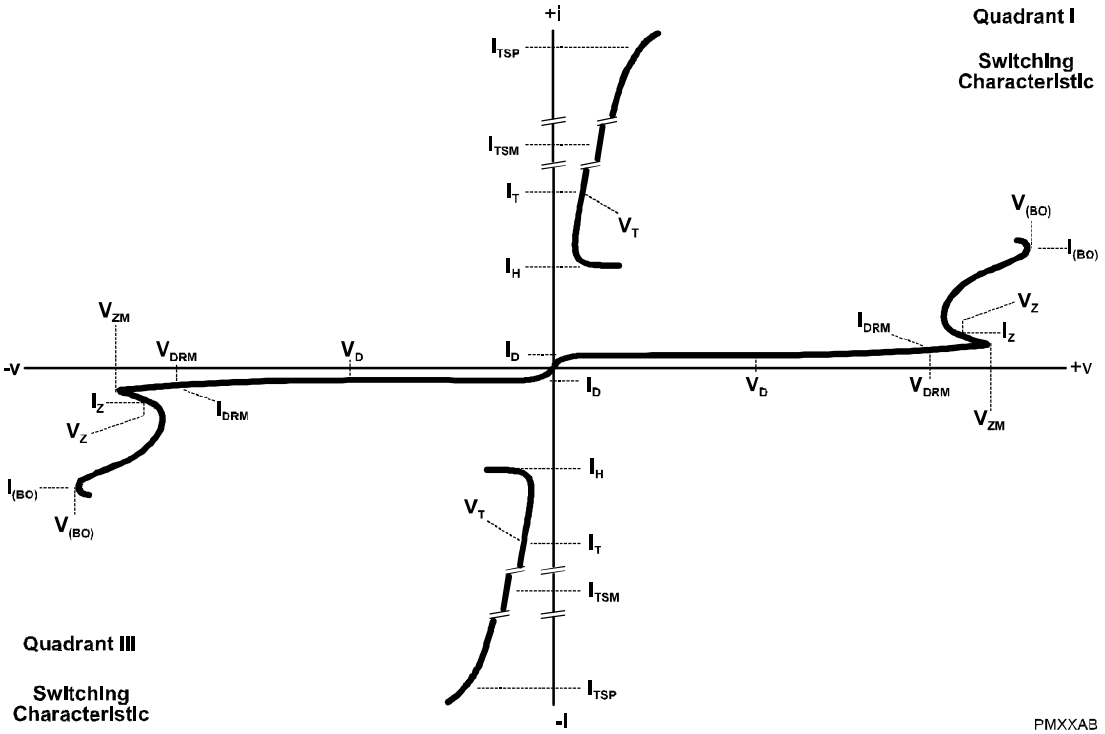


Figure 1. VOLTAGE-CURRENT CHARACTERISTIC FOR TERMINALS A AND B

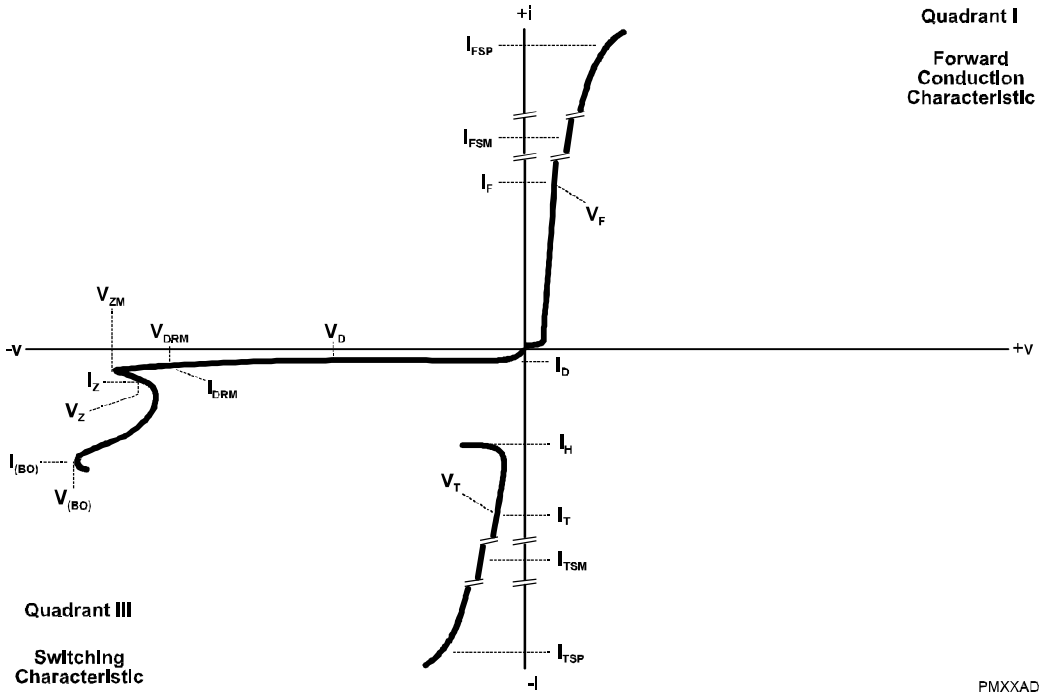


Figure 2. VOLTAGE-CURRENT CHARACTERISTIC FOR TERMINALS A AND C OR B AND C†

†Polarity is determined at terminal A or B with respect to C

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance			62.5	°C/W

TYPICAL CHARACTERISTICS
A and C, or B and C terminals

ON-STATE AND FORWARD CURRENTS vs ON-STATE AND FORWARD VOLTAGES

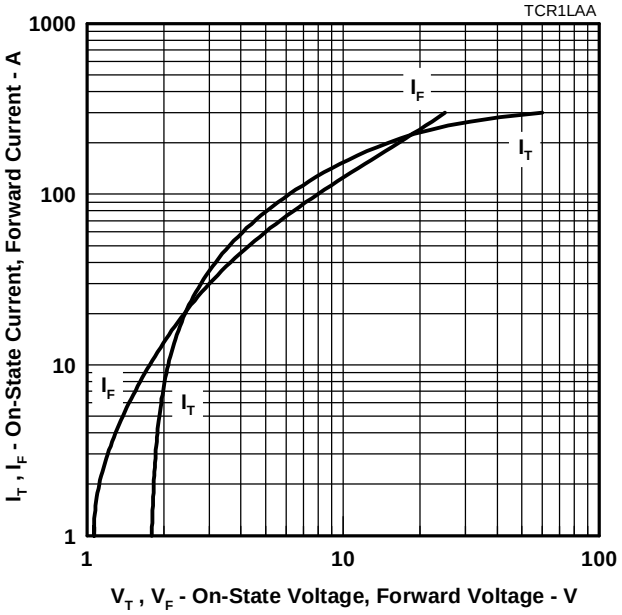


Figure 3.

ZENER AND BREAKOVER VOLTAGE vs JUNCTION TEMPERATURE

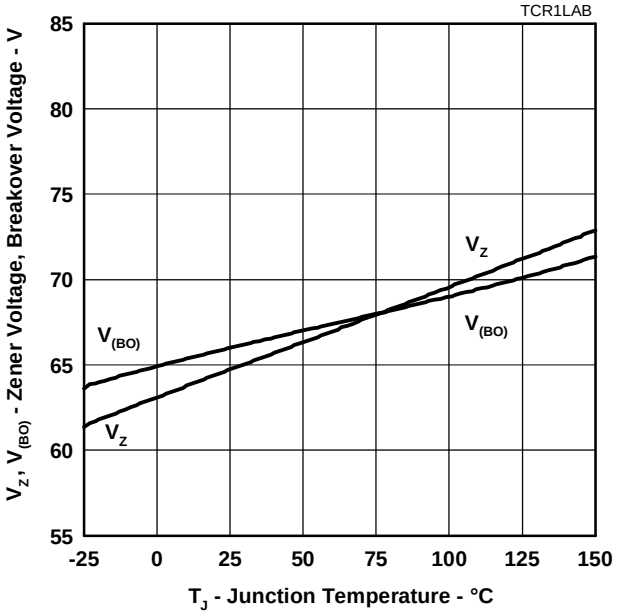


Figure 4.

TYPICAL CHARACTERISTICS
A and C, or B and C terminals

HOLDING CURRENT & BREAKOVER CURRENT vs JUNCTION TEMPERATURE

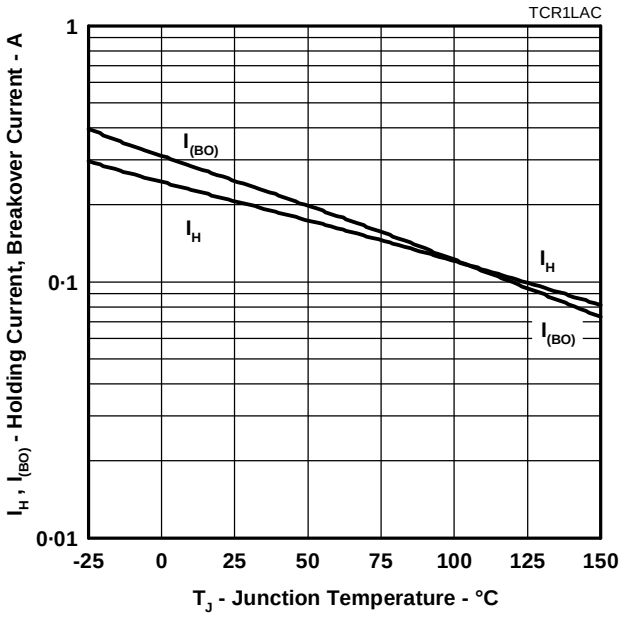


Figure 5.

OFF-STATE CURRENT vs JUNCTION TEMPERATURE

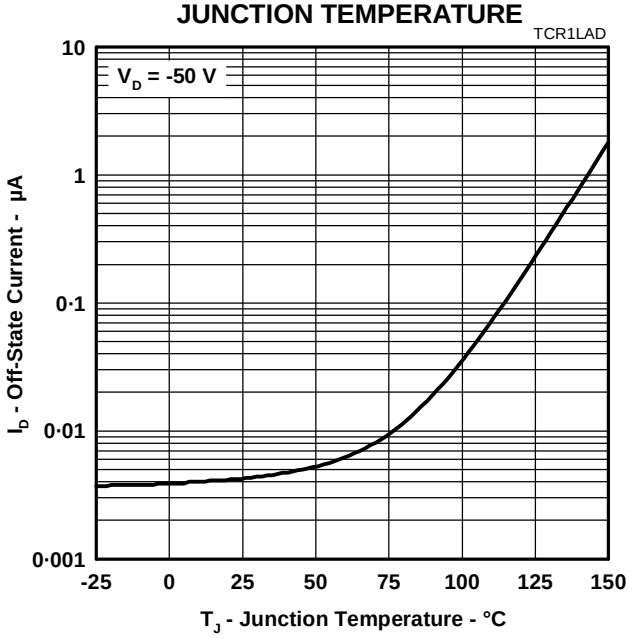


Figure 6.

ON-STATE VOLTAGE & FORWARD VOLTAGE vs JUNCTION TEMPERATURE

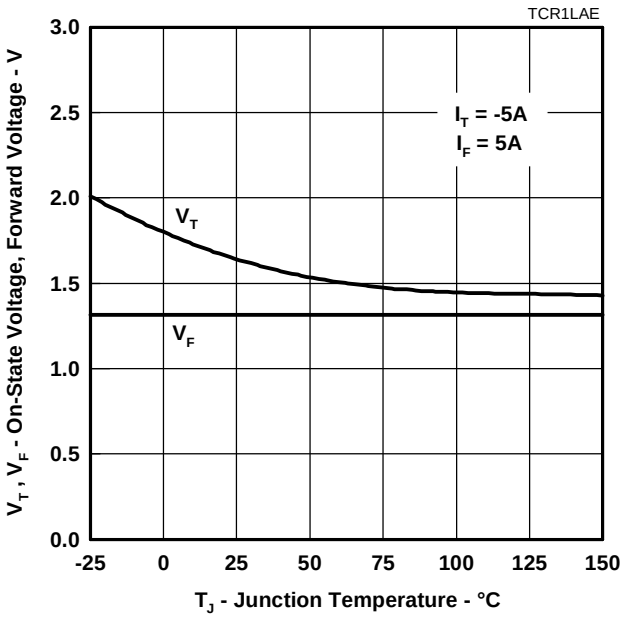


Figure 7.

NORMALISED BREAKOVER VOLTAGE vs RATE OF RISE OF PRINCIPLE CURRENT

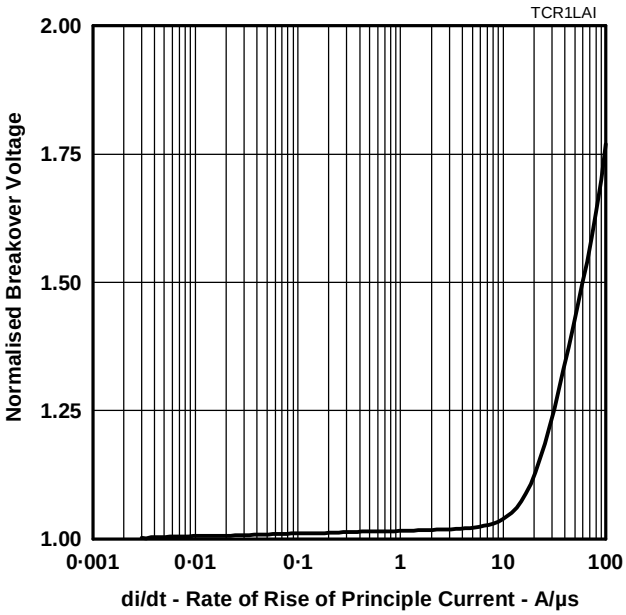


Figure 8.

TYPICAL CHARACTERISTICS
A and C, or B and C terminals

PEAK DIODE FORWARD VOLTAGE
vs
RATE OF RISE OF PRINCIPLE CURRENT

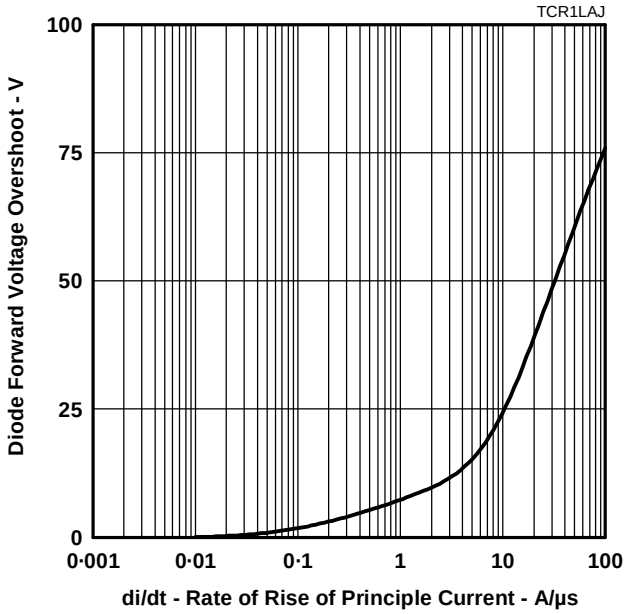


Figure 9.

OFF-STATE CAPACITANCE
vs
A OR B TERMINAL VOLTAGE (POSITIVE)

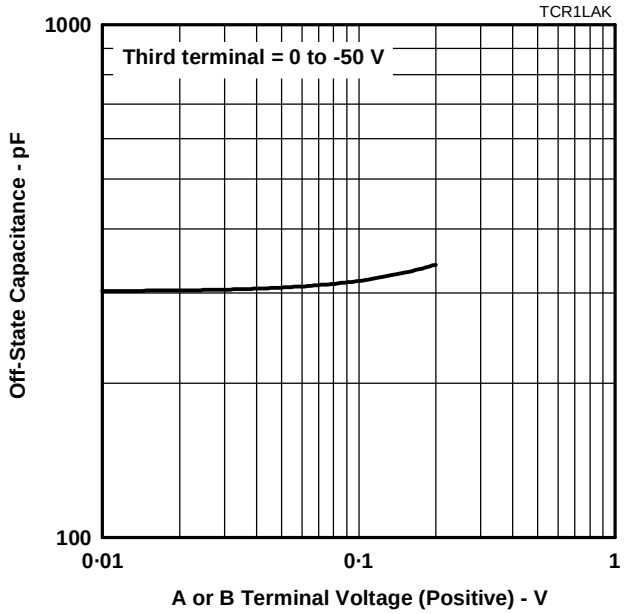


Figure 10.

OFF-STATE CAPACITANCE
vs
A OR B TERMINAL VOLTAGE (NEGATIVE)

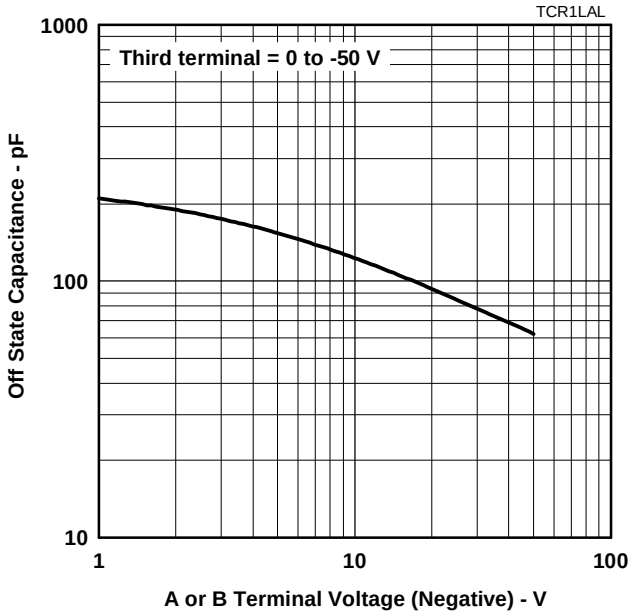


Figure 11.

TYPICAL CHARACTERISTICS
A and B terminals

ZENER VOLTAGE & BREAKOVER VOLTAGE
vs
JUNCTION TEMPERATURE

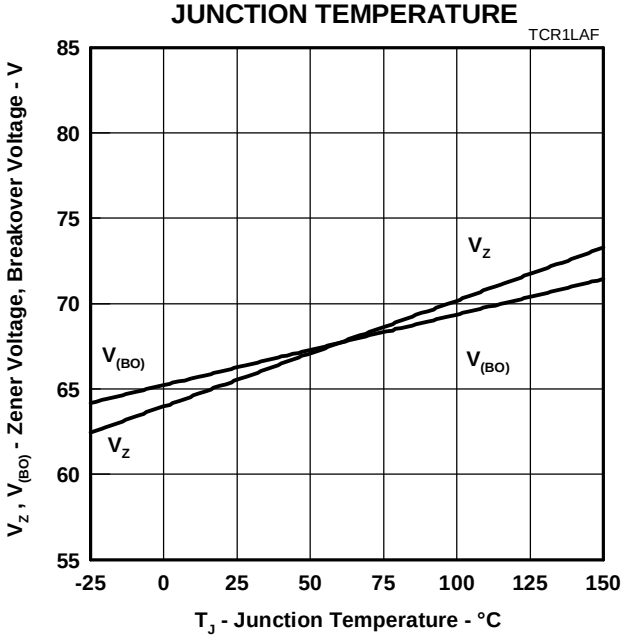


Figure 12.

HOLDING CURRENT & BREAKOVER CURRENT
vs
JUNCTION TEMPERATURE

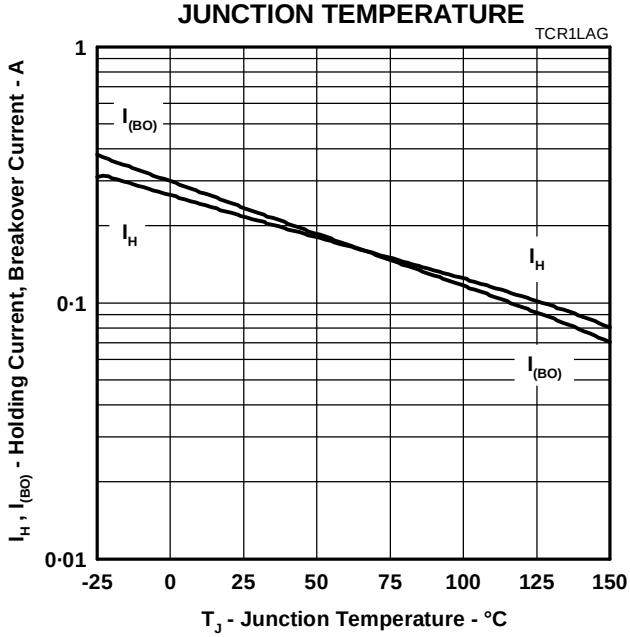


Figure 13.

OFF-STATE CURRENT
vs
JUNCTION TEMPERATURE

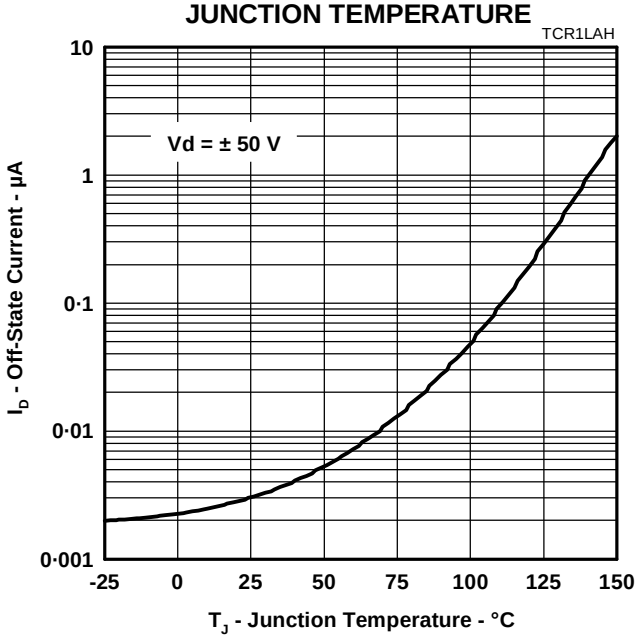


Figure 14.

TYPICAL CHARACTERISTICS
A and B terminals

OFF-STATE CAPACITANCE vs A OR B TERMINAL VOLTAGE (POSITIVE)

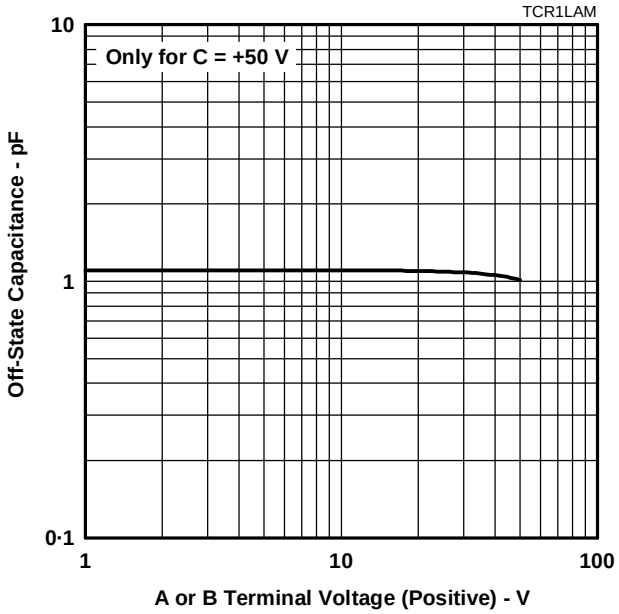


Figure 15.

OFF-STATE CAPACITANCE vs A OR B TERMINAL VOLTAGE (NEGATIVE)

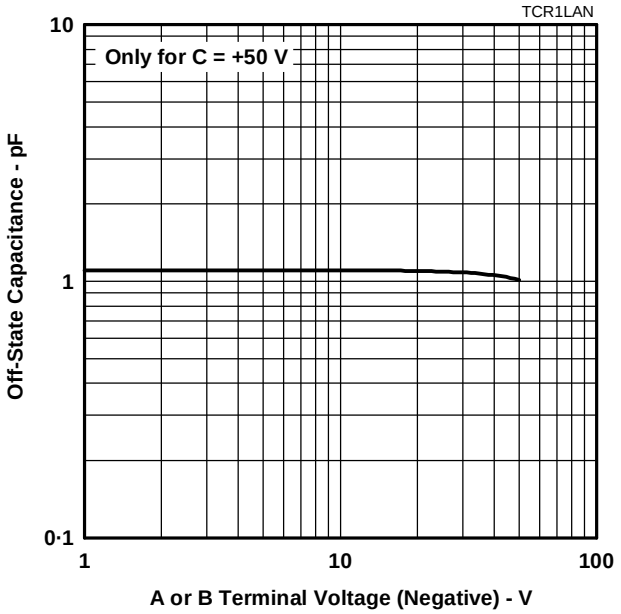


Figure 16.

SURGE CURRENT vs DECAY TIME

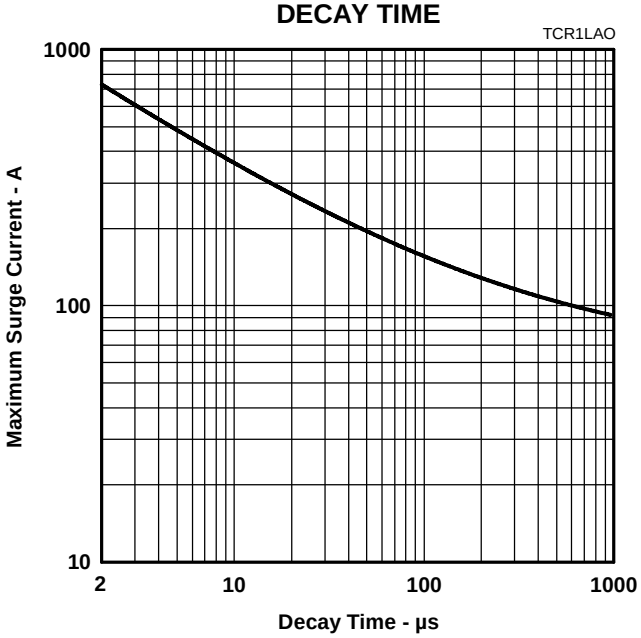


Figure 17.

THERMAL INFORMATION

THERMAL RESPONSE

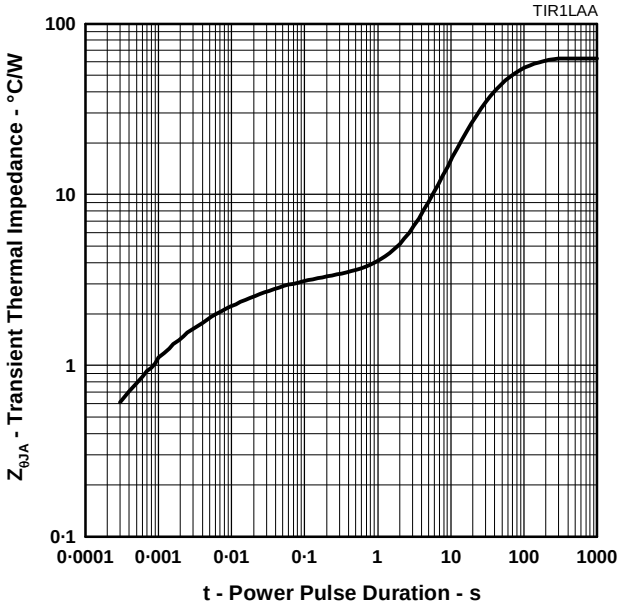


Figure 18.

MAXIMUM NON-RECURRENT 50Hz CURRENT vs CURRENT DURATION

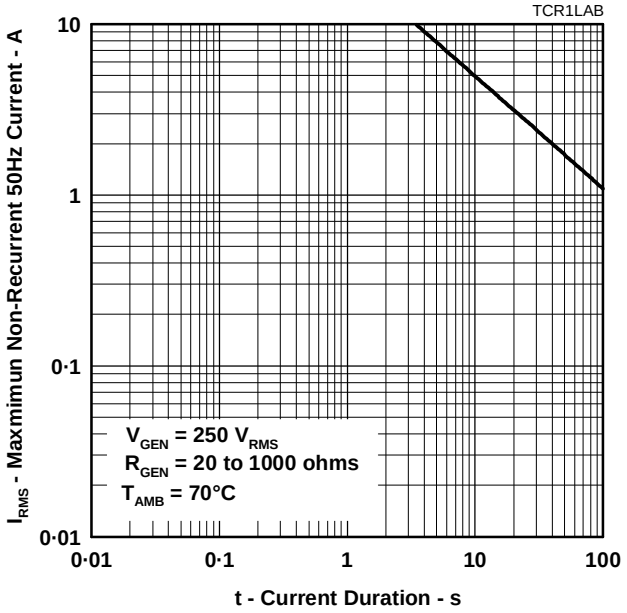


Figure 19.

FREE AIR TEMPERATURE DERATING CURVE

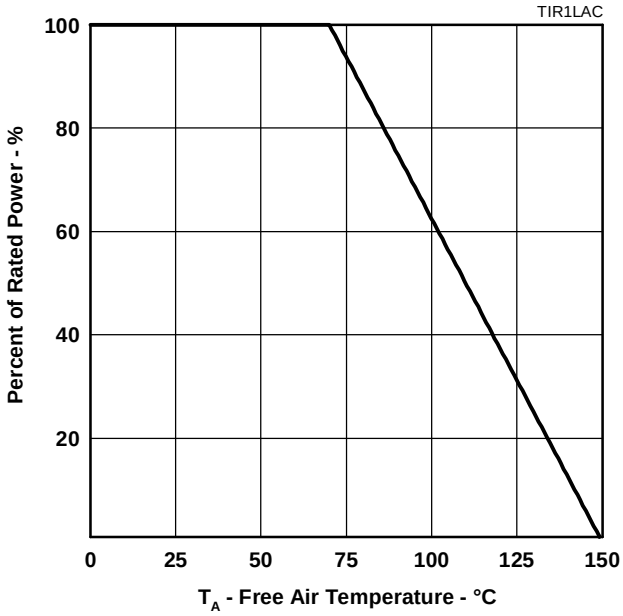


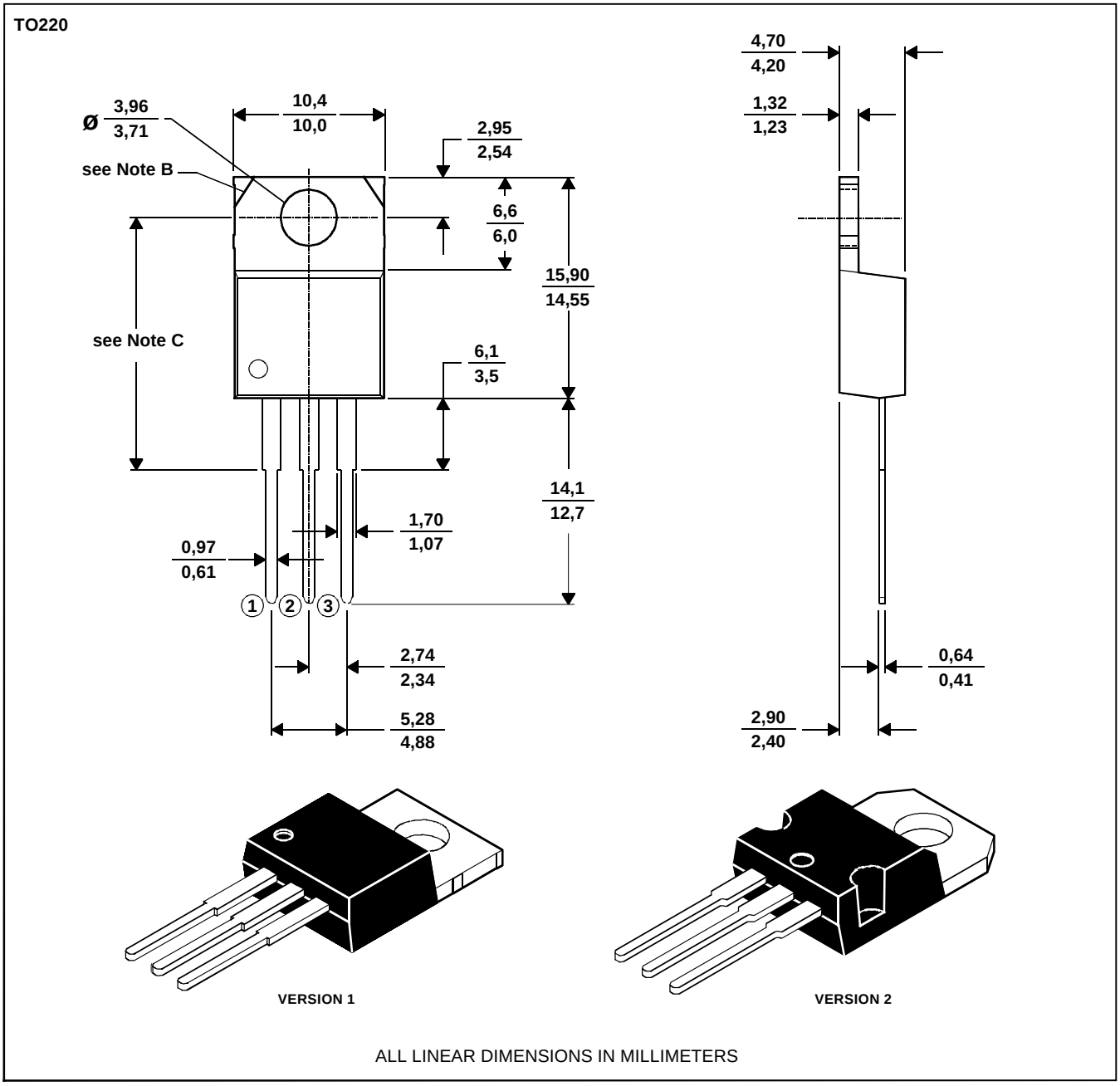
Figure 20.

MECHANICAL DATA

TO-220

3-pin plastic flange-mount package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. The centre pin is in electrical contact with the mounting tab.
B. Mounting tab corner profile according to package version.
C. Typical fixing hole centre stand off height according to package version.
Version 1, 18.0 mm. Version 2, 17.6 mm.

MDXXBE

IMPORTANT NOTICE

Power Innovations Limited (PI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to verify, before placing orders, that the information being relied on is current.

PI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with PI's standard warranty. Testing and other quality control techniques are utilized to the extent PI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except as mandated by government requirements.

PI accepts no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor is any license, either express or implied, granted under any patent right, copyright, design right, or other intellectual property right of PI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

PI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS.

Copyright © 1997, Power Innovations Limited