TOKO

TK83854

HIGH POWER FACTOR PREREGULATOR

FEATURES

- Control Boost PWM to 0.99 Power Factor
- Limit Line Current Distortion to < 5%
- Worldwide Operation without Switches
- Feed-Forward Line Regulation
- Low Noise Sensitivity
- Pin Compatible with UC2854, and UC3854 (Licensed Source)

FEATURES (CONT.)

- Low Start-Up Supply Current
- Fixed-Frequency PWM Drive
- Low-Offset Analog Multiplier/Divider
- 1 Amp Totem-Pole Gate Driver
- Precision Voltage Reference

DESCRIPTION

The TK83854 family of integrated circuits provide active power factor correction for power systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. These parts implement all the control functions necessary to build a power supply preregulator capable of optimally using available power-line current while minimizing line-current distortion. To do this, the TK83854 contains a voltage amplifier, a precision analog multiplier/divider, a current amplifier, and a fixed-frequency PWM. In addition, the TK83854 contains a power MOSFET gate driver, 7.5 V reference, line anticipator, load-enable comparator, low supply detector, and overcurrent comparator.

The TK83854 family uses average current-mode control to accomplish fixed-frequency current control with stability and low distortion. Unlike peak current-mode control, average current control accurately maintains sinusoidal line current without slope compensation.

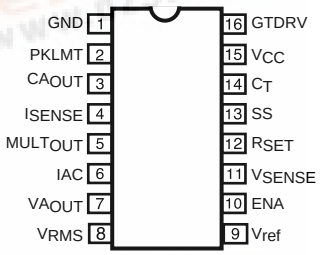
The TK83854's high reference voltage and high oscillator amplitude minimize noise sensitivity while fast PWM elements permit chopping frequencies above 200 kHz. The TK83854 can be used in systems with line voltages that vary from 75 to 275 V and with line frequencies across the 50 Hz to 400 Hz range. To reduce the burden on the circuitry that supplies power to this device, the TK83854 family features low start-up supply current.

These devices are available in 16-pin plastic dual in-line (DIP) and 16-pin surface mount (SOP) packages.

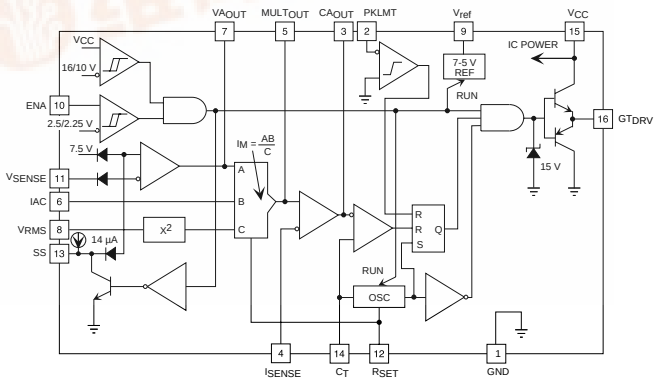
TK83854

SOP-16

DIP-16



BLOCK DIAGRAM



ORDERING INFORMATION

TK83854 □□□□

- Package Code
- Tape/Reel Code
- Extended Temp. Range

PACKAGE CODE
D: DIP-16
M: SOP-16

TEMP. RANGE (OPTIONAL)
I: -40 TO +85 °C

TAPE/REEL CODE
TL: Tape Left
MG: Magazine

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 35 V
Power Dissipation TK83854D (Note 1) ..... 1 W
Power Dissipation TK83854M (Note 2) ..... 750 mW
GTDRV Current (Continuous) ..... 0.5 A
GTDRV Current (50% Duty Cycle) ..... 1.5 A
Input Voltage ($V_{SENSE,}$ V_{RMS}) ..... 11 V
Input Voltage (ENA, I_{SENSE}, MULTOUT) ..... 11 V
Input Voltage (PKLMT) ..... 5 V
Input Voltage (IAC, R_{SET}, PKLMT) ..... 10 mA
Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range ..... 0 to +70 °C
Extended Temperature Range ..... -40 to +85 °C
Junction Temperature ..... 150 °C
Lead Soldering Temperature (10 s) ..... 235 °C

TK83854 ELECTRICAL CHARACTERISTICS

Test conditions: V_{CC} = 18 V, R_{SET} = 15 k to GND, C_T = 1.5 nF, PKLMT = 1 V, ENA = 7.5 V, V_{RMS} = 1.5 V, IAC = 100 µA, VI_{SENSE} = 0 V, $V_{OUT(CA)}$ = 3.5 V, $V_{OUT(VA)}$ = 5 V, V_{SENSE} = 7.5 V, No load on SS, CA_{OUT}, VA_{OUT}, V_{ref}, GTDRV, T_A = Operating Temperature Range, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{CC(OFF)}$	Supply Current OFF	ENA = 0 V		1.5	2.0	mA
$I_{CC(ON)}$	Supply Current ON			10	16	mA
$UVLO_{(ON)}$	V_{CC} Turn-on Threshold		14.5	16.0	17.5	V
$UVLO_{(OFF)}$	V_{CC} Turn-off Threshold		9	10	11	V
V_{ENA}	Enable Threshold, Rising		2.40	2.55	2.70	V
$V_{ENA(HYST)}$	Enable Threshold Hysteresis		0.20	0.25	0.30	V
I_{ENA}	Enable Input Current	ENA = 0 V	-5.0	-0.2	5.0	µA
$I_{V(RMS)}$	V_{RMS} Input Current	V_{RMS} = 5 V	-1.0	-0.01	1.0	µA
VOLTAGE AMPLIFIER						
$V_{OS(VA)}$	Voltage Amp Offset Voltage	VA_{OUT} = 0 V	-8		8	mV
$I_{B(VA)}$	V_{SENSE} Bias Current		-500	-25	500	nA
$A_{OL(VA)}$	Voltage Amp Gain		70	100		dB
$\Delta V_{OUT(VA)}$	Voltage Amp Output Swing			0.5 to 5.8		V
$I_{SC(VA)}$	Voltage Amp Short Circuit Current	VA_{OUT} = 0 V	-30	-12	-5	mA
I_{SS}	SS Current	SS = 2.5 V	-20	-14	-6	µA
CURRENT AMPLIFIER						
$V_{OS(CA)}$	Current Amp Offset Voltage		-4		4	mV
$I_{B(CA)}$	I_{SENSE} Bias Current		-500	-120	500	nA
$A_{OL(CA)}$	Current Amp Gain		80	110		dB
$\Delta V_{OUT(CA)}$	Current Amp Output Swing			0.5 to 16		V

Note 1: Power dissipation is 1 W when mounted as recommended. Derate at 8 mW/°C for operation above 25°C.
Note 2: Power dissipation is 750 mW when mounted as recommended. Derate at 3.3 mW/°C for operation above 25°C.
Gen. Note: All voltages with respect to GND (Pin 1).
Gen. Note: All currents are positive into the specified terminal.

TK83854 ELECTRICAL CHARACTERISTICS (CONT.)

Test conditions: V_{CC} = 18 V, R_{SET} = 15 k to GND, C_T = 1.5 nF, PKLMT = 1 V, ENA = 7.5 V, V_{RMS} = 1.5 V, IAC = 100 µA, VI_{SENSE} = 0 V, $V_{OUT(CA)}$ = 3.5 V, $V_{OUT(VA)}$ = 5 V, V_{SENSE} = 7.5 V, No load on SS, CA_{OUT}, VA_{OUT}, V_{ref}, GTDRV, T_A = Operating Temperature Range, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT AMPLIFIER						
$I_{SC(CA)}$	Current Amp Short Circuit Current	CA_{OUT} = 0 V	-30	-12	-5	mA
$V_{(ISENSE)}$	Input Range, I_{SENSE}, $MULT_{OUT}$		-0.3 to 2.5			V
GBW	Current Amp Gain-BW Product	T_A = 25 ° C (Note 3)	400	800		kHz
REFERENCE						
V_{ref}	Reference Voltage	I_{ref} = 0 mA, T_A = 25 ° C	7.4	7.5	7.6	V
		I_{ref} = 0 mA, Over Temp.	7.35	7.50	7.65	V
$\Delta V_{ref(LOAD)}$	V_{ref} Load Regulation	-10 mA < I_{ref} < 0 mA	-15	5	15	mV
$\Delta V_{ref(LINE)}$	V_{ref} Line Regulation	15 V < V_{CC} < 35 V	-10	2	10	mV
$I_{ref(SC)}$	V_{ref} Short Circuit Current	V_{ref} = 0 V	-50	-28	-12	mA
PEAK LIMIT						
$V_{OS(PL)}$	PKLMT Offset Voltage		-10		10	mV
$I_{B(PL)}$	PKLMT Input Current	PKLMT = -0.1 V	-200	-100		µA
$t_{D(PL)}$	PKLMT to GTDRV Prop. Delay	PKLMT falling from 50 mV to -50 mV		175		ns
GATE DRIVER						
$V_{G(MAX)}$	Maximum GTDRV Output Voltage	18 V < V_{CC} < 35 V, No Load	13.0	14.5	18.0	V
V_{GH}	GTDRV Output Voltage HIGH	200 mA Source, V_{CC} = 15 V	12.0	12.8		V
$V_{GL(OFF)}$	GTDRV Output Voltage LOW, OFF	50 mA Sink, V_{CC} = 0 V		0.9	1.5	V
V_{GL}	GTDRV Output Voltage LOW,	200 mA Sink		1.0	2.2	V
		10 mA Sink		0.1	0.4	V
$I_{G(PK)}$	Peak GTDRV Current	10 nF Load		1.0		A
$t_{R(G)}$ / $t_{F(G)}$	GTDRV Rise/Fall Time	1 nF Load		35		ns
D_{MAX}	GTDRV Maximum Duty Cycle	CA_{OUT} = 7 V		95		%

Note 3: Guaranteed by design; not 100% tested.
Gen Note: ENA input is internally clamped to approximately 14 V.

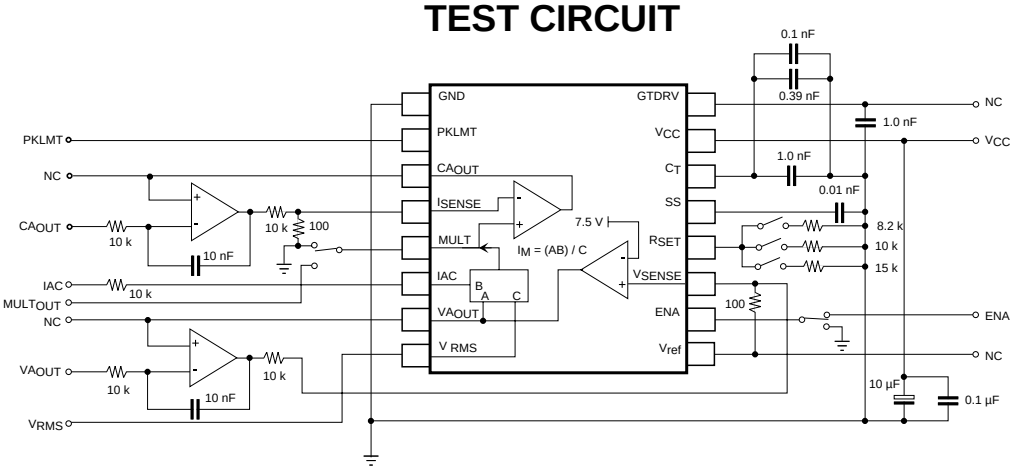
TK83854 ELECTRICAL CHARACTERISTICS (CONT.)

Test conditions: V_{CC} = 18 V, R_{SET} = 15 k to GND, C_T = 1.5 nF, PKLMT = 1 V, ENA = 7.5 V, V_{RMS} = 1.5 V, IAC = 100 µA, VI_{SENSE} = 0 V, $V_{OUT(CA)}$ = 3.5 V, $V_{OUT(VA)}$ = 5 V, V_{SENSE} = 7.5 V, No load on SS, CA_{OUT}, VA_{OUT}, V_{ref}, GTDRV, T_A = Operating Temperature Range, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MULTIPLIER						
$I_{OM(IAC)}$	Multiplier Output Current (IAC LIMITED)	IAC = 100 µA, R_{SET} = 10 k	-220	-200	-180	µA
$I_{OM(ZC)}$	Multiplier Output Current Zero	IAC = 0 µA, R_{SET} = 15 k	-2.0	-0.2	2.0	µA
$I_{OM(SET)}$	Multiplier Output Current (R_{SET} LIMITED)	IAC = 450 µA, R_{SET} = 15 k, V_{RMS} = 1 V, VA = 6 V	-280	-255	-220	µA
I_{OM}	Multiplier Output Current	IAC = 50 µA, V_{RMS} = 2 V, VA = 4 V	-50	-42	-33	µA
		IAC = 100 µA, V_{RMS} = 2 V, VA = 2 V	-38	-27	-12	µA
		IAC = 200 µA, V_{RMS} = 2 V, VA = 4 V	-165	-150	-105	µA
		IAC = 300 µA, V_{RMS} = 1 V, VA = 2 V	-250	-225	-150	µA
		IAC = 100 µA, V_{RMS} = 1 V, VA = 2 V	-95	-80	-60	µA
K	Multiplier Gain Current	(Note 4)		-1.0		V
OSCILLATOR						
f_{OSC}	Oscillator Frequency	R_{SET} = 15 k	46	55	62	kHz
		R_{SET} = 8.2 k	86	102	118	kHz
V_{RP}	C_T Ramp Peak-to-Peak Amplitude		4.9	5.4	5.9	V
V_{RV}	C_T Ramp Valley Voltage		0.8	1.1	1.3	V

Note 4: Multiplier gain constant (K) is defined by $IOM = [K \times I_{IAC} \times (V_{OUT(VA)} - 1)] / V_{RMS}^2$.

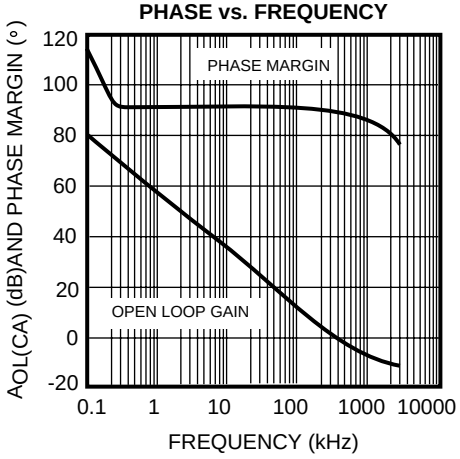
TEST CIRCUIT



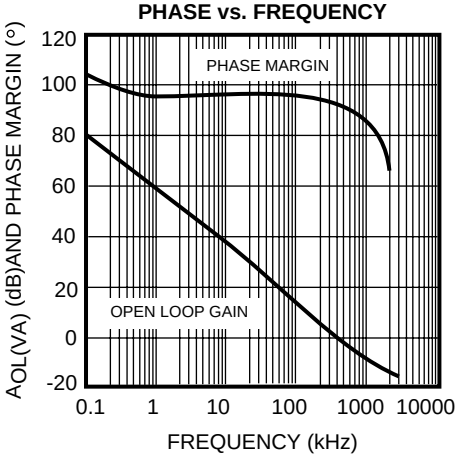
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = T_J = 25\ °C$

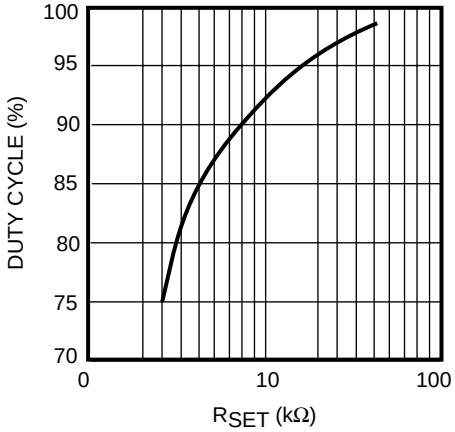
CURRENT AMPLIFIER GAIN AND PHASE vs. FREQUENCY



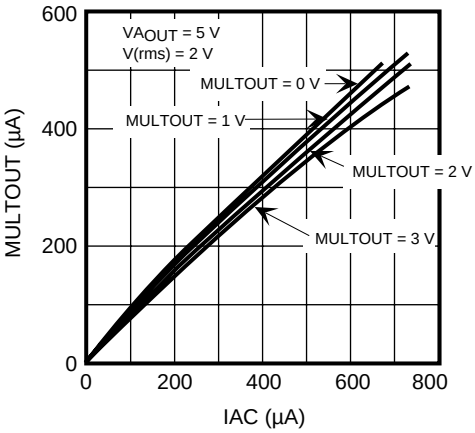
VOLTAGE AMPLIFIER GAIN AND PHASE vs. FREQUENCY



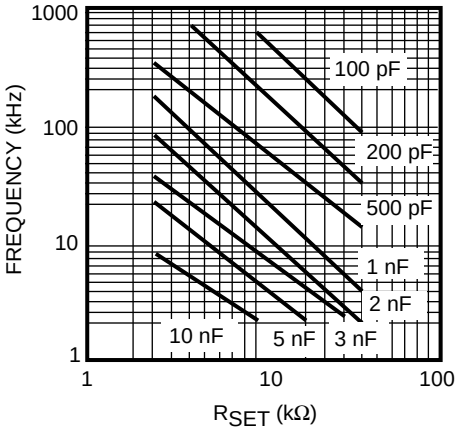
GATE DRIVE MAXIMUM DUTY CYCLE vs. R_{SET}



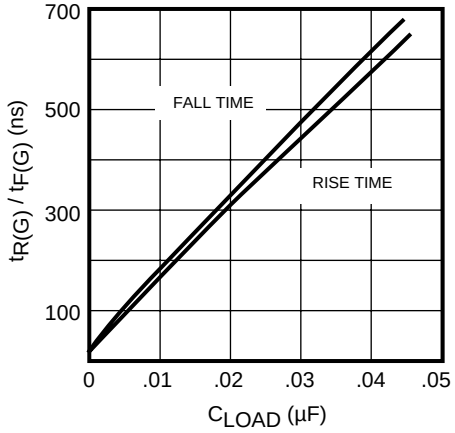
MULTIPLIER OUTPUT vs. VOLTAGE ON MULTIPLIER



OSCILLATOR FREQUENCY vs. R_{SET} AND C_T



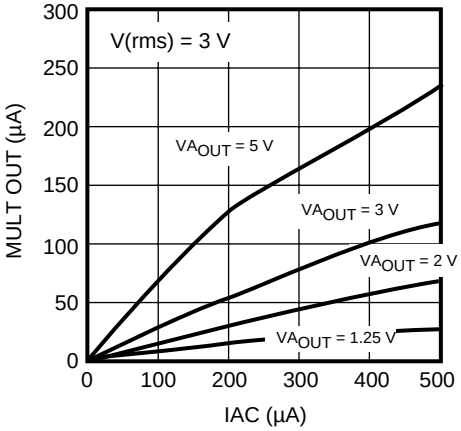
GATE DRIVE RISE AND FALL TIMES vs. LOAD CAPACITANCE



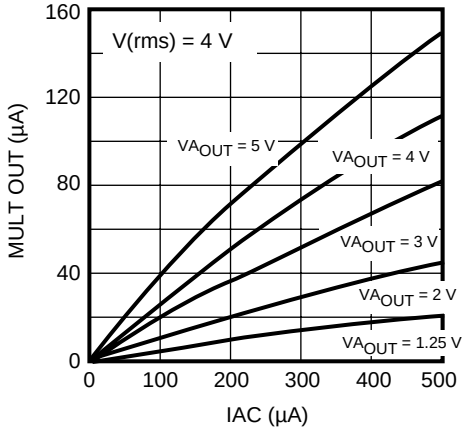
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

$T_A = T_J = 25\ °C$

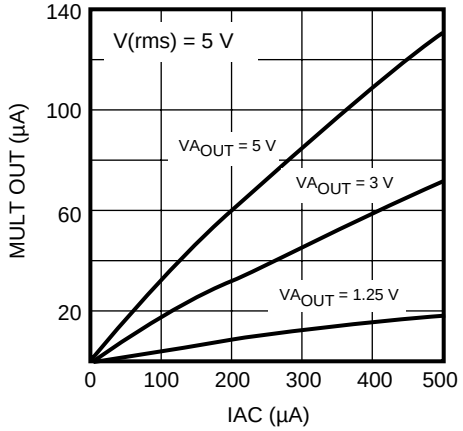
MULTIPLIER OUTPUT vs. MULTIPLIER INPUT (MULTOUT = 0 V)



MULTIPLIER OUTPUT vs. MULTIPLIER INPUT (MULTOUT = 0 V)



MULTIPLIER OUTPUT vs. MULTIPLIER INPUT (MULTOUT = 0 V)



PIN DESCRIPTION

GROUND PIN (GND)

All voltages are measured with respect to GND. V_{CC} and V_{ref} should be bypassed directly to GND with a 0.1 µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing capacitor to GND should also be as short and as direct as possible.

PEAK LIMIT (PKLMT)

The threshold for PKLMT is GND. Connect this input to the negative voltage on the current sense resistor as shown in Figure 1. Use a resistor to V_{ref} to offset the negative current sense signal up to GND.

CURRENT AMPLIFIER OUTPUT (CA_{OUT})

This is the output of a wide-bandwidth op-amp that senses line current and commands the Pulse Width Modulator (PWM) to force the correct current. This output can swing close to GND, allowing the PWM to force zero duty cycle when necessary. The current amplifier will remain active even if the IC is disabled.

CURRENT SENSE MINUS (I_{SENSE})

This is the inverting input to the current amplifier. This input and the non-inverting input $MULT_{OUT}$ remain functional down to and below GND. Care should be taken to avoid taking these inputs below –0.5 V, because they are protected with diodes to GND.

MULTIPLIER OUTPUT AND CURRENT SENSE PLUS ($MULT_{OUT}$)

The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at $MULT_{OUT}$. The cautions about taking I_{SENSE} below –0.5 V also apply to $MULT_{OUT}$. As the multiplier output is a current, this is a high impedance input similar to I_{SENSE}, so the current amplifier can be configured as a differential amplifier to reject GND noise. Figure 1 shows an example of using the current amplifier differentially.

INPUT AC CURRENT (IAC)

This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (IAC to $MULT_{OUT}$), so this is the only multiplier input that should be used for sensing instantaneous line voltage. The nominal voltage on IAC is 6 V, so in addition to a resistor from IAC to rectified line, connect a resistor from IAC to V_{ref}. If the resistor to V_{ref} is one-fourth of the value of the resistor to the rectifier, then the 6 V offset will be cancelled, and the line current will have minimal crossover distortion.

VOLTAGE AMPLIFIER OUTPUT (VA_{OUT})

This is the output of the op-amp that regulates output voltage. Like the current amplifier, the voltage amplifier will also stay active even if the IC is disabled with either ENA or V_{CC}. This means that large feedback capacitors across the amplifier will stay charged through momentary disable cycles. Voltage amplifier output levels below ~1 V will inhibit multiplier output.

RMS LINE VOLTAGE (V(rms))

The output of a boost PWM is proportional to the input voltage, so when the line voltage into a low-bandwidth boost PWM voltage regulator changes, the output will change immediately and slowly recover to the regulated level. For these devices, the V(rms) input compensates for line voltage changes if it is connected to a voltage proportional to the RMS input line voltage. For best control, the V_{RMS} voltage should stay between 1.5 V and 3.5 V.

VOLTAGE REFERENCE OUTPUT (V_{ref})

V_{ref} is the output of an accurate 7.5 V voltage reference. This output is capable of delivering 10 mA to peripheral circuitry and is internally short circuit current limited. V_{ref} is disabled and will remain at 0 V when V_{CC} is low or when ENA is low. Bypass V_{ref} to GND with a 0.1 µF or larger ceramic capacitor for best stability.

ENABLE (ENA)

ENA is a logic input that will enable the PWM output, voltage reference, and oscillator. ENA also will release the soft start clamp, allowing SS to rise. When unused, connect ENA to a +5 V supply or pull ENA high with a 22 k resistor. The ENA pin is not intended to be used as a high-speed shutdown to the GTDRV output.

PIN DESCRIPTION (CONT.)

VOLTAGE AMPLIFIER INVERTING OUTPUT (V_{SENSE})

This is normally connected to a feedback network and to the boost converter output through a divider network.

OSCILLATOR CHARGING CURRENT AND MULTIPLIER LIMIT SET (R_{SET})

A resistor from R_{SET} to ground will program oscillator charging current and maximum multiplier output. Multiplier output current will not exceed 3.75 V divided by the resistor from R_{SET} to ground.

SOFT-START (SS)

SS will remain at GND as long as the IC is disabled or V_{CC} is too low. SS will pull up to over 8 V by an internal 14 µA current source when both V_{CC} becomes valid and the IC is enabled. SS will act as the reference input to the voltage amplifier if SS is below V_{ref}. With a large capacitor from SS to GND, the reference to the voltage regulating amplifier will rise slowly, and increase the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS will quickly discharge to ground and disable the PWM.

OSCILLATOR TIMING CAPACITOR (C_T)

A capacitor from C_T to GND will set the PWM oscillator frequency according to this relationship:

$$f_{OSC} = 1.25 / (R_{SET} \times C_T)$$

POSITIVE SUPPLY VOLTAGE (V_{CC})

Connect V_{CC} to a stable source of at least 20 mA above 17 V for normal operation. Also bypass V_{CC} directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate GTDRV signals, these devices will be inhibited unless V_{CC} exceeds the upper undervoltage lockout threshold and remains above the lower threshold.

GATE DRIVER (GTDRV)

The output of the PWM is a totem pole MOSFET gate driver on GTDRV. This output is internally clamped to 15 V so the IC can be operated with V_{CC} as high as 35 V. Use a series gate resistor of at least 5 ohms to prevent interaction between the gate impedance and the GTDRV output driver that might cause the GTDRV output to overshoot excessively. Some overshoot of the GTDRV output is always expected when driving a capacitive load.

APPLICATION INFORMATION

A 250 W PREREGULATOR

Figure 1 shows a typical application of the TK83854 as a preregulator with high power factor and efficiency. The assembly consists of two distinct parts, the control circuit centering on the TK83854 and the power section.

The power section is a "boost" converter, with the inductor operating in the continuous mode. In this mode, the duty cycle is dependent on the ratio between input and output voltages. Also, the input current has low switching frequency ripple, which means that the line noise is low. Furthermore, the output voltage must be higher than the peak value of the highest expected AC line voltage, and all components must be rated accordingly.

In the control section, the TK83854 provides PWM pulses to the power MOSFET gate (GTDRV, Pin 16). The duty cycle of this output is simultaneously controlled by four separate inputs to the chip:

INPUT	PIN #	FUNCTION
V_{SENSE}	11	Output DC Voltage
IAC	6	Line Voltage Waveform
I_{SENSE} /$MULT_{OUT}$	4/5	Line Current
V_{RMS}	8	RMS Line Voltage

Additional controls of an auxiliary nature are provided. They are intended to protect the switching power MOSFET from certain transient conditions, as follows:

INPUT	PIN #	FUNCTION
ENA	10	Start-up Delay
SS	13	Soft Start
PKLMT	2	Maximum Current Limit

PROTECTION INPUTS

Enable (ENA)

The ENA input must reach 2.5 V before the V_{ref} and GTDRV outputs are enabled. This provides a means to shut down the gate in case of trouble, or to add a time delay at power up. A hysteresis gap of 200 mV is provided at this terminal to prevent erratic operation. Undervoltage protection is provided directly at Pin 15, where the on/off thresholds are 16 V and 10 V, respectively.

Soft-Start (SS)

The voltage at Pin 13 (SS) can reduce the reference voltage used by the error amplifier to regulate the output DC voltage. With Pin 13 open, the reference voltage is typically 7.5 V. An internal current source delivers approximately 14 µA from Pin 13. Thus, a capacitor connected between that pin and GND will charge linearly from zero to 7.5 V in 0.54 x C seconds, with C expressed in microfarads.

Peak Current Limit (PKLMT)

Use Pin 2 to establish the highest value of current to be controlled by the power MOSFET. With the resistor divider values shown in Figure 1, the 0.0 V threshold at Pin 2 is reached when the voltage drop across the 0.25 Ω current sense resistor is 7.5 V x 1.6 k / 10 k = 1.2 V, corresponding to 4.8 A. A bypass capacitor from Pin 2 to ground is recommended to filter out very high frequency noise.

CONTROL INPUTS

Output DC Voltage Sense (V_{SENSE})

The threshold voltage for the V_{SENSE} input is 7.5 V and the input bias current is typically -10 nA. The values shown in Figure 1 are for an output voltage of 400 VDC. In this circuit, the voltage amplifier operates with a constant low frequency gain for minimum output excursions. The 0.047 µF feedback capacitor places a 15 Hz pole in the voltage loop that prevents 120 Hz ripple from propagating to the output current.

Line Waveform (IAC)

In order to force the line current waveshape to follow the line voltage, a sample of the power line voltage waveform is introduced at Pin 6. This signal is multiplied by the output of the voltage amplifier in the internal multiplier to generate a reference signal for the current control loop.

This input is not a voltage, but a current (hence IAC). It is set up by the 220 k and 910 k resistive divider (see Figure 1). The voltage at pin 6 is internally held at 6 V, and the two resistors are chosen so that the current flowing into pin 6 varies from zero (at each zero crossing) to about 400 µA at the peak of the waveshape. The following formulas were

APPLICATION INFORMATION (CONT.)

used to calculate these resistors:

$$R_{IAC} = V_{PK(MAX)} / 400 \text{ E - } 6$$
$$= (260 \text{ VAC} \times \sqrt{2}) / 400 \text{ µA}$$
$$= 910 \text{ k}$$
$$R_{REF} = R_{IAC} / 4 = 220 \text{ k}$$

where V_{PK} is the peak line voltage.

Line Current (I_{SENSE}/MULTOUT)

The voltage drop across the 0.25 Ω current-sense resistor is applied to Pins 4 and 5 as shown. The current-sense amplifier also operates with high low-frequency gain, but unlike the voltage amplifier, it is set up to give the current-control loop a very wide bandwidth. This enables the line current to follow the line voltage as closely as possible. In the present example, this amplifier has a zero at about 500 Hz, and a gain of about 18 dB thereafter.

RMS Line Voltage (V_{RMS})

An important feature of the TK83854 preregulator is that it can operate with a three-to-one range of input line voltages, covering everything from low line in Japan (85 VAC) to high line in Europe (255 VAC). This is done using line feed-forward, which keeps the input power constant with varying input voltage (assuming constant load power). To do this, the multiplier divides the line current by the square of the rms value of the line voltage. The voltage applied to Pin 8, proportional to the average of the rectified line voltage (and proportional to the RMS value), is squared in the TK83854, and then used as a divisor by the multiplier block. The multiplier output, at Pin 5, is a current that increases with the current at Pin 6 and the voltage at Pin 7, and decreases with the square of the voltage at pin 8.

PWM Frequency

The PWM oscillator frequency in Figure 1 is 100 kHz. This value is determined by C_T at Pin 14 and R_{SET} at Pin 12. R_{SET} should be chosen first because it affects the maximum value of I_{OM} according to the equation:

$$I_{OM(MAX)} = -3.75 \text{ V} / R_{SET}$$

This effectively sets a maximum PWM-controlled current.

With R_{SET} = 15 k:

$$I_{OM(MAX)} = -3.75 \text{ V} / 15 \text{ k} = -250 \text{ µA}$$

It is also important to note that the multiplier output current will never exceed twice IAC.

With the 3.9 k resistor from $MULT_{OUT}$ to the 0.25 Ω current sense resistor, the maximum current in the current sense resistor will be:

$$I_{RCS(MAX)} = (-I_{OM(MAX)} \times 3.9 \text{ k}) / 0.25 \text{ Ω} = -3.9 \text{ A}$$

Having selected R_{SET}, the current sense resistor, and the resistor from $MULT_{OUT}$ to the current sense resistor, calculate C_T for the desired PWM oscillator frequency from the equation:

$$C_T = 1.25 / (f_{OSC} \times R_{SET})$$

APPLICATION INFORMATION (CONT.)

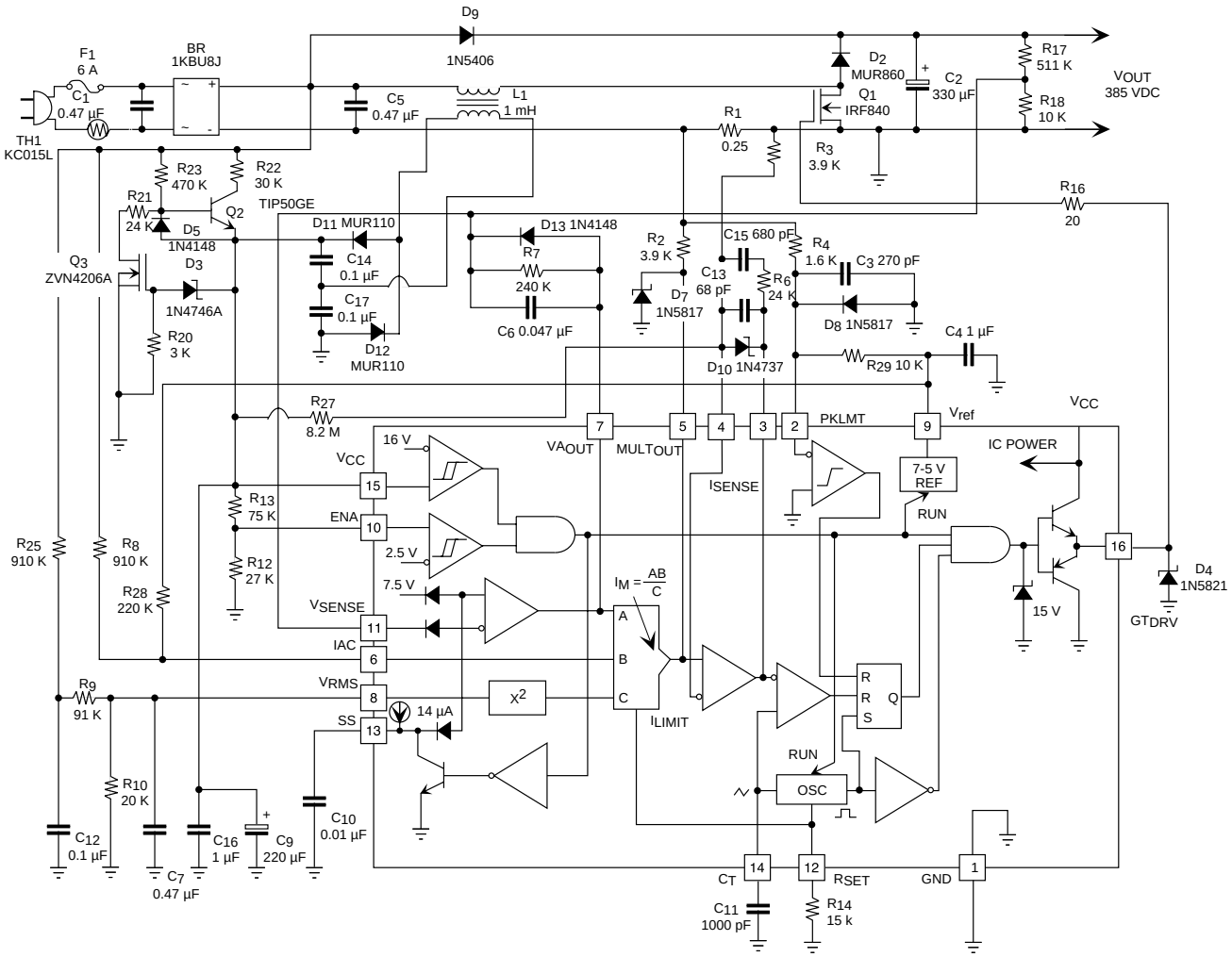
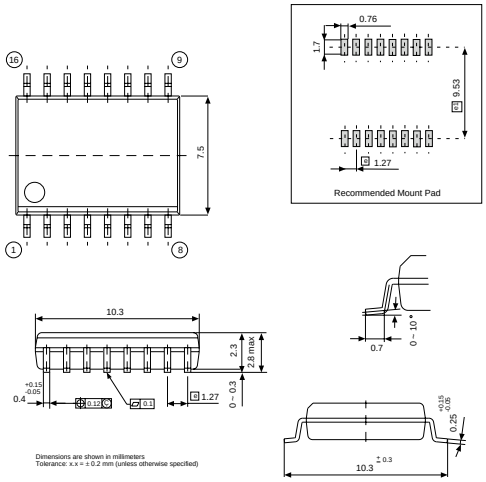


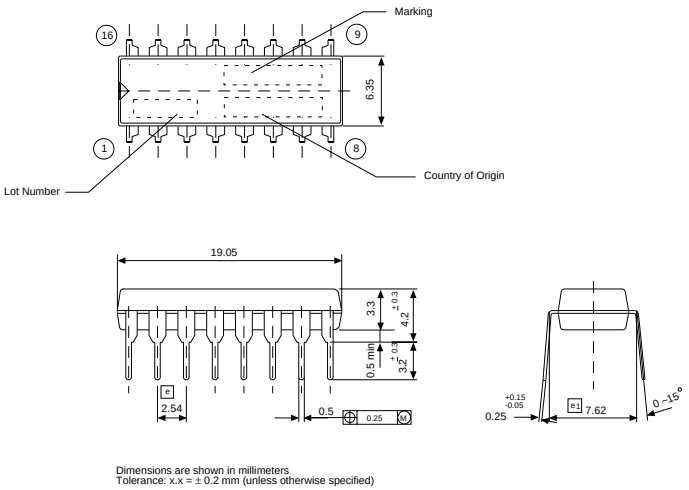
FIGURE 1: 250 W PREREGULATOR

PACKAGE OUTLINE

SOP-16



DIP-16



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