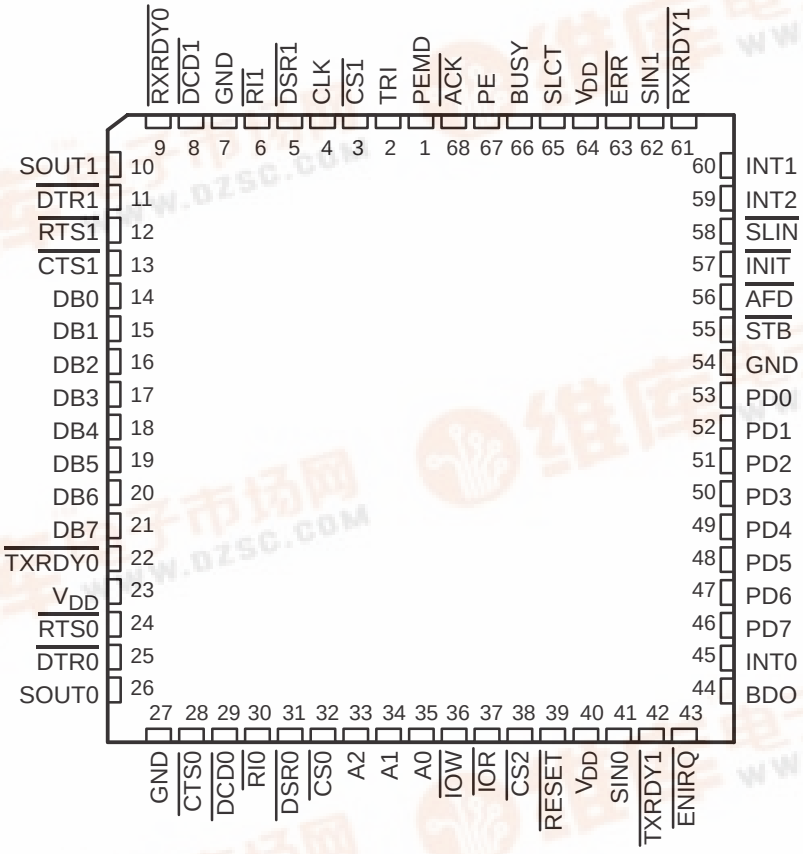
TL16C552
DUAL ASYCHRONOUS COMMUNICATIONS ELEMENT WITH FIFO

SLLS102B – DECEMBER 1990 – REVISED MARCH 1996

- IBM PC/AT™ Compatible
- Two TL16C550 ACEs
- Enhanced Bidirectional Printer Port
- 16-Byte FIFOs Reduce CPU Interrupts
- Independent Control of Transmit, Receive, Line Status, and Data Set Interrupts on Each Channel
- Individual Modem Control Signals for Each Channel
- Programmable Serial Interface Characteristics for Each Channel:
  - 5-, 6-, 7-, or 8-bit Characters
  - Even-, Odd-, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
- 3-State TTL Drive for the Data and Control Bus on Each Channel
- Hardware and Software Compatible With TL16C452

description

FN PACKAGE
(TOP VIEW)



description

The TL16C552 is an enhanced dual channel version of the popular TL16C550 asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters

description (continued)

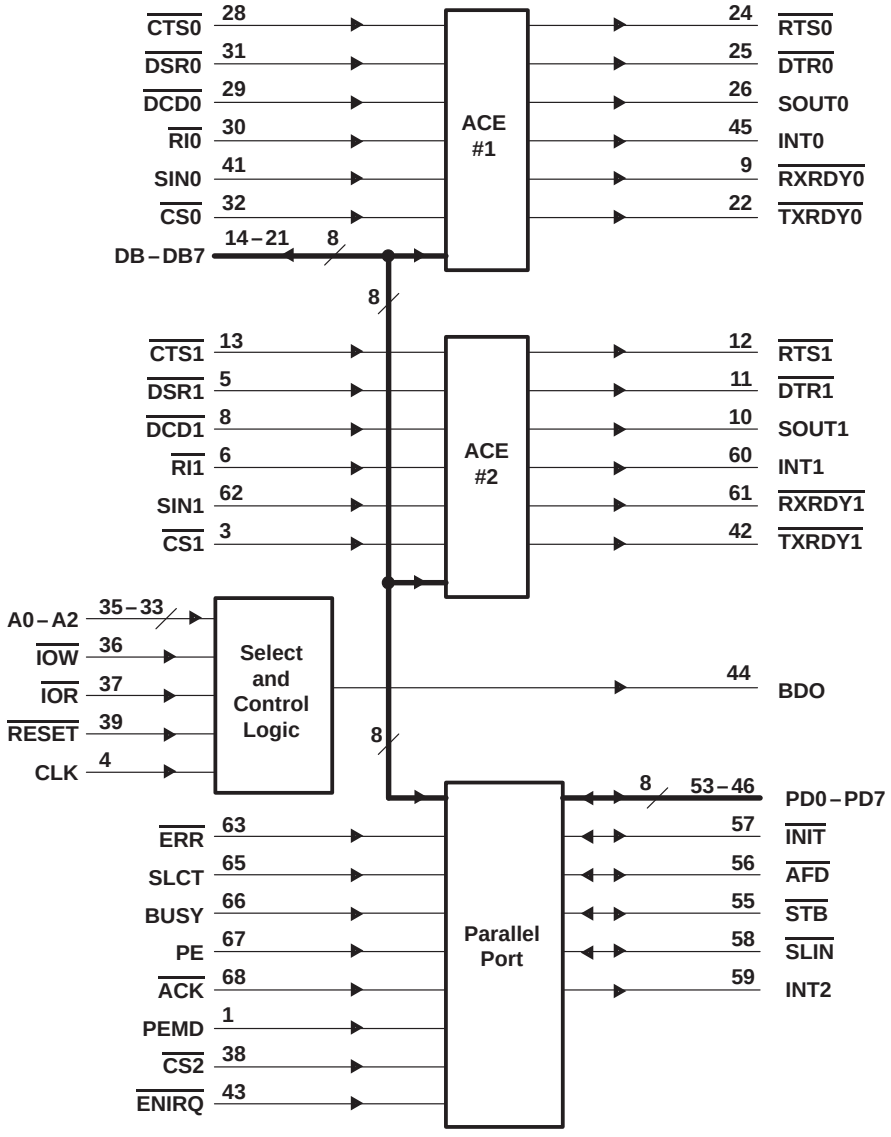
received from peripheral devices or modems and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed and the error conditions.

In addition to its dual communications interface capabilities, the TL16C552 provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics-type printer. The parallel port and the two serial ports provide IBM PC/AT-compatible computers with a single device to serve the three system ports.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and (2^{16} – 1).

The TL16C552 is housed in a 68-pin plastic leaded chip carrier.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{ACK}$	68	I	Line printer acknowledge. $\overline{ACK}$ goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.
$\overline{AFD}$	56	I/O	Line printer autofeed. $\overline{AFD}$ is an open-drain line that provides the printer with an active-low signal when continuous form paper is to be autofed to the printer. This terminal has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
A0, A1, A2	35, 34, 33	I	Address lines A0 – A2. A0, A1, and A2 select the internal registers during CPU bus operations. See Table 2 for the decode of the serial channels and Table 13 for the decode of the parallel printer port.
BDO	44	O	Bus buffer output. BDO is an active-high output that is asserted when either serial channel or the parallel port is read. This output can control the system bus driver (74LS245).
BUSY	66	I	Line printer busy. BUSY is an input line from the printer that goes high when the printer is not ready to accept data.
CLK	4	I	Clock input. CLK is an external clock input to the baud rate divisor of each ACE.
$\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$	32, 3, 38	I	Chip selects. $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ act as an enable for the write and read signals for the serial channels 1 ($\overline{CS0}$) and 2 ($\overline{CS1}$). $\overline{CS2}$ enables the signals to the printer port.
$\overline{CTS0}$, $\overline{CTS1}$	28, 13	I	Clear to send inputs. The logical state of $\overline{CTS0}$ or $\overline{CTS1}$ is reflected in the CTS bit of the modem status register ($\overline{CTS}$ is bit 4 of the modem status register, written MSR4) of each ACE. A change of state in either $\overline{CTS}$ terminal, since the previous reading of the associated modem status register, causes the setting of delta clear to send (ΔCTS) bit (MSR0) of each modem status register.
DB0 – DB7	14 – 21	I/O	Data bits DB0 – DB7. The data bus provides eight 3-state I/O lines for the transfer of data, control, and status information between the TL16C552 and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
$\overline{DCD0}$, $\overline{DCD1}$	29, 8	I	Data carrier detect. $\overline{DCD}$ is a modem input. Its condition can be tested by the CPU by reading the MSR7 (DCD) bit of the modem status registers. The MSR3 (delta data carrier detect or ΔDCD) bit of the modem status register indicates whether the $\overline{DCD}$ input has changed states since the previous reading of the modem status register. $\overline{DCD}$ has no affect on the receiver.
$\overline{DSR0}$, $\overline{DSR1}$	31, 5	I	Data set ready inputs. The logical state of $\overline{DSR0}$ and $\overline{DSR1}$ is reflected in MSR5 of its associated modem status register. The MSR1 (delta data set ready or ΔDSR) bit indicates whether the associated DSR terminal has changed states since the previous reading of the modem status register.
$\overline{DTR0}$, $\overline{DTR1}$	25, 11	O	Data terminal ready lines. $\overline{DTR0}$ and $\overline{DTR1}$ can be asserted low by setting modem control register bit 0 (MCR0) of its associated ACE. This signal is asserted high by clearing the DTR bit (MCR0) or whenever a reset occurs. When active (low), the DTR terminal indicates that its ACE is ready to receive data.
$\overline{ENIRQ}$	43	I	Parallel port interrupt source mode selection. When $\overline{ENIRQ}$ is low, the PC/AT mode of interrupts is enabled. In this mode, the INT2 output is internally connected to the $\overline{ACK}$ input. When the $\overline{ENIRQ}$ input is tied high, the INT2 output is internally tied to the $\overline{PRINT}$ signal in the line printer status register. INT2 is latched high on rising edge of $\overline{ACK}$.
$\overline{ERR}$	63	I	Line printer error. $\overline{ERR}$ is an input line from the printer. The printer reports an error by holding this line low during the error condition.
GND	7, 27, 54		Ground (0 V). All terminals must be tied to ground for proper operation.
$\overline{INIT}$	57	I/O	Line printer initialize. $\overline{INIT}$ is an open-drain line that provides the printer with an active-low signal, which allows the printer initialization routine to be started. This terminal has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
$\overline{IOR}$	37	I	Input/output read strobe. $\overline{IOR}$ is an active-low input that enables the selected channel to output data to the data bus (DB0 – DB7). The data output depends upon the register selected by the address inputs A0, A1, A2, and chip select. Chip select 0 ($\overline{CS0}$) selects ACE #1, chip select 1 ($\overline{CS1}$) selects ACE #2, and chip select 2 ($\overline{CS2}$) selects the printer port.
$\overline{IOW}$	36	I	Input/output write strobe. $\overline{IOW}$ is an active-low input causing data from the data bus to be input to either ACE or to the parallel port. The destination depends upon the register selected by the address inputs A0, A1, A2, and chip selects $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
INT0, INT1	45, 60	O	Serial channel interrupts. INT0 and INT1 are 3-state serial channel interrupt outputs (enabled by bit 3 of the MCR) that go active (high) when one of the following interrupts has an active (high) condition and is enabled by the interrupt enable register of its associated channel: receiver error flag, received data available, transmitter holding register empty, and modem status. The interrupt is cleared upon appropriate service. When reset, the interrupt output is in the high-impedance state.
INT2	59	O	Printer port interrupt. INT2 is an active-high, 3-state output generated by the positive transition of $\overline{ACK}$. It is enabled by bit 4 of the write control register. Upon a reset, the interrupt output is in the high-impedance state. Its mode is also controlled by $\overline{ENIRQ}$.
PD0–PD7	53–46	I/O	Parallel data bits (0–7). These eight lines (PD0–PD7) provide a byte wide input or output port to the system.
PE	67	I	Printer paper empty. PE is an input line from the printer that goes high when the printer runs out of paper.
PEMD	1	I	Printer enhancement mode. When low, PEMD enables the write data register to the PD0–PD7 lines. A high on this signal allows direction control of the PD0–PD7 port by the DIR bit in the control register. PEMD is usually tied low for the printer operation.
$\overline{RESET}$	39	I	Reset. When low, $\overline{RESET}$ forces the TL16C552 into an idle mode in which all serial data activities are suspended. The modem control register along with its associated outputs are cleared. The line status register is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities. This input has a hysteresis level of typically 400 mV.
$\overline{RTS0}$, $\overline{RTS1}$	24, 12	O	Request to send outputs. $\overline{RTSx}$ is asserted low by setting MCR1, bit 1 of its UARTs modem control register. Both $\overline{RTSx}$ terminals are set by $\overline{RESET}$. A low on the $\overline{RTSx}$ terminal indicates that its ACE has data ready to transmit. In half-duplex operations, $\overline{RTSx}$ controls the direction of the line.
$\overline{RXRDY0}$, $\overline{RXRDY1}$	9, 61	O	Receiver ready. $\overline{RXRDY0}$ and $\overline{RXRDY1}$ are receiver direct memory access (DMA) signaling terminals. One of two types of DMA signaling can be selected using FIFO control register bit 3 (FCR3) when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. For signal transfer DMA (a transfer is made between CPU bus cycles), mode 0 is used. Multiple transfers that are made continuously until the receiver FIFO has been emptied are supported by mode 1. Mode 0. $\overline{RXRDYx}$ is active (low) when in the FIFO mode (FCR0=1, FCR3=0) or when in the TL16C450 mode (FCR0=0) and the receiver FIFO or receiver holding register contain at least one character. When there are no more characters in the receiver FIFO or receiver holding register, the $\overline{RXRDYx}$ terminal goes inactive (high). Mode 1. $\overline{RXRDYx}$ goes active (low) in the FIFO mode (FCR0=1) when FCR3=1 and the time-out or trigger levels have been reached. It goes inactive (high) when the FIFO or receiver holding register is empty.
$\overline{RI0}$, $\overline{RI1}$	30, 6	I	Ring indicator inputs. $\overline{RI0}$ and $\overline{RI1}$ are modem control inputs. Their condition is tested by reading MSR6 (RI) of each ACE. The modem status register outputs trailing edge of ring indicator (TERI or MSR2) that indicates whether either input has changed states from high to low since the previous reading of the modem status register.
SIN0, SIN1	41, 62	I	Serial data inputs. SIN0 and SIN1 are serial data inputs that move information from the communication line or modem to the TL16C552 receiver circuits. Mark (set) is a high state and a space (cleared) is low state. Data on the serial data inputs is disabled when operating in the loop mode.
SLCT	65	I	Printer selected. SLCT is an input line from the printer that goes high when the printer has been selected.
$\overline{SLIN}$	58	I/O	Line printer select. $\overline{SLIN}$ is an open-drain input that selects the printer when it is active (low). This terminal has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
SOUT0, SOUT1	26, 10	O	Serial data outputs. SOUT0 and SOUT1 are the serial data outputs from the ACE transmitter circuitry. A mark is a high state and a space is a low state. Each SOUT is held in the mark condition when the transmitter is disabled, when $\overline{RESET}$ is true (low), when the transmitter register is empty, or when in the loop mode.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{STB}$	55	I/O	Printer strobe. $\overline{STB}$ is an open-drain line that provides communication between the TL16C552 and the printer. When it is active (low), it provides the printer with a signal to latch the data currently on the parallel port. This terminal has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
TRI	2	I	3-state control. TRI controls the 3-state control of all I/O and output terminals. When TRI is asserted, all I/O and outputs become high impedance, allowing board level testers to drive the outputs without overdriving the internal buffers. This terminal is level sensitive, is a CMOS input, and is pulled down with an internal resistor that is approximately 5 kΩ.
$\overline{TXRDY0}$, $\overline{TXRDY1}$	22, 42	O	Transmitter ready. $\overline{TXRDY0}$ and $\overline{TXRDY1}$ are transmitter ready signals. Two types of DMA signaling are available. Either can be selected using FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. Single-transfer DMA (a transfer is made between CPU bus cycles) is supported by mode 0. Multiple transfers that are made continuously until the transmitter FIFO has been filled are supported by mode 1. Mode 0. When in the FIFO mode (FCR0=1, FCR3=0) or in the TL16C450 mode (FCR0=0) and there are no characters in the transmitter holding register or transmitter FIFO, $\overline{TXRDY}$ are active (low). Once $\overline{TXRDY}$ is activated (low), it goes inactive after the first character is loaded into the holding register of transmitter FIFO. Mode 1. $\overline{TXRDYx}$ goes active (low) if in the FIFO mode (FCR0=1) when FCR3=1 and there are no characters in the transmitter FIFO. When the transmitter FIFO is completely full, $\overline{TXRDYx}$ goes inactive (high).
V_{DD}	23, 40, 64		Power supply. V_{DD} is the power supply requirement is 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.5 V to V_{DD} + 0.3 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Output voltage range, V_O . . . . . –0.5 V to V_{DD} + 0.3 V
Continuous total power dissipation . . . . . 500 mW
Operating free-air temperature range, T_A . . . . . –10°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to ground (V_{SS}).

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75	5	5.25	V
Clock high-level input voltage, $V_{IH(CLK)}$	2		V_{DD}	V
Clock low-level input voltage, $V_{IL(CLK)}$	–0.5		0.8	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	–0.5		0.8	V
Clock frequency, f_{clock}			8	MHz
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –0.4 mA for DB0–DB7, I_{OH} = –2 mA for PD0–PD7, I_{OH} = –0.4 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OH} = –0.4 mA for all other outputs	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA for DB0–DB7, I_{OL} = 12 mA for PD0–PD7, I_{OL} = 10 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OL} = 2 mA for all other outputs		0.4	V
I_I	Input current	V_{DD} = 5.25 V, All other terminals are floating		±10	µA
$I_{I(CLK)}$	Clock input current	V_I = 0 to 5.25 V		±10	µA
I_{OZ}	High-impedance output current	V_{DD} = 5.25 V, V_O = 0 with chip deselected, or V_O = 5.25 V with chip and write mode selected		±20	µA
I_{DD}	Supply current	V_{DD} = 5.25 V, No loads on outputs, $\overline{SIN0}$, $\overline{SIN1}$, $\overline{DSR0}$, $\overline{DSR1}$, $\overline{DCD0}$, $\overline{DCD1}$, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{RI0}$ and $\overline{RI1}$ at 2 V, Other inputs at 0.8 V, Baud rate generator f_{clock} = 8 MHz, Baud rate = 56 kbit/s		50	mA

NOTE 2: These four terminals contain an internal pullup resistor to V_{DD} of approximately 10 kΩ.

clock timing requirements over recommended ranges of operating free-air temperature and supply voltage

		MIN	MAX	UNIT
t_{w1}	Pulse duration, CLK high (external clock, 8 MHz max) (see Figure 1)	55		ns
t_{w2}	Pulse duration, CLK low (external clock, 8 MHz max) (see Figure 1)	55		ns
t_{w3}	Pulse duration, master ($\overline{RESET}$) low (see Figure 16)	1000		ns

read cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

		MIN	MAX	UNIT
t_{w4}	Pulse duration, $\overline{IOR}$ low	80		ns
t_{su1}	Setup time, chip select valid before $\overline{IOR}$ low (see Note 3)	15		ns
t_{su2}	Setup time, A2–A0 valid before $\overline{IOR}$ low (see Note 3)	15		ns
t_{h1}	Hold time, A2–A0 valid after $\overline{IOR}$ high (see Note 3)	20		ns
t_{h2}	Hold time, chip select valid after $\overline{IOR}$ high (see Note 3)	20		ns
t_{d1}	Delay time, $t_{su2} + t_{w4} + t_{d2}$ (see Note 4)	175		ns
t_{d2}	Delay time, $\overline{IOR}$ high to $\overline{IOR}$ or $\overline{IOW}$ low	80		ns

NOTES: 3. The internal address strobe is always active.
4. In the FIFO mode, t_{d1} = 425 ns (min) between reads of the receiver FIFO and the status registers (IIR and LSR).

write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

		MIN	MAX	UNIT
t_{w5}	Pulse duration, $\overline{IOW}$ low	80		ns
t_{su4}	Setup time, chip select valid before $\overline{IOW}$ low (see Note 3)	15		ns
t_{su5}	Setup time, A2–A0 valid before $\overline{IOW}$ low (see Note 3)	15		ns
t_{su6}	Setup time, D0–D7 valid before $\overline{IOW}$ high	15		ns
t_{h3}	Hold time, A2–A0 valid after $\overline{IOW}$ high (see Note 3)	20		ns
t_{h4}	Hold time, chip select valid after $\overline{IOW}$ high (see Note 3)	20		ns
t_{h5}	Hold time, D0–D7 valid after $\overline{IOW}$ high	15		ns
t_{d3}	Delay time, $t_{su5} + t_{w5} + t_{d4}$	175		ns
t_{d4}	Delay time, $\overline{IOW}$ high to $\overline{IOW}$ or $\overline{IOR}$ low	80		ns

NOTE 3: The internal address strobe is always active.

read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	Propagation delay time from $\overline{IOR}$ high to BDO high or from $\overline{IOR}$ low to BDO low	C_L = 100 pF, See Note 5		60	ns
t_{en}	Enable time from $\overline{IOR}$ low to D0–D7 valid	C_L = 100 pF, See Note 5		60	ns
t_{dis}	Disable time from $\overline{IOR}$ high to D0–D7 released	C_L = 100 pF, See Note 5	0	60	ns

NOTE 5: V_{OL} and V_{OH} (and the external loading) determine the charge and discharge time.

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 6, 7, and 8)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, interrupt THRE low to SOUT low at start		8	24	RCLK cycles
t_{d6}	Delay time, SOUT low at start to interrupt THRE high	See Note 6	8	8	RCLK cycles
t_{d7}	Delay time, $\overline{IOW}$ (WR THR) high to interrupt THRE high	See Note 6	16	32	RCLK cycles
t_{d8}	Delay time, SOUT low at start to $\overline{TXRDY}$ low	C_L = 100 pF		8	RCLK cycles
t_{pd2}	Propagation delay time from $\overline{IOW}$ (WR THR) low to interrupt THRE low	C_L = 100 pF		140	ns
t_{pd3}	Propagation delay time from $\overline{IOR}$ (RD IIR) high to interrupt THRE low	C_L = 100 pF		140	ns
t_{pd4}	Propagation delay time from $\overline{IOW}$ (WR THR) high to $\overline{TXRDY}$ high	C_L = 100 pF		195	ns

NOTE 6: When the transmitter interrupt delay is active, this delay si lengthened by one character time minus the last stop bit time.

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 9, 10, 11, 12 and 13)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time from stop to INT high	See Note 7		1	RCLK cycle
t_{pd5}	Propagation delay time from RCLK high to sample CLK high			100	ns
t_{pd6}	Propagation delay time from $\overline{IOR}$ (RD RBR/RD LSR) high to reset interrupt low	C_L = 100 pF		150	ns
t_{pd7}	Propagation delay time from $\overline{IOR}$ (RD RBR) low to $\overline{RXRDY}$ high			150	ns

NOTE 7: The receiver data available indication, the overrun error indication, the trigger level interrupts and the active $\overline{RXRDY}$ indication is delayed three RCLK cycles in the FIFO mode (FCR0 = 1). After the first byte has been received, status indicators (PE, FE, BI) is delayed three RCLK cycles. These indicators are updated immediately for any further bytes received after RD RBR goes active. There are eight RCLK cycle delays for trigger change level interrupts.

modem control switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 14)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd8}	Propagation delay time from $\overline{IOW}$ (WR MCR) high to $\overline{RTS}$ ($\overline{DTR}$) low/high	C_L = 100 pF		100	ns
t_{pd9}	Propagation delay time from modem input ($\overline{CTS}$, $\overline{DSR}$) low/high to interrupt high	C_L = 100 pF		170	ns
t_{pd10}	Propagation delay time from $\overline{IOR}$ (RD MSR) high to interrupt low	C_L = 100 pF		140	ns
t_{pd11}	Propagation delay time from $\overline{RI}$ high to interrupt high	C_L = 100 pF		170	ns

parallel port timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 15)

		MIN	MAX	UNIT
t_{su7}	Setup time, data valid before $\overline{STB}$ low	1		µs
t_{h6}	Hold time, data valid after $\overline{STB}$ high	1		µs
t_{w6}	Pulse duration, $\overline{STB}$ low	1	500	µs
t_{d10}	Delay time, BUSY high to $\overline{ACK}$ low	Defined by printer		
t_{d11}	Delay time, BUSY low to $\overline{ACK}$ low	Defined by printer		
t_{w6}	Pulse duration, $\overline{ACK}$ low	Defined by printer		
t_{w7}	Pulse duration, BUSY high	Defined by printer		
t_{d12}	Delay time, BUSY high after $\overline{STB}$ high	Defined by printer		

PARAMETER MEASUREMENT INFORMATION

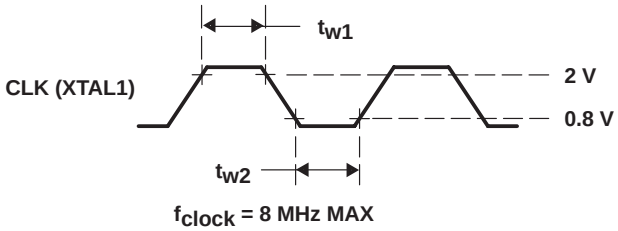
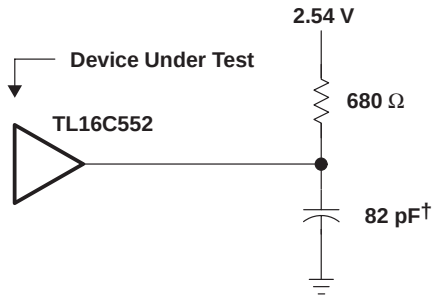


Figure 1. Clock Input (CLK) Voltage Waveform



†Includes scope and jig capacitance

Figure 2. Output Load Circuit

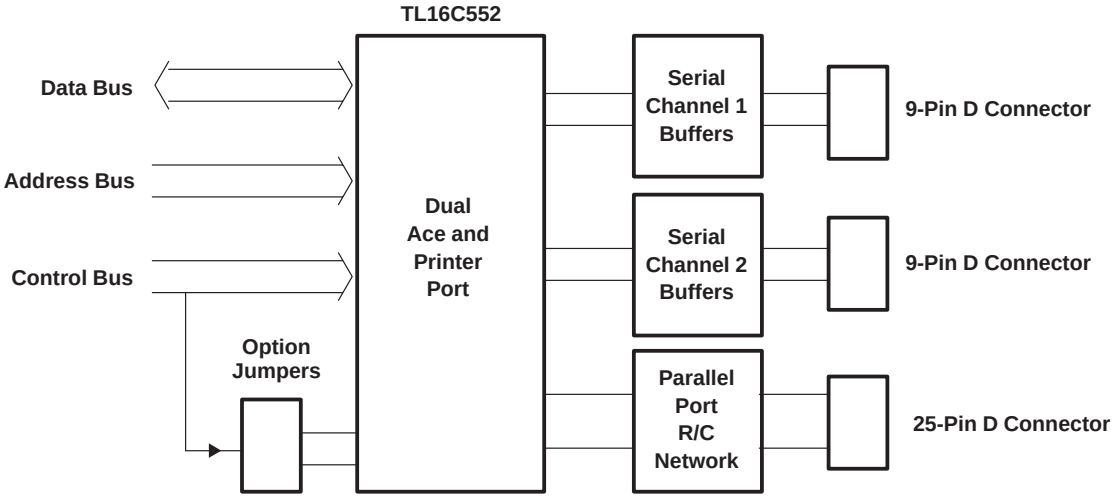


Figure 3. Basic Test Configuration

PARAMETER MEASUREMENT INFORMATION

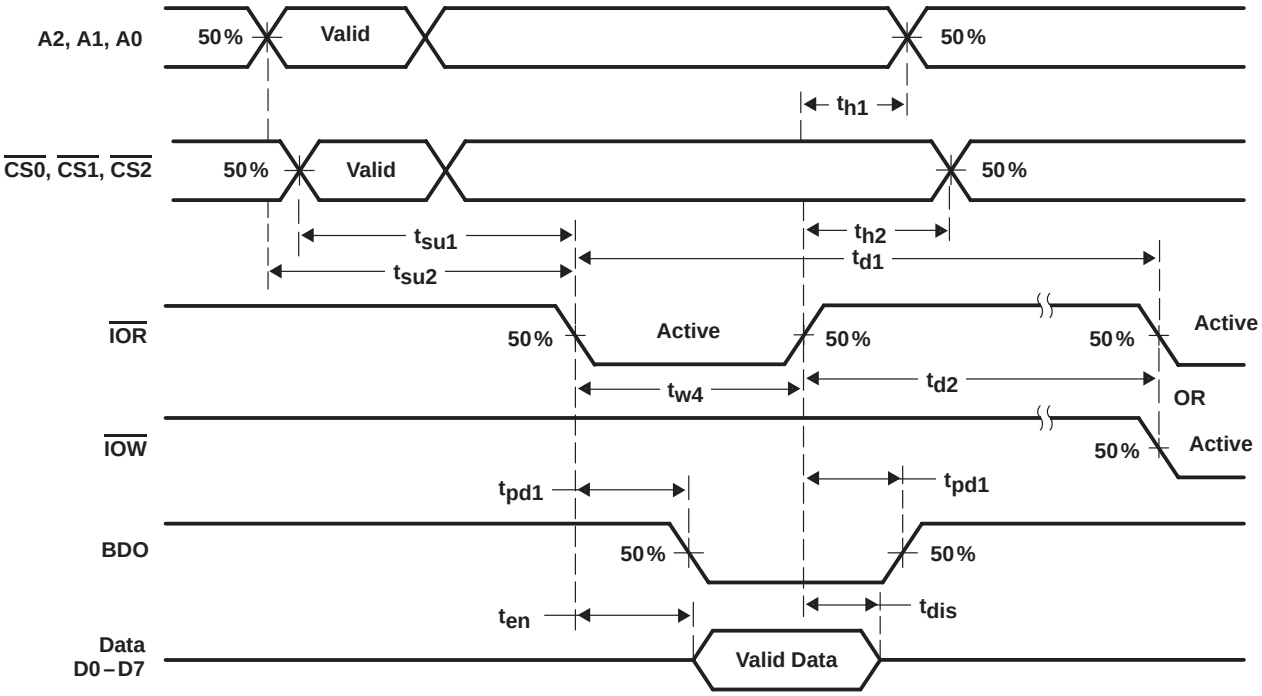


Figure 4. Read Cycle Timing Waveforms

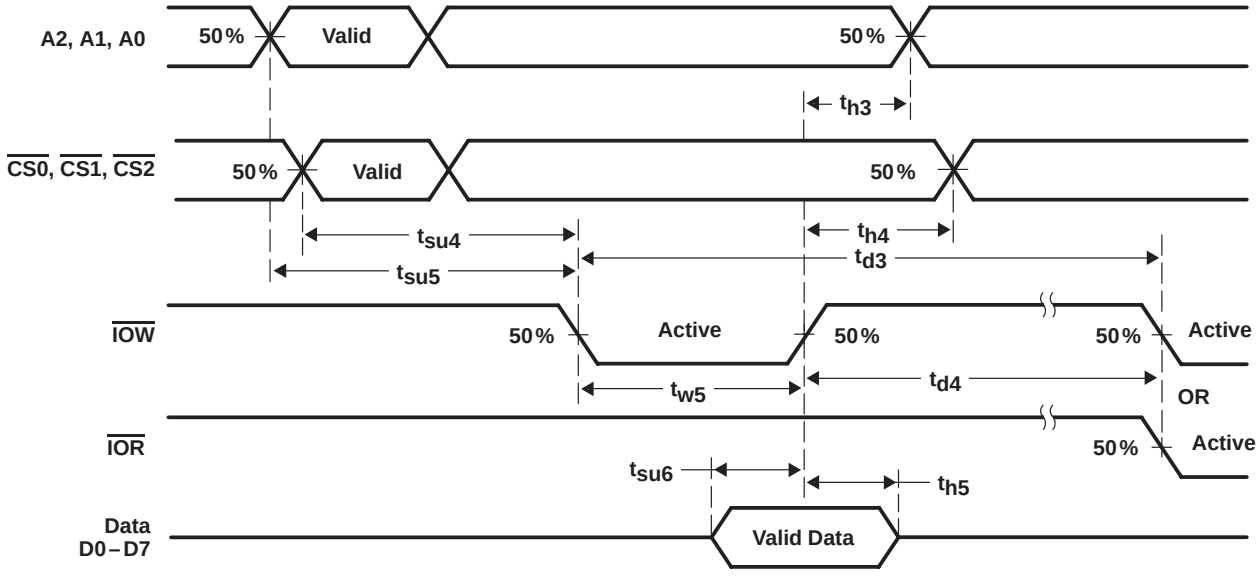


Figure 5. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

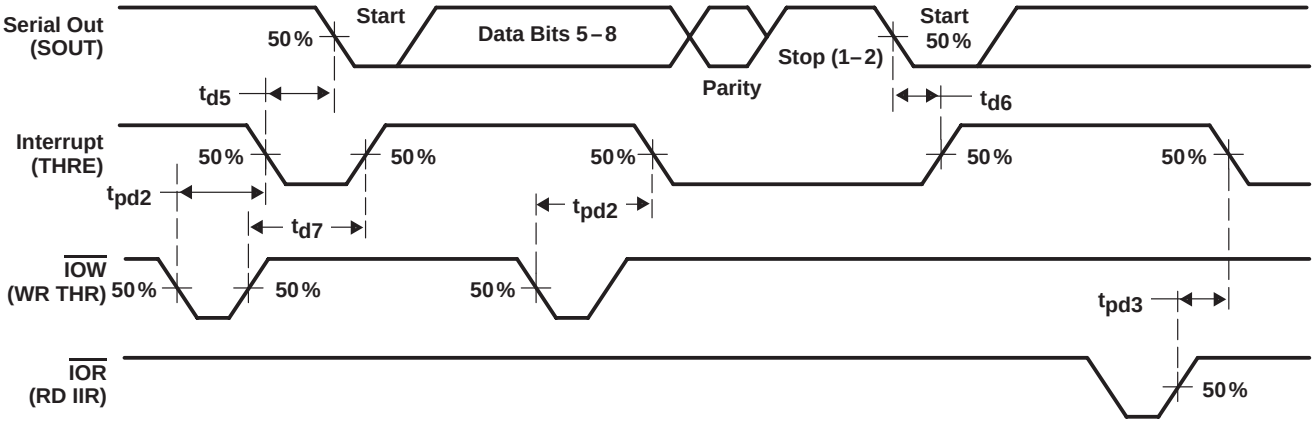


Figure 6. Transmitter Timing Waveforms

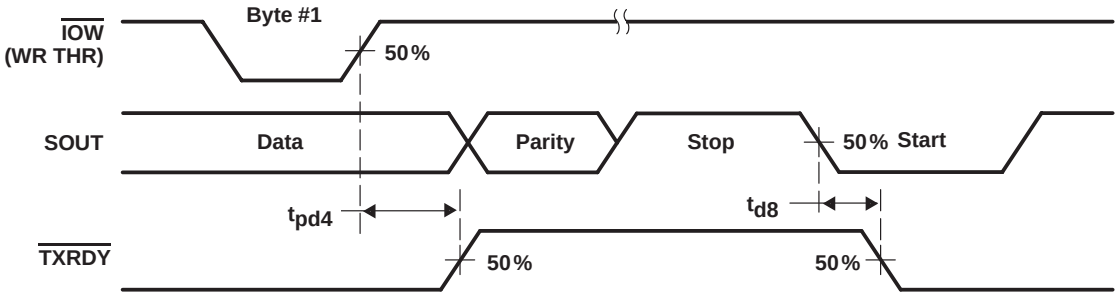


Figure 7. Transmitter Ready Mode 0 Timing Waveforms

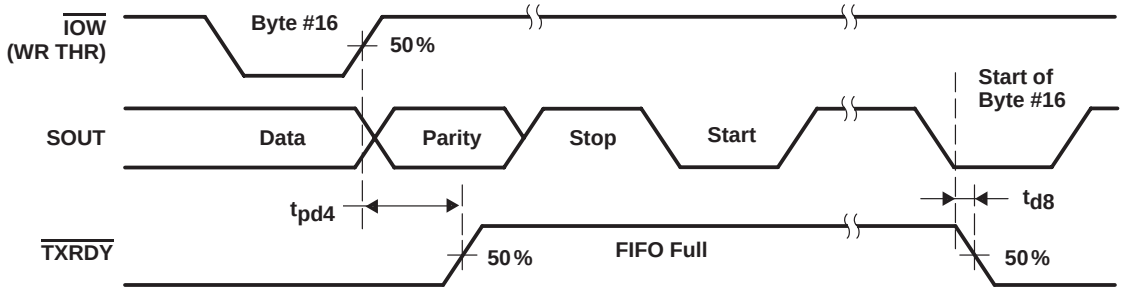


Figure 8. Transmitter Ready Mode 1 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

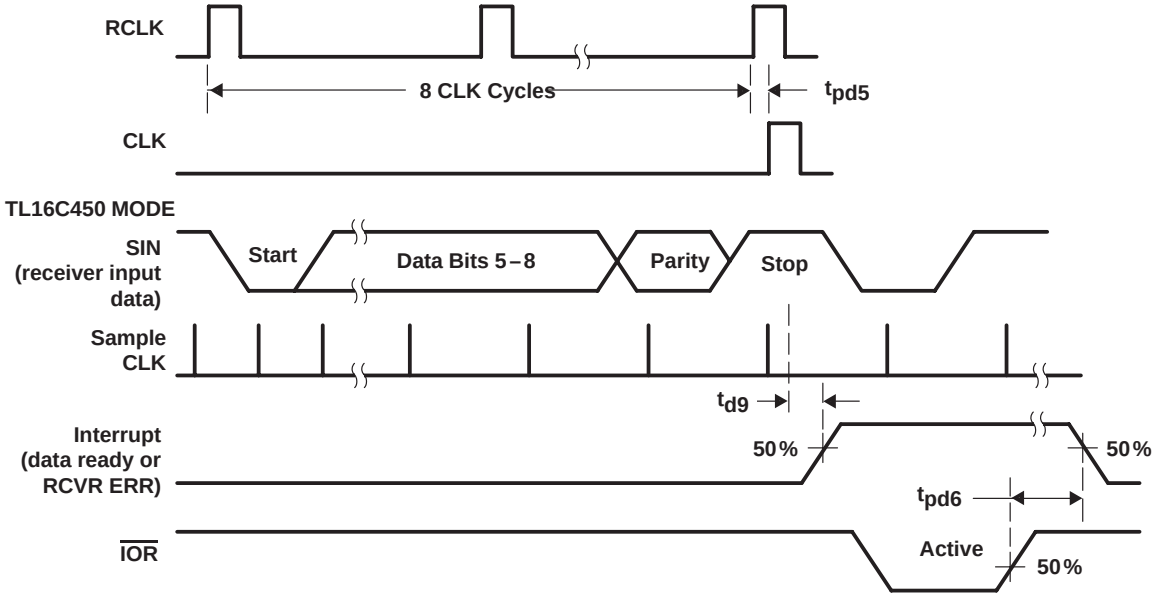


Figure 9. Receiver Timing Waveforms

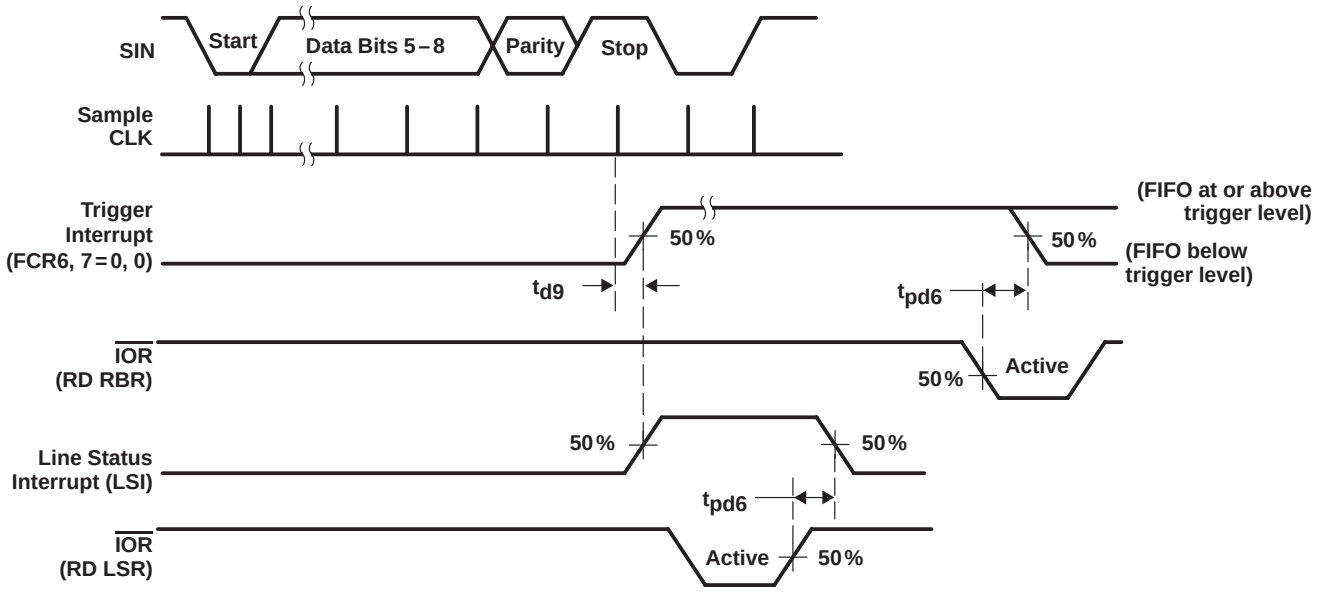


Figure 10. Receiver FIFO First Byte (Sets RDR) Waveforms

PARAMETER MEASUREMENT INFORMATION

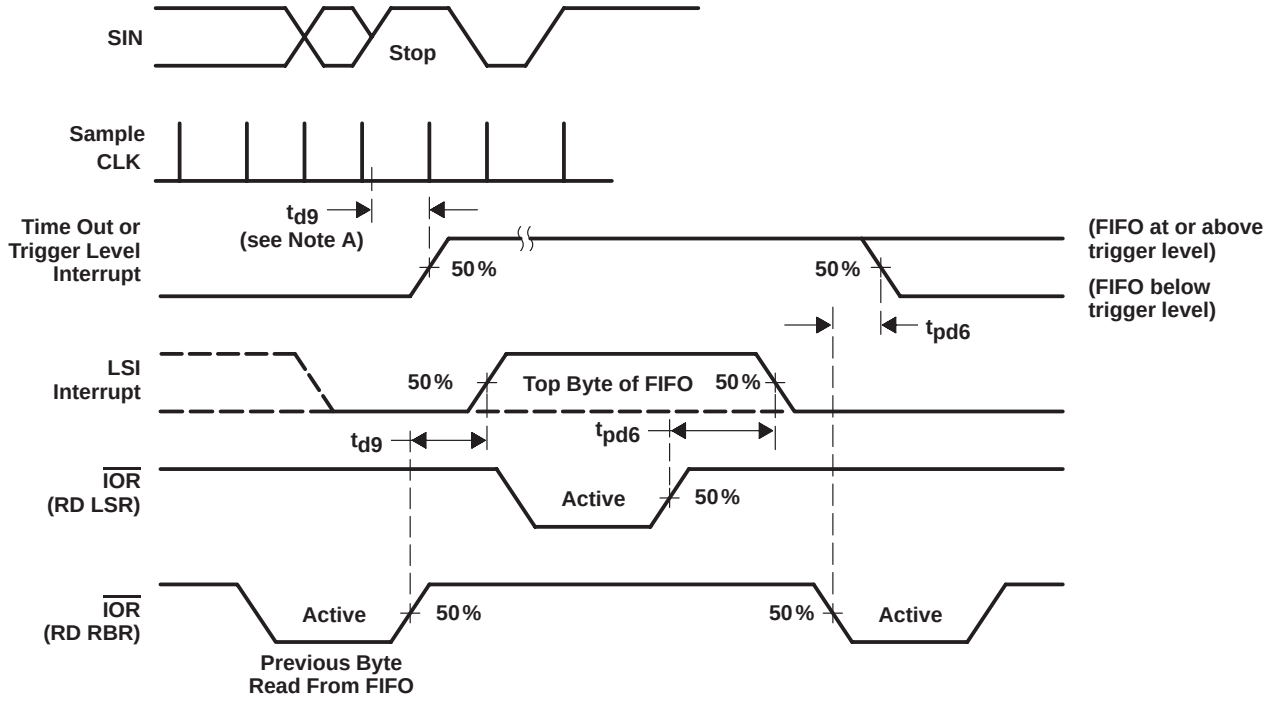


Figure 11. Receiver FIFO After First Byte (After RDR Set) Waveforms

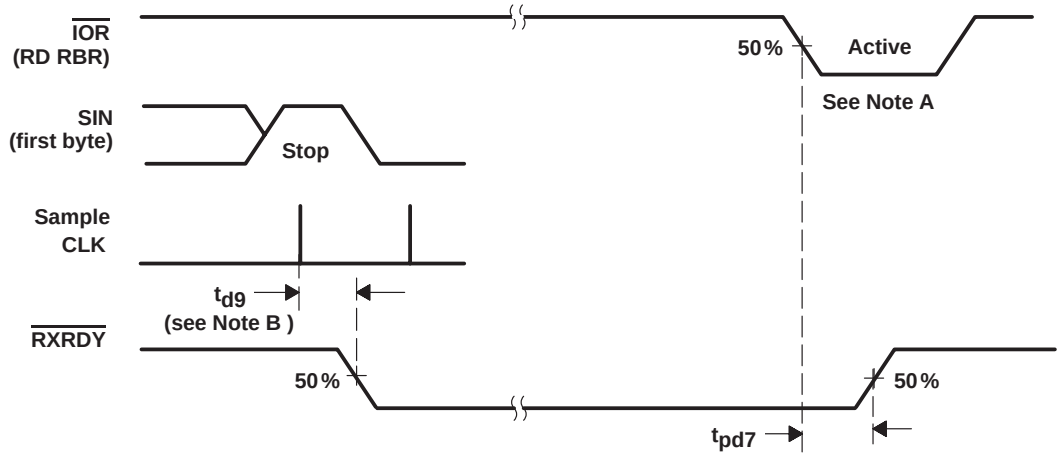
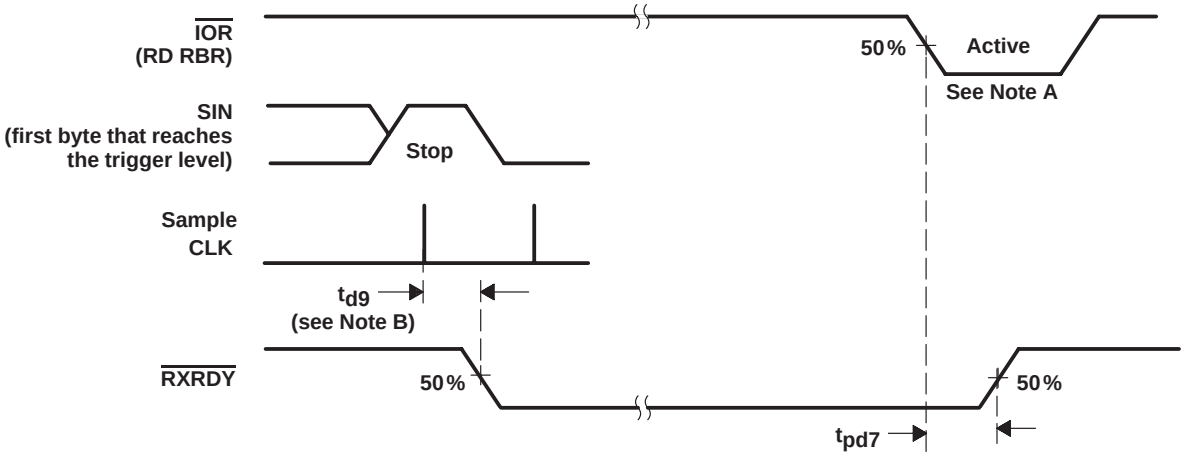


Figure 12. Receiver Ready Mode 0 Waveforms

NOTES: A. This is the reading of the last byte in the FIFO.
B. When FCR0=1, then t_{d9} = 3 RCLK cycles. For a time-out interrupt, t_{d9} = 8 RCLK cycles.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. When FCR0=1, then t_{d9} = 3 RCLK cycles. For a trigger change level interrupt, t_{d9} = 8 RCLK

Figure 13. Receiver Ready Mode 1 Waveforms

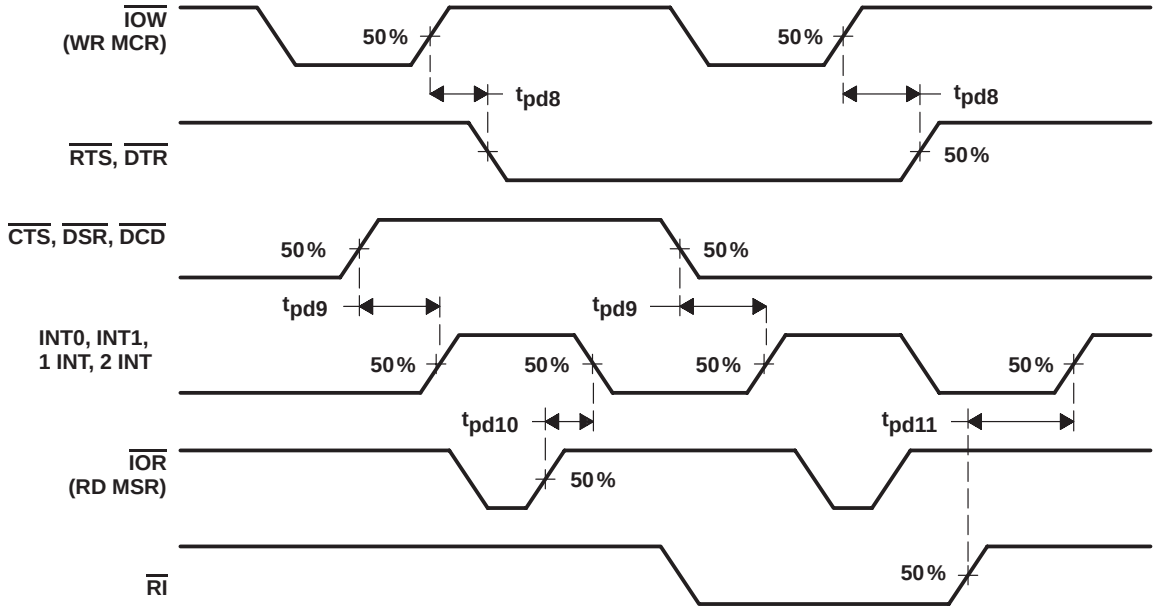


Figure 14. Modem Control Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

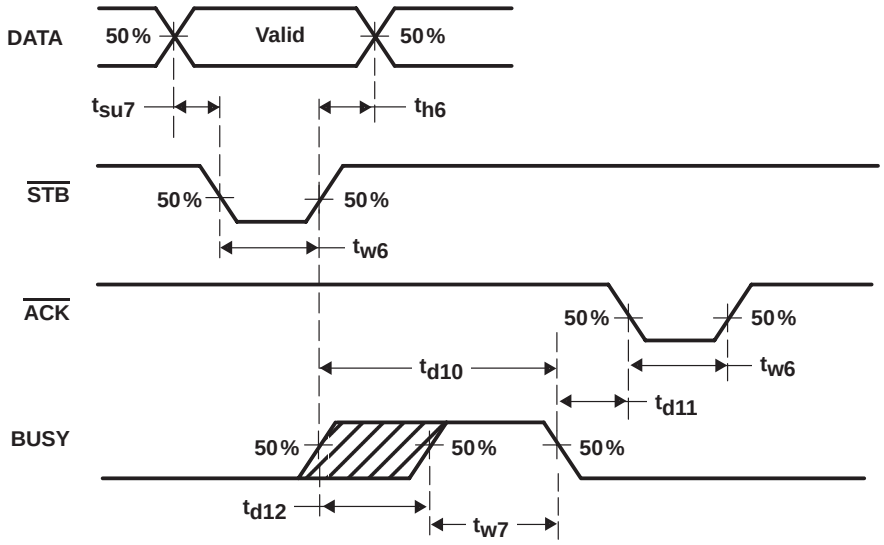


Figure 15. Parallel Port Timing Waveforms

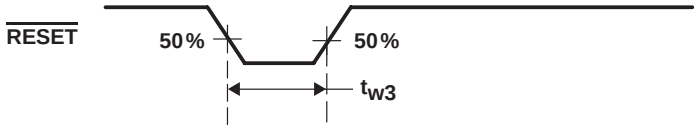


Figure 16. $\overline{\text{RESET}}$ Voltage Waveform

PRINCIPLES OF OPERATION

Three types of information are stored in the internal registers used in the ACE: control, status, and data. Mnemonic abbreviations are shown in the Table 1 for the registers.

Table 1. Internal Register Types With Mnemonics

CONTROL	MNEMONIC	STATUS	MNEMONIC	DATA	MNEMONIC
Line control register	LCR	Line status register	LSR	Receiver buffer register	RBR
FIFO control register	FCR	Modem status register	MSR	Transmitter holding register	THR
Modem control register	MCR				
Divisor latch LSB	DLL				
Divisor latch MSB	DLM				
Interrupt enable register	IER				

The address, read, and write inputs are used with the divisor latch access bit (DLAB) in the line control register (bit 7) to select the register to be written to or read from (see Table 2).

Table 2. Register Selection†‡

DLAB	A2	A1	A0	MNEMONIC	REGISTER
L	L	L	L	RBR	Receiver buffer register (read only)
L	L	L	L	THR	Transmitter holding register (write only)
L	L	L	H	IER	Interrupt enable register
X	L	H	L	IIR	Interrupt identification register (read only)
X	L	H	L	FCR	FIFO control register (write only)
X	L	H	H	LCR	Line control register
X	H	L	L	MCR	Modem control register
X	H	L	H	LSR	Line status register
X	H	H	L	MSR	Modem status register
X	H	H	H	SCR	Scratch register
H	L	L	L	DLL	Divisor latch (LSB)
H	L	L	H	DLM	Divisor latch (MSB)

† X = irrelevant, L = low level, H = high level
‡ The serial channel is accessed when either $\overline{CS0}$ or $\overline{CS1}$ is low.

Individual bits within the registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR7 refers to line control register bit 7.

The transmitter buffer register and receiver buffer register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double buffered so that read and write operations may be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 2. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

ADDRESS	REGISTER MNEMONIC	REGISTER BIT NUMBER							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RBR (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (write only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0†	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1†	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable modem status interrupt	(ERLSI) Enable receiver line status interrupt	(ETBEI) Enable transmitter holding register empty interrupt	(ERBFI) Enable received data available interrupt
2	FCR (write only)	Receiver Trigger (MSB)	Receiver Trigger (LSB)	Reserved	Reserved	DMA mode select	Tranmitter FIFO reset	Receiver FIFO reset	FIFO Enable
2	IIR (read only)	FIFOs Enabled‡	FIFOs Enabled‡	0	0	Interrupt ID Bit (2)‡	Interrupt ID Bit (1)	Interrupt ID Bit (0)	0 If interrupt pending
3	LCR	(DLAB) Divisor latch access bit	Set break	Stick parity	(EPS) Even parity select	(PEN) Parity enable	(STB) Number of stop bits	(WLSB1) Word length select bit 1	(WLSB0) Word length select bit 0
4	MCR	0	0	0	Loop	Enable external interrupt (INT0 or INT1)	OUT1 (an unused internal signal)	(RTS) Request to send	(DTR) Data terminal ready
5	LSR	Error in receiver FIFO‡	(TEMT) Transmitter empty	(THRE) Transmitter holding register empty	(BI) Break interrupt	(FE) Framing error	(PE) Parity error	(OE) Overrun error	(DR) Data ready
6	MSR	(DCD) Data carrier detect	(RI) Ring indicator	(DSR) Data set ready	(CTS) Clear to send	(ΔDCD) Delta data carrier detect	(TERI) Trailing edge ring indicator	(ΔDSR) Delta data set ready	(ΔCTS) Delta clear to send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

† DLAB = 1
‡ These bits are always 0 when FIFOs are disabled.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

This write-only register is at the same location as the IIR. It enables and clears the FIFOs, sets the trigger level of the receiver FIFO, and selects the type of DMA signaling. The contents of FCR are described in Table 3 and the following bulleted list.

- Bit 0: FCR0 enables both the transmitter and receiver FIFOs. All bytes in both FIFOs can be reset by clearing FCR0. Data is cleared automatically from the FIFOs when changing from the FIFO mode to the TL16C450 mode and vice versa. Programming of other FCR bits is enabled by setting FCR0=1.
- Bit 1: FCR1=1 clears all bytes in the receiver FIFO and resets the counter. This does not clear the shift register.
- Bit 2: FCR2=1 clears all bytes in the transmitter FIFO and resets the counter. This does not clear the shift register.
- Bit 3: FCR3=1 changes the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ terminals from mode 0 to mode 1 when FCR0=1.
- Bits 4 and 5: These two bits are reserved for future use.
- Bits 6 and 7: These two bits set the trigger level for the receiver FIFO interrupt as shown in Table 4.

Table 4. Receiver FIFO Trigger Level

BIT		RECEIVER FIFO TRIGGER LEVEL (BYTES)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

The following receiver status occurs when the receiver FIFO and receiver interrupts are enabled:

1. LSR0 is set when a character is transferred from the shift register to the receiver FIFO. When the FIFO is empty, it is cleared.
2. IIR = 06 receiver line status interrupt has higher priority than the received data available interrupt IIR = 04.
3. Receive data available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. As soon as the FIFO drops below its programmed trigger level, it is cleared.
4. IIR = 04 (receive data available indication) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following receiver FIFO character time-out status occurs when receiver FIFO and receiver interrupts are enabled.

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

1. A FIFO timeout interrupt occurs when the following conditions exist:
   a. Minimum of one character in FIFO
   b. Last received serial character was longer than four continuous previous character times ago (if two stop bits are programmed, the second one is included in the time delay).
   c. The last CPU read of the FIFO was more than four continuous character times earlier. At 300 baud and 12-bit characters, the FIFO time-out interrupt causes a latency of 160 ms maximum from received character to interrupt issued.
2. By using the RCLK input for a clock signal, the character times can be calculated. (The delay is proportional to the baud rate.)
3. The time-out timer is reset after the CPU reads the receiver FIFO or after a new character is received, when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the receiver FIFO.

Transmitter interrupts occur as follows when the transmitter and transmitter FIFO interrupts are enabled (FCRO = 1, IER = 1).

1. When the transmitter FIFO is empty, the THR interrupt (IIR = 02) occurs. The interrupt is cleared as soon as the THR is written to or the IIR is read. One to sixteen characters can be written to the transmit FIFO when servicing this interrupt.
2. The transmitter FIFO empty indications are delayed one character time minus the last stop bit time whenever the following occurs:

   THRE = 1 and there has not been a minimum of two bytes at the same time in transmitter FIFO, since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate, however, assuming it is enabled.

Receiver FIFO trigger level and character time-out interrupts have the same priority as the received data available interrupt. The THRE interrupt has the same priority as the transmitter FIFO empty interrupt.

FIFO polled mode operation

Clearing IER0, IER1, IER2, IER3, or all, with FCR0 = 1, puts the ACE into the FIFO polled mode. Receiver and transmitter are controlled separately. Therefore, either or both can be in the polled mode.

In the FIFO polled mode, there is no time-out condition indicated or trigger level reached. However, the receiver and transmitter FIFOs still have the capability of holding characters. The LSR must be read to determine the ACE status.

interrupt enable register (IER)

The IER independently enables the four serial channel interrupt sources that activate the interrupt (INT0 or INT1) output. All interrupts are disabled by clearing IER0 – IER3. Interrupts are enabled by setting the appropriate bits of the IER. Disabling the interrupt system inhibits the IIR and the active (high) interrupt output. All other system functions operate in their normal manner, including the setting of the LSR and MSR. The contents of the IER are described in Table 3 and in the following bulleted list.

- Bit 0: IER0, when set, enables the received data available interrupt and the time-out interrupts in the FIFO mode.

PRINCIPLES OF OPERATION

interrupt enable register (IER) (continued)

- Bit 1: IER1, when set, enables the THRE interrupt.
- Bit 2: IER2, when set, enables the receiver line status interrupt.
- Bit 3: IER3, when set, enables the modem status interrupt.
- Bits 4 – 7: IER4 – IER7 are always cleared.

interrupt identification register (IIR)

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are shown in the following bulleted list:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the IIR. The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 5.

Table 5. Interrupt Control Functions

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	–	None	None	–
0	1	1	0	First	Receiver line status	OE, PE, FE, or BI	LSR read
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	RBR read until FIFO drops below the trigger level
1	1	0	0	Second	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time.	RBR read
0	0	1	0	Third	THRE	THRE	IIR read if THRE is the interrupt source or THR write
0	0	0	0	Fourth	Modem status	$\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{RI}}$, or $\overline{\text{DCD}}$	MSR read

- Bit 0: IIR0 indicates whether an interrupt is pending. When IIR0 is cleared, an interrupt is pending.
- Bits 1 and 2: IIR1 and IIR2 identify the highest priority interrupt pending as indicated in Table 5.
- Bit 3: IIR3 is always cleared when in the TL16C450 mode. This bit is set along with bit 2 when in the FIFO mode and a trigger change level interrupt is pending.
- Bits 4 and 5: IIR4 and IIR5 are always cleared.
- Bits 6 and 7: IIR6 and IIR7 are set when FCR0=1.

PRINCIPLES OF OPERATION

line control register (LCR)

The format of the data character is controlled by the LCR. The LCR may be read. Its contents are described in the following bulleted list and shown in Figure 17.

- Bits 0 and 1: LCR0 and LCR1 are the word length select bits. The number of bits in each serial character is programmed as shown in Figure 17.
- Bit 2: LCR2 is the stop bit select bit. LCR2 specifies the number of stop bits in each transmitted character as shown in Figure 17. The receiver always checks for one stop bit.
- Bit 3: LCR3 is the parity enable bit 3. When LCR3 is high, a parity bit between the last data word bit and stop bit is generated and checked.
- Bit 4: LCR4 is the even parity select bit 4. When enabled, setting this bit selects even parity.
- Bit 5: LCR5 is the stick parity bit 5. When parity is enabled (LCR3=1), LCR5=1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR4. This forces parity to a known state and allows the receiver to check the parity bit in a known state.
- Bit 6: LCR6 is the break control bit 6. When LCR6 is set, the serial output (SOUT1 and SOUT0) is forced to the spacing state (low). The break control bit acts only on the serial output and does not affect the transmitter logic. When the following sequence is used, no invalid characters are transmitted because of the break:

  Step 1. Load a zero byte in response to the transmitter holding register empty (THRE) status indication.

  Step 2. Set the break in response to the next THRE status indication.

  Step 3. Wait for the transmitter to be idle when transmitter empty status signal is set high (TEMT=1). Then clear the break when the normal transmission has to be restored.

- Bit 7: LCR7 is the divisor latch access bit (DLAB) bit 7. Bit 7 must be set to access the divisor latches DLL and DLM of the baud rate generator during a read or write operation. LCR7 must be cleared to access the receiver buffer register, the transmitter holding register or the interrupt enable register.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

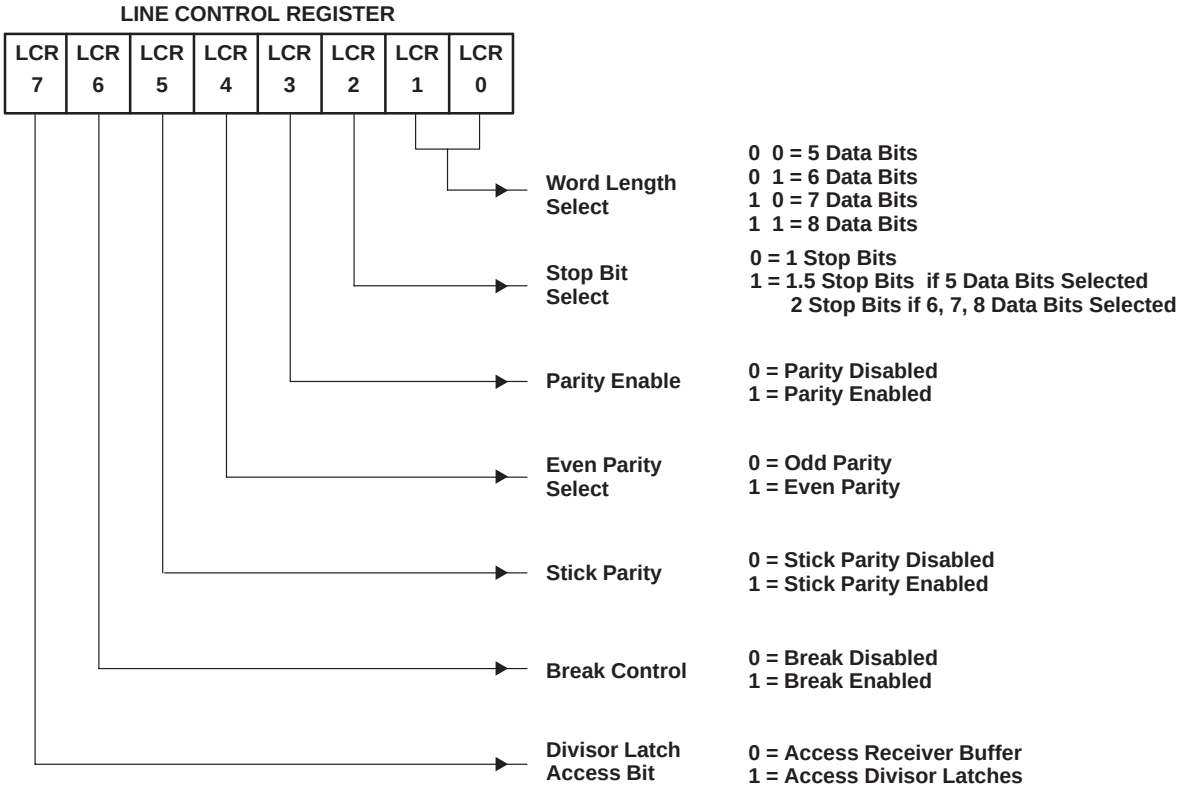


Figure 17. Line Control Register Contents

line printer port (LPT)

The line printer port contains the functionality of the port included in the TL16C452, but offers a hardware programmable extended mode controlled by the printer enhancement mode (PEMD) terminal. This enhancement is the addition of a direction control bit, and an interrupt status bit.

register 0 line printer data register (LPD)

The LPD port is either output only or bidirectional, depending on the state of the extended mode terminal and data direction control bits.

- Compatibility mode (PEMD is low). Reads to the LPD register return the last data that was written to the port. Write operations immediately output data to the PD0–PD7 terminals.
- Extended mode (PEMD is high). Read operations return either the data last written to the LPT data register when the direction bit is cleared to write, or the data that is present on PD0–PD7 when the direction is set to read. Writes to the LPD register latch data into the output register, but only drive the LPT port when the direction bit is cleared to write.

PRINCIPLES OF OPERATION

line printer port (LPT) (continued)

Table 6 summarizes the possible combinations of extended mode and the direction control bit. In either case, the bits of the LPD register are defined as follows:

Table 6. Extended Mode and Direction Control Bit Combinations

PEMD	DIR	PD0 – PD7 FUNCTION
L	X	PC/AT mode – output
H	0	PS/2™ mode – output
H	1	PS/2™ mode – input

register 1 read line printer status register

The line printer status (LPS) register is a read-only register that contains interrupt and printer status of the LPT connector terminals. In Table 7 (in the default column), are the values of each bit after reset in the case of the printer being disconnected from the port.

Table 7. LPS Register Bit Description

BIT	DESCRIPTION	DEFAULT
0	Reserved	1
1	Reserved	1
2	$\overline{\text{PRINT}}$	1
3	$\overline{\text{ERR}}$	†
4	SLCT	†
5	PE	†
6	$\overline{\text{ACK}}$	†
7	$\overline{\text{BSY}}$	†

† Outputs are dependent upon device inputs.

- Bits 0 and 1: These bits are reserved and are always set.
- Bit 2: This bit is the printer interrupt ($\overline{\text{PRINT}}$, active low) status bit. When cleared indicates that the printer has acknowledged the previous transfer with an ACK handshake (bit 4 of the control register is set). The bit is cleared on the active to inactive transition of the $\overline{\text{ACK}}$ signal. This bit is set after a read of the status port.
- Bit 3: This bit is the error ($\overline{\text{ERR}}$, active low) status bit corresponds to $\overline{\text{ERR}}$ input.
- Bit 4: This bit is the select (SLCT) status bit corresponds to SLCT input.
- Bit 5: This bit is the paper empty (PE) status bit corresponds to PE input.
- Bit 6: This bit is the acknowledge ($\overline{\text{ACK}}$, active low) status bit corresponds to $\overline{\text{ACK}}$ input.
- Bit 7: This bit is the busy ($\overline{\text{BSY}}$, active low) status bit corresponds to BUSY input (active high).

register 2 line printer control (LPC) register

The LPC register is read/write port that controls the PD0 – PD7 direction and drive the printer control lines. Write operations set or clear these bits, while read operations return the state of the last write operation to this register. The bits in this register are described in Table 8.

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PRINCIPLES OF OPERATION

line printer port (LPT) (continued)

Table 8. LPC Register Bit Description

BIT	DESCRIPTION
0	STB
1	AFD
2	$\overline{\text{INIT}}$
3	SLIN
4	INT2 EN
5	DIR
6	Reserved (0)
7	Reserved (0)

- Bit 0: This bit is the printer strobe (STB) control bit. When this bit is set, the $\overline{\text{STB}}$ signal is asserted on the LPT interface. When STB is cleared, the signal is negated.
- Bit 1: This bit is the auto feed (AFD) control bit. When this bit is set, the $\overline{\text{AFD}}$ signal is asserted on the LPT interface. When AFD is cleared, the signal is negated.
- Bit 2: This bit is the initialize printer ($\overline{\text{INIT}}$) control bit. When this bit is set, the $\overline{\text{INIT}}$ signal is negated. When $\overline{\text{INIT}}$ is cleared, the $\overline{\text{INIT}}$ signal is asserted on the LPT interface.
- Bit 3: This bit is the select input (SLIN) control bit. When this bit is set, the SLCT signal is asserted on the LPT interface. when SLIN is cleared, the signal is negated.
- Bit 4: This bit is the interrupt request enable (INT2 EN) control bit. When set, this bit enables interrupts from the LPT port whenever the $\overline{\text{ACK}}$ signal is released. When cleared, INT2 EN disables interrupts and places INT2 signal in 3-state.
- Bit 5: This bit is the direction (DIR) control bit (only used when PEMD is high). When this bit is set, the output buffers in the LPD port are disabled allowing data driven from external sources to be read from the LPD port. When DIR is cleared, the LPD port is in output mode.

line status register (LSR)

The LSR is a single register that provides status indications. The LSR is shown in Table 9 and is described in the following bulleted list.

Table 9. Line Status Register Bits

LSR BITS	1	0
LSR0 data ready (DR)	Ready	Not ready
LSR1 overrun error (OE)	Error	No error
LSR2 parity error (PE)	Error	No error
LSR3 framing error (FE)	Error	No error
LSR4 break interrupt (BI)	Break	No break
LSR5 THRE	Empty	Not empty
LSR6 transmitter empty (TEMT)	Empty	Not empty
LSR7 receiver FIFO error	Error in FIFO	No error in FIFO

† LSR is intended only for factory test. It should be considered as read only by applications software.

PRINCIPLES OF OPERATION

line status register (LSR) (continued)

- Bit 0: LSR0 is the data ready (DR) bit. DR is set high when an incoming character has been received and transferred into the receiver buffer register or the FIFO. LSR0 is cleared by a CPU read of the data in the receiver buffer register or the FIFO.
- Bit 1: SR1 is the overrun error (OE) bit. OE indicates that data in the receiver buffer register was not read by the CPU before the next character was transferred into the receiver buffer register overwriting the previous character. The OE indicator is cleared whenever the CPU reads the contents of the LSR. An OE occurs in the FIFO mode after the FIFO is full and the next character is completely received. The OE is detected by the CPU on the first LSR read after the overrun happens. The character in the shift register is not transferred to the FIFO but it is overwritten.
- Bit 2: LSR2 is the parity error (PE) bit. PE indicates that the received data character does not have the correct parity as selected by LCR3 and LCR4. The PE bit is set upon detection of a parity error and is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO. LSR2 reflects the error when the character is at the top of the FIFO.
- Bit 3: LSR3 is the framing error (FE) bit. FE indicates that the received character did not have a valid stop bit. LSR3 is set when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the framing error is associated with a particular character in the FIFO. LSR3 reflects the error when the character is at the top of the FIFO.
- Bit 4: LSR4 is the break interrupt (BI) bit. BI is set when the received data input is held in the spacing (cleared) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, this is associated with a particular character in the FIFO. LSR2 reflects the BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR1 – LSR4 are the error conditions that produce a receiver line status interrupt (priority 1 interrupt in the interrupt identification register) when any of the conditions are detected. This interrupt is enabled by setting IER2=1 in the interrupt enable register.

- Bit 5: LSR5 is the THRE bit. THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set when a character is transferred from the transmitter holding register (THR) into the transmitter shift register (TSR). LSR5 is cleared by the loading of the transmitter holding register by the CPU. LSR5 is not reset by a CPU read of the LSR. In the FIFO mode when the transmitter FIFO is empty, this bit is set. It is cleared when one byte is written to the transmitter FIFO. When the THRE interrupt is enabled by IER1, THRE causes a priority 3 interrupt in the IIR. When THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.
- Bit 6: LSR6 is the transmitter empty (TEMT) bit. TEMT is set when the THR and the TSR are both empty. LSR6 is cleared when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not cleared by a CPU read of the LSR. In the FIFO mode, when both the transmitter FIFO and shift register are empty, this bit is set.
- Bit 7: LSR7 is the receiver FIFO error bit. The LSR7 bit is always cleared in the TL16C450 mode. In FIFO mode, it is set when at least one of the following data errors is in the FIFO: PE, FE, or BI indication. It is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.

PRINCIPLES OF OPERATION

master reset

After power up, the ACE $\overline{\text{RESET}}$ input should be held low for one microsecond to reset the ACE circuits to an idle mode until initialization. A low on $\overline{\text{RESET}}$ causes the following:

1. It initializes the transmitter and receiver clock counters.
2. It clears the LSR, except for TEMT and THRE, which are set. The MCR is also cleared. All of the discrete lines, memory elements, and miscellaneous logic associated with these register bits are also cleared or turned off. The LCR, divisor latches, RBR, and transmitter buffer register are not effected.

Following the removal of the reset condition ($\overline{\text{RESET}}$ high), the ACE remains in the idle mode until programmed.

A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE. A summary of the affect of a reset on the ACE is given in Table 10.

Table 10. $\overline{\text{RESET}}$ Affects On Registers and Signals

REGISTER/SIGNAL	RESET CONTROL	RESET
Interrupt enable register	Reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt identification register	Reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 cleared Bits 4–5 are permanently cleared
Line control register	Reset	All bits cleared
Modem control register	Reset	All bits cleared
FIFO control register	Reset	All bits cleared
Line status register	Reset	All bits cleared, except bits 5 and 6 are set
Modem status register	Reset	Bits 0–3 cleared, bits 4–7 input signal
SOUT	Reset	High
Interrupt (receiver errs)	Read LSR/Reset	Cleared
Interrupt (receiver data ready)	Read RBR/Reset	Cleared
Interrupt (THRE)	Read IIR/Write THR/Reset	Cleared
Interrupt (modem status changes)	Read MSR/Reset	Cleared
$\overline{\text{OUT2}}$	Reset	High
$\overline{\text{RTS}}$	Reset	High
$\overline{\text{DTR}}$	Reset	High
$\overline{\text{OUT1}}$	Reset	High

PRINCIPLES OF OPERATION

modem control register (MCR)

The MCR controls the interface with the modem or data set as described in Figure 18. The MCR can be written to and read from. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output terminals. MCR bits 0, 1, 2, 3, and 4 are shown as follows:

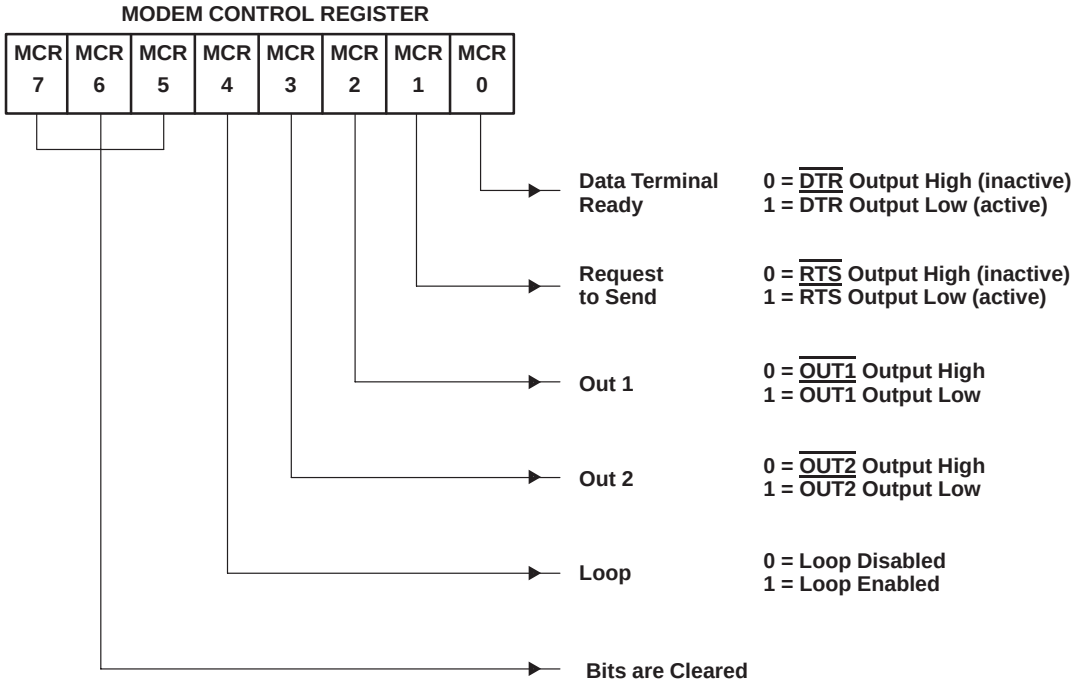

Figure 18. Modem Control Register Contents

- Bit 0: When MCR0 is set, the $\overline{DTR}$ output is forced low. When MCR0 is cleared, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the serial channel can be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.
- Bit 1: When MCR1 is set, the $\overline{RTS}$ output is forced low. When MCR1 is cleared, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the serial channel can be input into an inverting line driver to obtain the proper polarity input at the modem or data set.
- Bit 2: When MCR2 is set, $\overline{OUT1}$ is forced low.
- Bit 3: When MCR3 is set, the $\overline{OUT2}$ output is forced low.
- Bit 4: MCR4 provides a local loopback feature for diagnostic testing of the channel. When MCR4 is set, serial output (SOUT) is set to the marking (high) state, and the SIN is disconnected. The output of the TSR is looped back into the receiver shift register input. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected. The modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OIUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs. The modem control output terminals are forced to their inactive state (high) on the TL16C552. In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Interrupt control is fully operational. However, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external terminals represented by those four bits.
- Bits 5 – 7: These three bits(MCR5 – MCR7) are permanently cleared.

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modem status register (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the ACE in addition to the current status of four bits of the MSR that indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set when a control input from the modem changes state and cleared when the CPU reads the MSR.

The modem input lines are $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$. MSR4 – MSR7 are status indications of these lines. A status bit = 1 indicates the input is a low. A status bit = 0 indicates the input is high. When the modem status interrupt in the interrupt enable register is enabled (IER3), an interrupt is generated whenever MSR0 – MSR3 is set. The MSR is a priority 4 interrupt. The contents of the MSR are described in Table 11.

Table 11. Modem Status Register Bits

MSR BIT	MNEMONIC	DESCRIPTION
MSR0	ΔCTS	Delta clear to send
MSR1	ΔDSR	Delta data set ready
MSR2	TERI	Trailing edge of ring indicator
MSR3	ΔDCD	Delta data carrier detect
MSR4	$\overline{CTS}$	Clear to send
MSR5	$\overline{DSR}$	Data set ready
MSR6	$\overline{RI}$	Ring indicator
MSR7	$\overline{DCD}$	Data carrier detect

- Bit 0: MSR0 is the delta clear to send (ΔCTS) bit. ΔCTS displays that the $\overline{CTS}$ input to the serial channel has changed state since it was last read by the CPU.
- Bit 1: MSR1 is the delta data set ready (ΔDSR) bit. ΔDSR indicates that the $\overline{DSR}$ input to the serial channel has changed state since the last time it was read by the CPU.
- Bit 2: MSR2 is the trailing edge of ring indicator (TERI) bit. TERI indicates that the $\overline{RI}$ input to the serial channel has changed states from low to high since the last time it was read by the CPU. High-to-low transitions on RI do not activate TERI.
- Bit 3: MSR3 is the delta data carrier detect (ΔDCD) bit. ΔDCD indicates that the $\overline{DCD}$ input to the serial channel has changed state since the last time it was read by the CPU.
- Bit 4: MSR4 is the clear to send (CTS) bit. CTS is the complement of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from SOUT. When the serial channel is in the loop mode ((MCR4 = 1), MSR4 reflects the value of RTS in the MCR.
- Bit 5: MSR5 is the data set ready (DSR) bit. DSR is the complement of the $\overline{DSR}$ input from the modem to the serial channel that indicates that the modem is ready to provide received data to the serial channel receiver circuitry. When the channel is in the loop mode (MCR4=1), MSR5 reflects the value of DTR in the MCR.
- Bit 6: MSR6 is the ring indicator (RI) bit. RI is the complement of the $\overline{RI}$ input. When the channel is in the loop mode (MCR4=1), MSR6 reflects the value of $\overline{OUT1}$ in the MCR.
- Bit 7: MSR7 is the data carrier detect (DCD) bit. DCD indicates the status of the data carrier detect ($\overline{DCD}$) input. When the channel is in the loop mode (MCR4=1), MSR7 reflects the value of OUT2 in the MCR.

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modem status register (MSR) (continued)

Reading the MSR register clears the delta modem status indications but has no affect on the other status bits. For LSR and MSR, the setting of status bits is inhibited during status register read operations. When a status condition is generated during a read $\overline{IOR}$ operation, the status bit is not set until the trailing edge of the read. If a status bit is set during a read operation, and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again. In the loop back mode, when modem status interrupts are enabled, the $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$ input terminals are ignored. However, a modem status interrupt can still be generated by writing to MCR3 – MCR0. Applications software should not write to the MSR.

parallel port registers

The TL16C552 parallel port can interface to the device to a Centronics-style printer interface. When chip select 2 ($\overline{CS2}$) is low, the parallel port is selected. Table 12 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read ($\overline{IOR}$) and write ($\overline{IOW}$) terminal as shown. The read data register allows the microprocessor to read the information on the parallel bus.

The read status register allows the microprocessor to read the status of the printer in the six most significant bits. The status bits are printer busy $\overline{BSY}$, acknowledge ($\overline{ACK}$) which is a handshake function, paper empty (PE), printer selected ($\overline{SLCT}$), error ($\overline{ERR}$) and printer interrupt ($\overline{PRINT}$). The read control register allows the state of the control lines to be read. The write control register sets the state of the control lines. They are direction (DIR), interrupt enable (INT2 EN), select in ($\overline{SLIN}$), initialize the printer ($\overline{INIT}$), autofeed the paper ($\overline{AFD}$), and strobe ($\overline{STB}$), which informs the printer of the presence of a valid byte on the parallel bus. The write data register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel port implementation used in the IBM™ serial parallel adaptor.

Table 12. Parallel Port Registers

REGISTER	REGISTER BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	$\overline{BSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERR}$	$\overline{PRINT}$	1	1
Read Control	0	0	DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	0	0	DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB

Table 13. Parallel Port Register Select

CONTROL TERMINALS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{CS2}$	A1	A0	
L	H	L	L	L	Read data
L	H	L	L	H	Read status
L	H	L	H	L	Read control
L	H	L	H	H	Invalid
H	L	L	L	L	Write data
H	L	L	L	H	Invalid
H	L	L	H	L	Write control
H	L	L	H	H	Invalid

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programmable baud generator

The ACE serial channel contains a programmable baud rate generator that divides the clock (dc to 8 MHz) by any divisor from 1 to ($2^{16}-1$). The output frequency of the baud rate generator is 16× the data rate (divisor # = clock ÷ (baud rate × 16)) referred to in this document as RCLK. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These divisor latch registers must be loaded during initialization. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The baud rate generator can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50- to 512-kbits/s are available. Tables 14, 15, and 16 illustrate the divisors needed to obtain standard rates using these three frequencies.

Table 14. Baud Rates Using a 1.8432-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.690
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.860

Table 15. Baud Rates Using a 3.072-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.230
9600	20	–
19200	10	–
38400	5	–

PRINCIPLES OF OPERATION

programmable baud generator (continued)

Table 16. Baud Rates Using a 8.192-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	1000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

programming

The serial channel of the ACE is programmed by the control registers: LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

receiver

Serial asynchronous data is input into the SIN terminal. The ACE continually searches for a high-to-low transition
from the idle state. When the transition is detected, a counter is cleared, and counts the 16× clock to 7 1/2, which is the center of the start bit. The start bit is valid when the SIN is still low. Verifying the start bits prevents the receiver from assembling a false data character due to a low-going noise spike on the SIN input.

The LCR determines the number of data bits in a character [LCR0, LCR1]. When parity is used LCR3 and the polarity of parity LCR4 are needed. Status for the receiver is provided in the LSR. When a full character is received, including parity and stop bits, the data received indication in LSR0 is set. The CPU reads the RBR, which clears LSR0. If the character is not read prior to a new character transfer from the RSR to the RBR, the OE status indication is set in LSR1. When there is a PE, the PE bit is set in LSR2. If a stop bit is not detected, a FE indication is set in LSR3.

When the data into SIN is a symmetrical square wave, the center of the data cells occurs within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16× clock cycle prior to being detected.

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scratchpad register

The scratch register is an 8-bit read/write register that has no affect on either channel in the ACE. It is intended to be used by the programmer to temporarily hold data.

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