TEXAS INSTRUMENTS

TL16C754B Errata August 2006

1. **Problem:** The TL16C754B UART correctly generates a character timeout interrupt (if IER0 set) when the serial input (RX) has gone quiescent (continuously high) for more than four character times. The problem is that if a new character is received after the timeout, the interrupt will be cleared. The interrupt will be generated again if another timeout occurs. This is an error because reading the RHR (RBR) should be the only clearing mechanism for this interrupt.
   Work Around: If software is responding to an asserted INT and a read of the IIR reports no active interrupt, then assume it is caused by a new byte being received. Check the LSR; if LSR0 (DR) is set, read the RHR and repeat.
   Severity: Moderate

2. **Problem:** The TL16C754B UART can present a stuck interrupt caused by the LSR being stuck at 62 (overrun indication). The conditions are non-FIFO mode (FCR0=0), LSR error interrupts enabled (IER2=1), and the RX input held low for an extended period. Note that the marking state for RX is high, so this last condition is usually only seen at startup when the RX source has not yet stabilized. Since the device powers up in non-FIFO mode, the problem can occur before FIFO mode has had a chance to be enabled. Figure 1 illustrates when the problem can occur. Each low time on the RX signal is relatively long, and since the divisor registers power up unknown, it is impossible to say with certainty if the low times are sufficient to generate a break character. However, assume that they are. The problem occurs only if more than one break character is detected, which causes an overrun error since the device is in non-FIFO mode. Normally reading the LSR clears the overrun interrupt, but if the RX signal is still low when the LSR is read, the overrun condition will persist erroneously. Once the problem has occurred, changing from non-FIFO to FIFO mode will not clear it out until the RX source is stable.

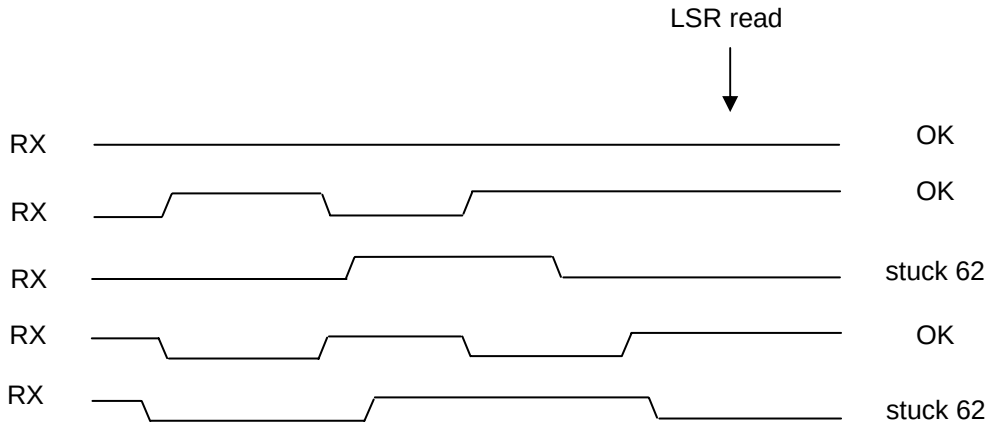

Figure 1.

   Work Around: The problem can be avoided by enabling only IER0 (IER2 left at default) and then waiting until a valid (non-error) character is received. The break characters will still be detected and read as 00 in the RHR with the correct status in the LSR. RX source has stabilized when a character with no errors present is detected. Then IER2 can be set, and normal FIFO operation can continue.
   Severity: Minor

3. **Problem:** The TL16C754B can clear the just set THRE interrupt condition if the IIR read is coincident to the THRE setting. Since IIR reads are generally asynchronous with respect to the THRE setting, the possibility exists for this problem to occur, although it is unlikely. Reading the IIR is one of the normal clearing mechanisms for the THRE interrupt. Most software will read the IIR only as a response to assertion of the INT pin, which means that this overlap cannot occur. This problem is seen only on systems that logically OR the four individual INTA,B,C, and D signals into one signal to the uP. In detecting which channel had the interrupt, it is necessary to read all four channel's IIRs, and this is when the overlap can occur.

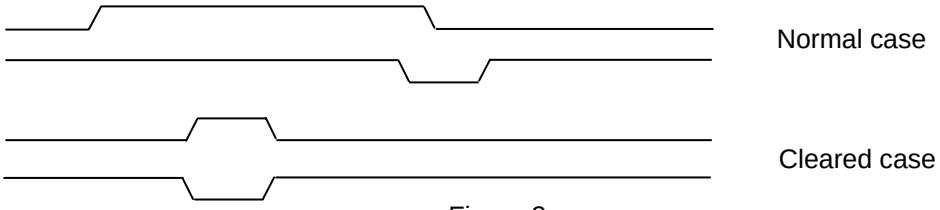

Figure 2.

Work Around: Read only the IIR that corresponds to the channel that generated the interrupt.
Severity: Minor

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