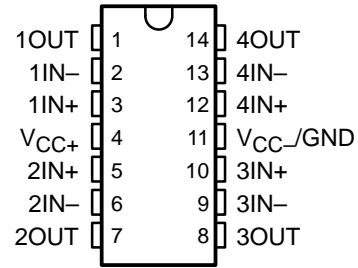


HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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- Low Offset . . . 3 mV (Max) for A-Grade
- Wide Gain-Bandwidth Product . . . 4 MHz
- High Slew Rate . . . 13 V/ $\mu$ s
- Fast Settling Time . . . 1.1  $\mu$ s to 0.1%
- Wide-Range Single-Supply Operation . . . 4 V to 36 V
- Wide Input Common-Mode Range Includes Ground ( $V_{CC-}$ )
- Low Total Harmonic Distortion . . . 0.02%
- Large-Capacitance Drive Capability . . . 10,000 pF
- Output Short-Circuit Protection
- Alternative to MC33074/A and MC34074/A

D, N, OR PW PACKAGE (TOP VIEW)



description/ordering information

ORDERING INFORMATION

TA	V <sub>IO</sub> max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	A-grade: 3 mV	PDIP (N)	Tube of 25	TL3474ACN	TL3474ACN
		SOIC (D)	Tube of 50	TL3474ACD	TL3474A
			Reel of 2500	TL3474ACDR	
	TSSOP (PW)	Tube of 90	TL3474ACPW	T3474A	
		Reel of 2000	TL3474ACPWR		
	0°C to 70°C	Standard grade: 10 mV	PDIP (N)	Tube of 25	TL3474CN
SOIC (D)			Tube of 50	TL3474CD	TL3474C
			Reel of 2500	TL3474CDR	
TSSOP (PW)		Tube of 90	TL3474CPW	TL3474	
		Reel of 2000	TL3474CPWR		
-40°C to 105°C		A-grade: 3 mV	PDIP (N)	Tube of 25	TL3474AIN
	SOIC (D)		Tube of 50	TL3474AID	TL3474AI
			Reel of 2500	TL3474AIDR	
	TSSOP (PW)	Tube of 90	TL3474AIPW	Z3474A	
		Reel of 2000	TL3474AIPWR		
	-40°C to 105°C	Standard grade: 10 mV	PDIP (N)	Tube of 25	TL3474IN
SOIC (D)			Tube of 50	TL3474ID	TL3474I
			Reel of 2500	TL3474IDR	
TSSOP (PW)			Tube of 90	TL3474IPW	Z3474
	Reel of 2000	TL3474IPWR			

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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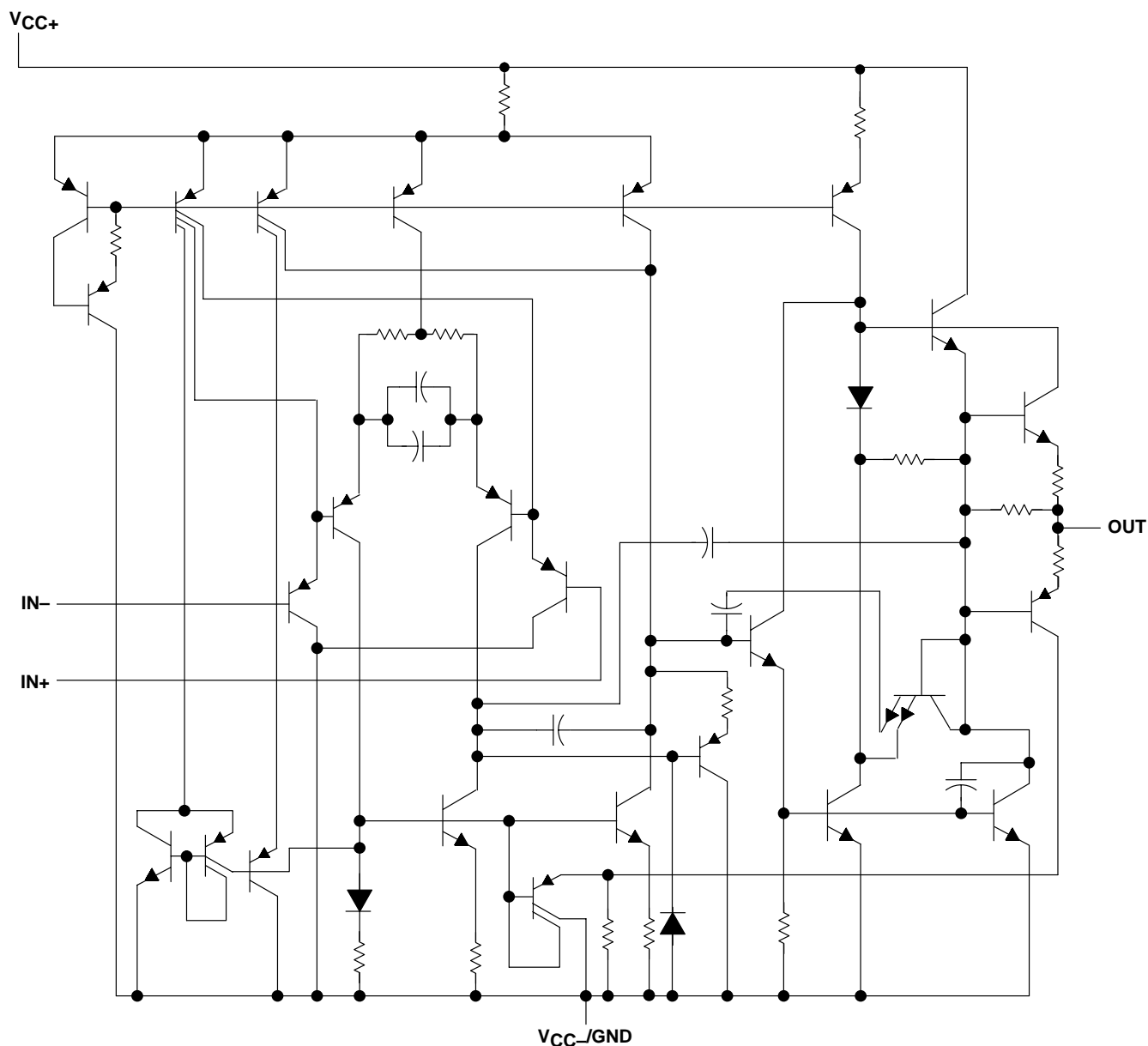
# TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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## description/ordering information (continued)

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3474, TL3474A operational amplifiers. These devices offer 4 MHz of gain-bandwidth product, 13-V/ $\mu$ s slew rate, and fast settling time without the use of JFET device technology. Although the TL3474 and TL3474A can be operated from split supplies, they are particularly suited for single-supply operation because the common-mode input voltage range includes ground potential ( $V_{CC-}$ ). With a Darlington transistor input stage, these devices exhibit high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. These low-cost amplifiers are an alternative to the MC34074/A and MC33074/A operational amplifiers.

## schematic (each amplifier)



# TL3474, TL3474A

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: $V_{CC+}$ (see Note 1) .....	18 V
$V_{CC-}$ .....	-18 V
Differential input voltage, $V_{ID}$ (see Note 2) .....	$\pm 36$ V
Input voltage, $V_I$ (any input) .....	$V_{CC\pm}$
Input current, $I_I$ (each input) .....	$\pm 1$ mA
Output current, $I_O$ .....	$\pm 80$ mA
Total current into $V_{CC+}$ .....	80 mA
Total current out of $V_{CC-}$ .....	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .....	Unlimited
Package thermal impedance, $\theta_{JA}$ (see Notes 4 and 5): D package .....	86°C/W
N package .....	80°C/W
PW package .....	113°C/W
Operating virtual junction temperature, $T_J$ .....	150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds .....	260°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}/GND$ .
  2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than  $V_{CC-} - 0.3$  V.
  3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
  4. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  5. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions

		MIN	MAX	UNIT	
$V_{CC\pm}$	Supply voltage	4	36	V	
$V_{IC}$	Common-mode input voltage	$V_{CC} = 5$ V	0	2.8	V
		$V_{CC\pm} = \pm 15$ V	-15	12.8	
$T_A$	Operating free-air temperature	TL3474C, TL3474AC	0	70	°C
		TL3474I, TL3474AI	-40	105	



# TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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## electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL3474			TL3474A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>IC</sub> = 0, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	V <sub>CC</sub> = 5 V	25°C	1.5	10	1.5	3	mV	
		V <sub>CC</sub> = ±15 V	25°C	1.0	10	1.0	3		
			Full range‡			12			5
αV <sub>IO</sub> Temperature coefficient of input offset voltage	V <sub>IC</sub> = 0, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	V <sub>CC</sub> = ±15 V	Full range‡	10		10		μV/°C	
I <sub>IO</sub> Input offset current		V <sub>CC</sub> = ±15 V	25°C	6	75	6	75	nA	
			Full range‡		300		300		
I <sub>IB</sub> Input bias current	V <sub>CC</sub> = ±15 V	25°C	100	500	100	500	nA		
		Full range‡		700		700			
V <sub>ICR</sub> Common-mode input voltage range	R <sub>S</sub> = 50 Ω	25°C	-15 to 12.8		-15 to 12.8		V		
		Full range‡	-15 to 12.8		-15 to 12.8				
V <sub>OH</sub> High-level output voltage	V <sub>CC+</sub> = 5 V, V <sub>CC-</sub> = 0, R <sub>L</sub> = 2 kΩ	25°C	3.7	4	3.7	4	V		
	R <sub>L</sub> = 10 kΩ	25°C	13.6	14	13.6	14			
	R <sub>L</sub> = 2 kΩ	Full range‡	13.4		13.4				
V <sub>OL</sub> Low-level output voltage	V <sub>CC+</sub> = 5 V, V <sub>CC-</sub> = 0, R <sub>L</sub> = 2 kΩ	25°C	0.1	0.3	0.1	0.3	V		
	R <sub>L</sub> = 10 kΩ	25°C	-14.7	-14.3	-14.7	-14.3			
	R <sub>L</sub> = 2 kΩ	Full range‡		-13.5		-13.5			
A <sub>VD</sub> Large-signal differential voltage amplification	V <sub>O</sub> = ±10 V, R <sub>L</sub> = 2 kΩ	25°C	25	100	25	100	V/mV		
		Full range‡	20		20				
I <sub>OS</sub> Short-circuit output current	Source: V <sub>ID</sub> = 1 V, V <sub>O</sub> = 0	25°C	-10	-34	-10	-34	mA		
	Sink: V <sub>ID</sub> = -1 V, V <sub>O</sub> = 0		20	27	20	27			
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICR</sub> (min), R <sub>S</sub> = 50 Ω	25°C	65	97	80	97	dB		
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>CC±</sub> = ±13.5 V to ±16.5 V, R <sub>S</sub> = 100 Ω	25°C	70	97	70	97	dB		
I <sub>CC</sub> Supply current (per channel)	V <sub>O</sub> = 0, No load	25°C	3.5	4.5	3.5	4.5	mA		
		Full range‡	4.5	5.5	4.5	5.5			
	V <sub>CC+</sub> = 5 V, V <sub>O</sub> = 2.5 V, V <sub>CC-</sub> = 0, No load	25°C	3.5	4.5	3.5	4.5			

† All typical values are at T<sub>A</sub> = 25°C.

‡ Full range is 0°C to 70°C for the TL3474C, TL3474AC devices and -40°C to 105°C for the TL3474I, TL3474AI devices.



# TL3474, TL3474A

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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**operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS		TL3474			TL3474A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_I = -10\text{ V to } 10\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 300\text{ pF}$	$A_V = 1$	8	10		8	10	$\text{V}/\mu\text{s}$	
SR-	Negative slew rate		$A_V = -1$				13	13		
$t_s$	Settling time	$A_{VD} = -1$ , 10-V step	To 0.1%		1.1		1.1		$\mu\text{s}$	
			To 0.01%		2.2		2.2			
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$ ,	$R_S = 100\ \Omega$		49		49		$\text{nV}/\sqrt{\text{Hz}}$	
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$			0.22		0.22		$\text{pA}/\sqrt{\text{Hz}}$	
THD	Total harmonic distortion	$V_{O(PP)} = 2\text{ V to } 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 10$ , $f = 10\text{ kHz}$			0.02		0.02		%	
GBW	Gain-bandwidth product	$f = 100\text{ kHz}$		3	4		3	4	MHz	
BW	Power bandwidth	$V_{O(PP)} = 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 1$ , THD = 5.0%			160		160		kHz	
$\phi_m$	Phase margin	$R_L = 2\text{ k}\Omega$ ,	$C_L = 0$		70		70		deg	
		$R_L = 2\text{ k}\Omega$ ,	$C_L = 300\text{ pF}$		50		50			
	Gain margin	$R_L = 2\text{ k}\Omega$ ,	$C_L = 0$		12		12		dB	
		$R_L = 2\text{ k}\Omega$ ,	$C_L = 300\text{ pF}$		4		4			
$r_i$	Differential input resistance	$V_{IC} = 0$			150		150		$\text{M}\Omega$	
$C_i$	Input capacitance	$V_{IC} = 0$			2.5		2.5		pF	
	Channel separation	$f = 10\text{ kHz}$			101		101		dB	
$z_o$	Open-loop output impedance	$f = 1\text{ MHz}$ ,	$A_V = 1$		20		20		$\Omega$	

# TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

**OUTPUT IMPEDANCE  
vs  
FREQUENCY**

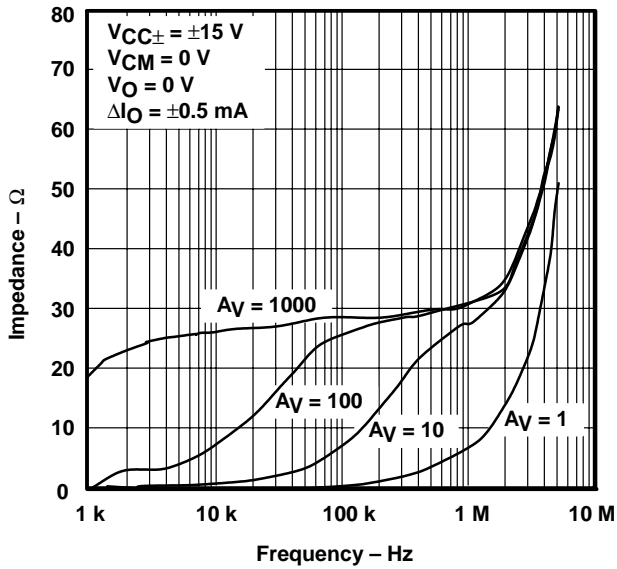


Figure 1

**TOTAL HARMONIC DISTORTION  
vs  
FREQUENCY**

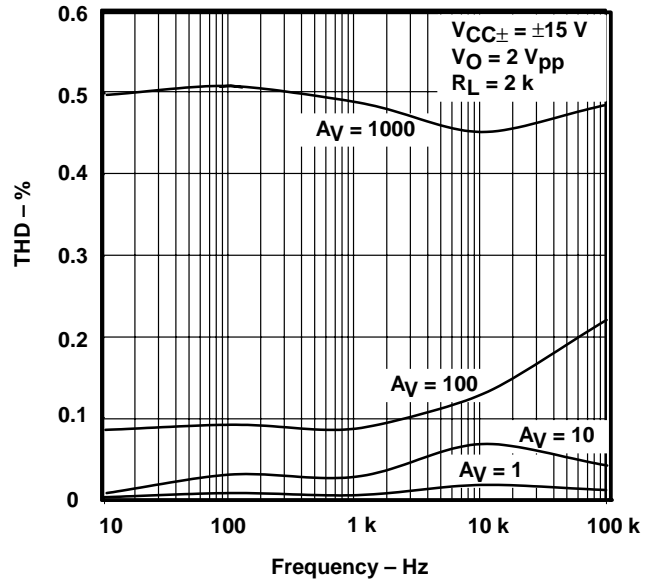


Figure 2

**GAIN AND PHASE  
vs  
FREQUENCY**

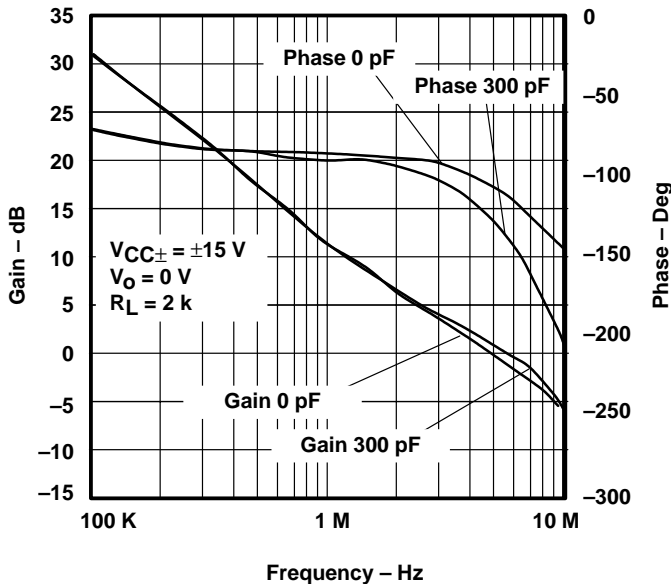


Figure 3

**NORMALIZED INPUT BIAS CURRENT  
vs  
TEMPERATURE**

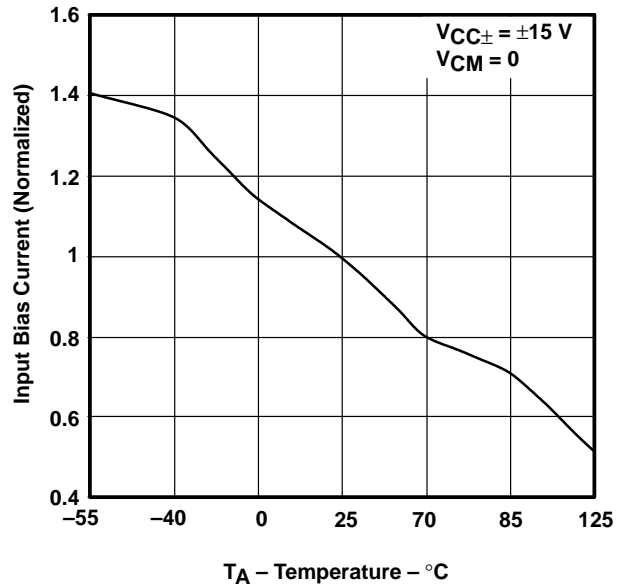


Figure 4



TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

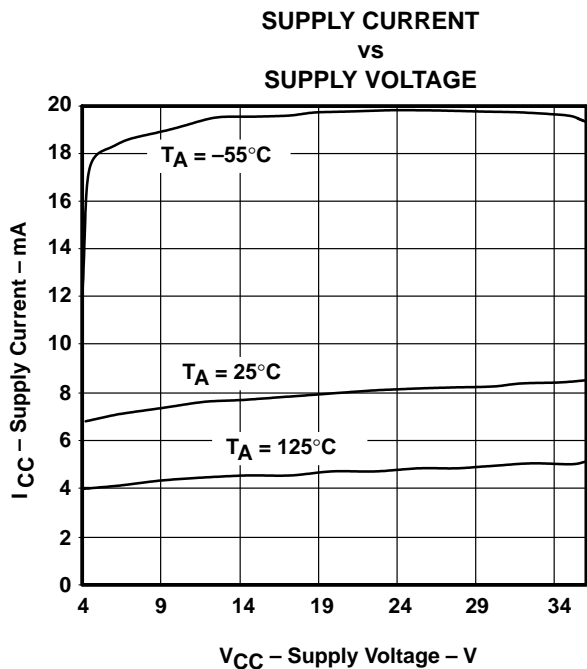


Figure 5

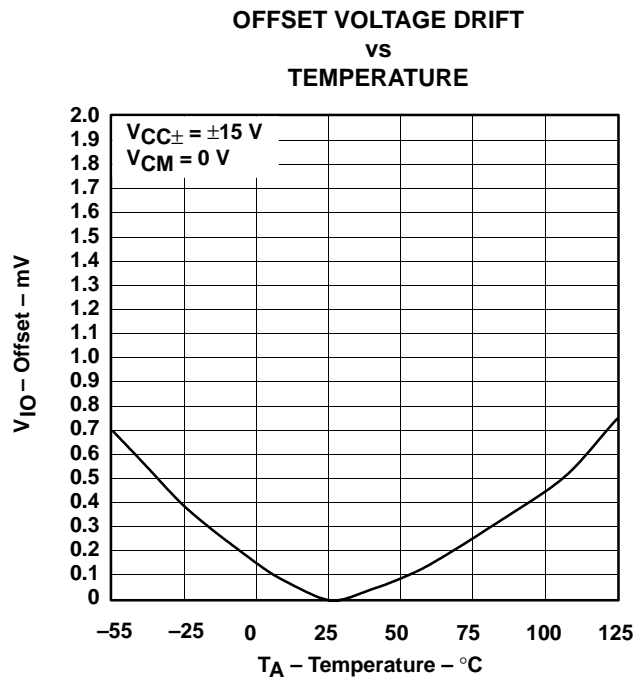


Figure 6

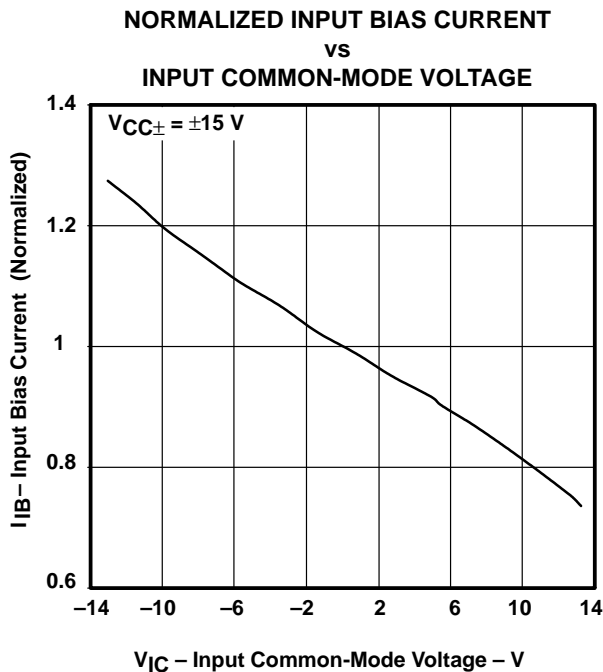


Figure 7

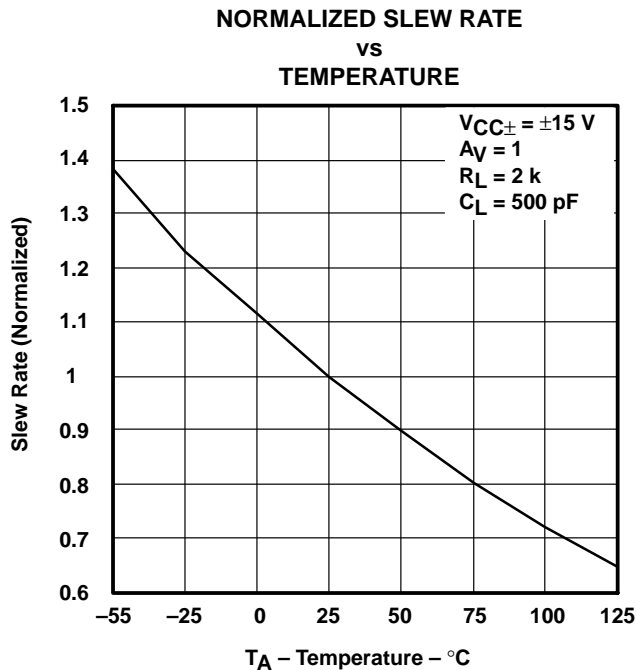


Figure 8

# TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

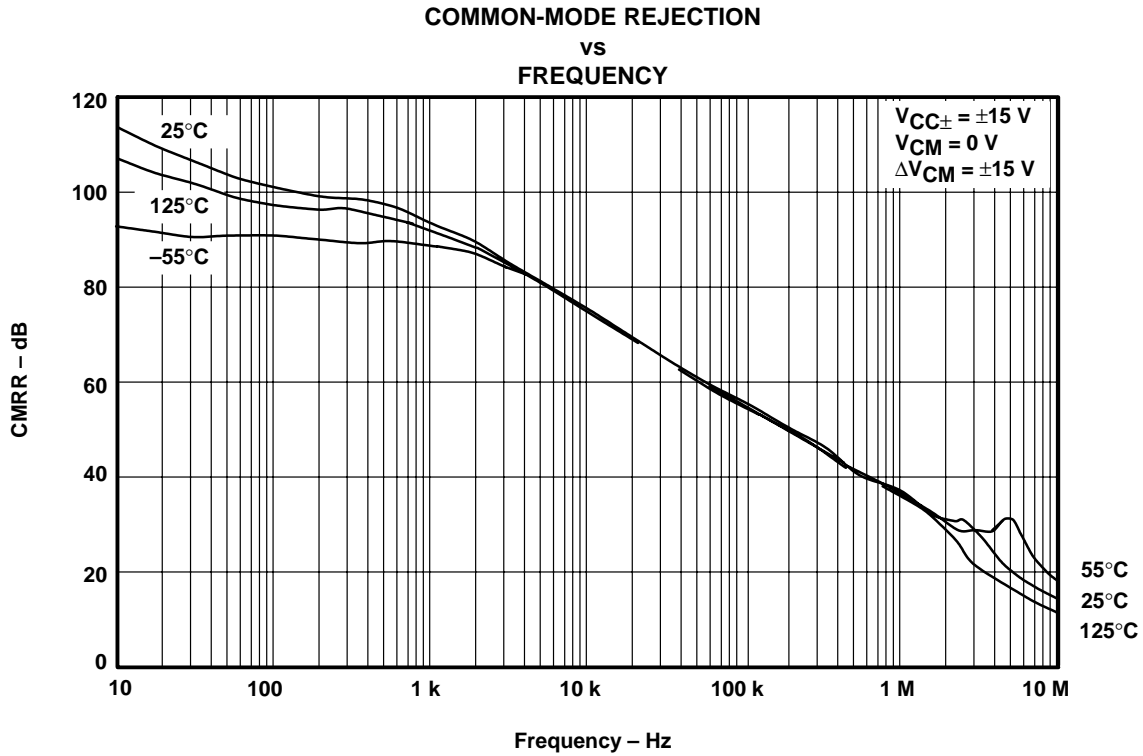


Figure 9



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL3474ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL3474ACNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL3474ACPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474ACPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474ACPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474ACPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474AIDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474AIDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474AIN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL3474AINE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL3474AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474AIPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474AIPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL3474CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL3474CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL3474CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474CPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL3474INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL3474IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474IPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3474IPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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