

TOSHIBA**TL8857F**

TENTATIVE TOSHIBA CCD ANALOG PROCESSOR INTEGRATED CIRCUIT SILICON MONOLITHIC

TL8857F

NTSC SKEW CORRECTION IC FOR VCR

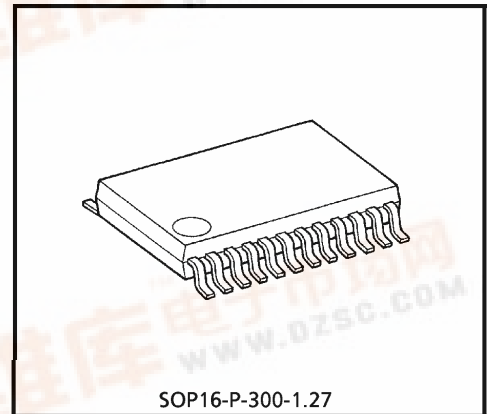
The TL8857F is the skew correction IC for the search playback signal of NTSC SP mode by 4 head PAL cylinder. This skew is made by the difference of 1H length on tape between NTSC (525 lines) and PAL (625 lines)

PAL : 625 lines = 2H

NTSC : 525 lines = $(2 / 625) \times 525 = 1.68H$

Difference (Skew) = 2H - 1.68H = 0.32H

TL8857F corrects the skew by changing the delay time of CCD delay lines.



Weight : 0.2g (Typ.)

FEATURES

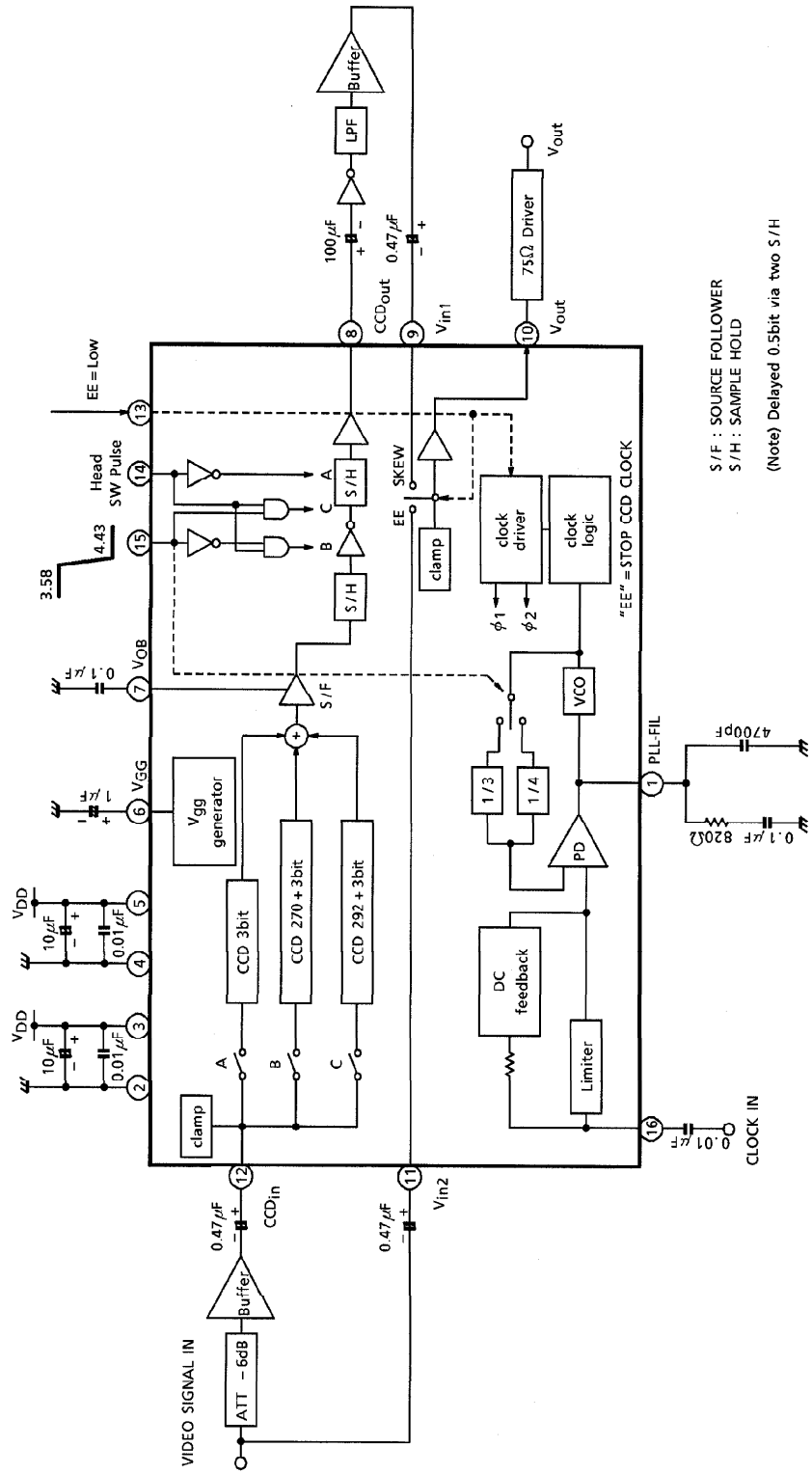
- CCD DELAY LINES
NTSC 0.32H/0H DELAY LINES (Apply to both 3.58NTSC and 4.43NTSC)
- SYNC TIP CLAMP CIRCUIT
- CCD DRIVE CIRCUIT, SAMPLE AND HOLD CIRCUIT
- 2 input SW (For the through mode)
- 2 input SW is controlled by Pin 13
Low = Through (EE) mode
High = Skew (correction) mode
- When Pin 13 is Low the CCD clock driver is off and the CCD output (Pin 8) is fixed to DC

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- The CCD delay time is 2 mode. 0H and 0.32H, controlled by Pin 14.
Low = 0H
High = 0.32H
- PLL frequency multiplier is built in. 3.58NTSC and 4.43NTSC are selected by Pin 15.
Low = 4.43NTSC
High = 3.58NTSC
- Input signal is sampling by 4 times (3.58NTSC) or 3 times (4.43NTSC) of subcarrier frequency, generated by internal PLL multiplier.
- 5V single power supply.
- As all supporting circuit for CCD such as CCD driver, bias generators and output amplifiers are built in, minimum external parts are needed.
- The output signal at pin 8 is inverted.

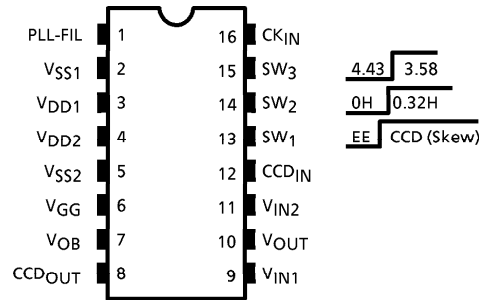
BLOCK DIAGRAM



S/F : SOURCE FOLLOWER
S/H : SAMPLE HOLD

(Note) Delayed 0.5bit via two S/H

PIN LIST



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	6	V
Input Voltage	V _{IN}	- 0.3~V _{DD} + 0.3	V
Power Dissipation	P _D (Note 1)	300	mW
Operating Temperature	T _{opr} (Note 2)	0~60	°C
Storage Temperature	T _{stg}	- 55~150	°C

(Note 1) Ta = 60°C

(Note 2) Frost isn't to stick to the condition.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTIC (Ta = 25°C, V_{DD} = 5.0V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V _{DD}	—	SKEW, 3.58NTSC mode V _{in} = No signal CLOCK = 3.579545MHz 300mV _{p-p} Pin 13, 14, 15 = "Hi" = 5V DC Input	4.75	5.0	5.25	V
Supply Current	I _{DD}	—		8.0	13.0	18.0	mA
Output DC Level	CCD _{out}	—		3.0	3.6	4.2	V
	V _{OUT}	—		1.5	2.0	2.5	
Pin DC Level	CCD _{in}	—		2.5	2.9	3.3	
	V _{IN1}	—		0.4	0.8	1.2	
	V _{IN2}	—		0.4	0.8	1.2	
	V _{OB}	—		0.9	1.5	2.1	
	PLL-FIL	—		0.5	1.5	2.5	
	CLOCK IN	—		1.3	2.3	3.3	
	V _{GG}	—	8.0	10.0	12.0		
Switch Input Select Level Pin Voltage	SW ₁ IL	—	—	—	1.5		
	SW ₁ IH	—	3.5	—	—		
	SW ₂ IL	—	—	—	1.5		
	SW ₂ IH	—	3.5	—	—		
	SW ₃ IL	—	—	—	1.5		
	SW ₃ IH	—	3.5	—	—		

ELECTRICAL CHARACTERISTICS (3.58NTSC mode, CCD part)

AC CHARACTERISTIC

(Ta = 25°C, VDD = 5.0V, clock = 3.579545MHz, 0.3Vp-p, S2 = 2, S3 = 2, S4 = 1, S6 = 1, S8 = 1)

CHARACTERISTIC	SYM-BOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Input Level	VIN	1	—	—	1.0	1.2	Vp-p		
Voltage Gain	Gv1	1	S1 = 1, S7 = 2, S9 = 1, S10 = 1, S11 = 2 VIN = 15.625kHz, 0.6Vp-p (Fig.2-b)	S5 = 2 (0H)	0	2.0	4.0	dB	
	Gv2			S5 = 1 (0.32H)	0	2.0	4.0		
Frequency Characteristic	Gf1	1	S1 = 1, S7 = 2, S9 = 1, S10 = 1, S11 = 2 VIN = 15.625kHz / 4.5MHz, 0.6Vp-p (Fig.2-b)	S5 = 2 (0H)	-3	-2	—	dB	
	Gf2			S5 = 1 (0.32H)	-3	-2	—		
Differential Gain	DG1	1	S1 = 1, S7 = 1, S9 = 1, S10 = 1, S11 = 3 VIN = 5 step signal, 1.0Vp-p Y = 140IRE = 1.0Vp-p, C = 40IRE (Fig.3)	S5 = 2 (0H)	—	5	7	%	
	DG2			S5 = 1 (0.32H)	—	5	7		
Differential Phase	DP1	1	DG = (COmax - COmin) / COmin (Fig.5)	S5 = 2 (0H)	—	5	7	deg	
	DP2			S5 = 1 (0.32H)	—	5	7		
Linearity	Ls1	1	S1 = 1, S7 = 1, S9 = 1, S10 = 2, S11 = 1 VIN = 5 step signal, 1.0Vp-p (Fig.2-a, Fig.4)	S / Y2	S5 = 2 (0H)	37	40	43	%
					S5 = 1 (0.32H)	37	40	43	
	Ly1	1		Y1 / Y2	S5 = 2 (0H)	56	60	64	
					S5 = 1 (0.32H)	56	60	64	
Output Impedance	Z01	1	S1 = 1, S7 = 2, S10 = 1, S11 = 1 VIN = 15.625kHz, 0.6Vp-p (Fig.2-b) Z0 = (V1 - V2) / V2 × 1000 V1 : S9 = 1, V2 : S9 = 2	S5 = 2 (0H)	100	250	400	Ω	
				S5 = 1 (0.32H)	100	250	400		
Clock Input Level	Vck	1	—	0.2	0.3	0.7	Vp-p		
Clock Leak (4fsc)	Lck 14.3	1	S1 = 2, S7 = 1, S9 = 1, S10 = 1, S11 = 2 VIN = No signal	S5 = 2 (0H)	—	20	40	mVrms	
				S5 = 1 (0.32H)	—	20	40		
Clock Leak (fsc)	Lsc 3.58	1	S1 = 2, S7 = 1, S9 = 1, S10 = 1, S11 = 2 VIN = No signal	S5 = 2 (0H)	—	1	2	mVrms	
				S5 = 1 (0.32H)	—	1	2		

ELECTRICAL CHARACTERISTIC (4.43NTSC mode, CCD part)

AC CHARACTERISTIC

(Ta = 25°C, VDD = 5.0V, clock = 4.43361875MHz, 0.3Vp-p, S2 = 2, S3 = 2, S4 = 2, S6 = 1, S8 = 1)

CHARACTERISTIC	SYM-BOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Input Level	V _{IN}	1	—	—	1.0	1.2	V _{p-p}		
Voltage Gain	G _{V3}	1	S ₁ = 2, S ₇ = 2, S ₉ = 1, S ₁₀ = 1, S ₁₁ = 2 V _{IN} = 15.625kHz, 0.6V _{p-p} (Fig.2-b)	S ₅ = 2 (0H)	0	2.0	4.0	dB	
	G _{V4}			S ₅ = 1 (0.32H)	0	2.0	4.0		
Frequency Characteristic	G _{f3}	1	S ₁ = 2, S ₇ = 2, S ₉ = 1, S ₁₀ = 1, S ₁₁ = 2 V _{IN} = 15.625kHz / 4.5MHz, 0.6V _{p-p} (Fig.2-b)	S ₅ = 2 (0H)	-3	-2	—	dB	
	G _{f4}			S ₅ = 1 (0.32H)	-3	-2	—		
Differential Gain	DG3	1	S ₁ = 2, S ₇ = 1, S ₉ = 1, S ₁₀ = 1, S ₁₁ = 3 V _{IN} = 5 step signal, 1.0V _{p-p} Y = 140IRE = 1.0V _{p-p} , C = 40IRE (Fig.3)	S ₅ = 2 (0H)	—	5	7	%	
	DG4			S ₅ = 1 (0.32H)	—	5	7		
Differential Phase	DP3	1	DG = (CO _{max} - CO _{min}) / CO _{min} (Fig.5)	S ₅ = 2 (0H)	—	5	7	deg	
	DP4			S ₅ = 1 (0.32H)	—	5	7		
Linearity	L _{s2}	1	S ₁ = 2, S ₇ = 1, S ₉ = 1, S ₁₀ = 2, S ₁₁ = 1 V _{IN} = 5 step signal, 1.0V _{p-p} (Fig.2-a, Fig.4)	S / Y ₂	S ₅ = 2 (0H)	37	40	43	%
					S ₅ = 1 (0.32H)	37	40	43	
	L _{y2}	1		Y ₁ / Y ₂	S ₅ = 2 (0H)	56	60	64	
					S ₅ = 1 (0.32H)	56	60	64	
Output Impedance	Z _{O2}	1	S ₁ = 2, S ₇ = 2, S ₁₀ = 1, S ₁₁ = 1 V _{IN} = 15.625kHz, 0.6V _{p-p} (Fig.2-b) Z _O = (V ₁ - V ₂) / V ₂ × 1000 V ₁ : S ₉ = 1, V ₂ : S ₉ = 2	S ₅ = 2 (0H)	100	250	400	Ω	
				S ₅ = 1 (0.32H)	100	250	400		
Clock Input Level	V _{ck}	1	—	0.2	0.3	0.7	V _{p-p}		
Clock Leak (3fsc)	L _{ck} 13.3	1	S ₁ = 2, S ₇ = 2, S ₉ = 1, S ₁₀ = 1, S ₁₁ = 2 V _{IN} = No signal	S ₅ = 2 (0H)	—	20	40	mV _{rms}	
				S ₅ = 1 (0.32H)	—	20	40		
Clock Leak (fsc)	L _{sc} 4.43	1	S ₁ = 2, S ₇ = 2, S ₉ = 1, S ₁₀ = 1, S ₁₁ = 2 V _{IN} = No signal	S ₅ = 2 (0H)	—	1	2	mV _{rms}	
				S ₅ = 1 (0.32H)	—	1	2		

ELECTRICAL CHARACTERISTIC Commonness (SW part)

AC CHARACTERISTIC (Ta = 25°C, VDD = 5.0V, clock = 3.579545MHz or 4.43361875MHz, 0.3Vp-p, S1 = 2, S4 = 1 or 2, S5 = 1 or 2, S8 = 2, S10 = 1)

CHARACTERISTIC	SYM-BOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Input Level	VIN	1	—	—	2.0	2.4	Vp-p		
Through Mode Voltage Gain	Gv5	1	S7 = 2, S9 = 1, S11 = 2 VIN = 15.625kHz, 1.2Vp-p (Fig.6-b)	S6 = 2, S2 = 1, S3 = 2 (Pin 11→Pin 10)	-1.5	-0.5	0.5	dB	
	Gv6			S6 = 1, S2 = 2, S3 = 1 (Pin 9→Pin 10)	-1.5	-0.5	0.5		
Through Mode Frequency Characteristic	fth1	1	S7 = 2, S9 = 1, S11 = 2 VIN = 15.625kHz / 4.5MHz, 1.2Vp-p (Fig.6-b)	S6 = 2, S2 = 1, S3 = 2 (Pin 11→Pin 10)	-1.0	0	1.0	dB	
	fth2			S6 = 1, S2 = 2, S3 = 1 (Pin 9→Pin 10)	-1.0	0	1.0		
Differential Gain	DG5	1	S7 = 1, S9 = 1, S11 = 3 VIN = 5 step signal, 2.0Vp-p Y = 140IRE = 1.0Vp-p, C = 40IRE (Fig.7)	S6 = 2, S2 = 1, S3 = 2 (Pin 11→Pin 10)	—	3	5	%	
	DG6			S6 = 1, S2 = 2, S3 = 1 (Pin 9→Pin 10)	—	3	5		
Differential Phase	DP5	1	DG = (COmax - COmin) / COmin (Fig.5)	S6 = 2, S2 = 1, S3 = 2 (Pin 11→Pin 10)	—	3	5	deg	
	DP6			S6 = 1, S2 = 2, S3 = 1 (Pin 9→Pin 10)	—	3	5		
Linearity	Ls3	1	S7 = 1, S9 = 1, S11 = 1 VIN = 5 step signal, 2.0Vp-p (Fig.6-a, Fig.4)	S / Y2	S6 = 2, S2 = 1, S3 = 2 (Pin 11→Pin 10)	37	40	43	%
					S6 = 1, S2 = 2, S3 = 1 (Pin 9→Pin 10)	37	40	43	
	Ly3	1		Y 1 / Y2	S6 = 2, S2 = 1, S3 = 2 (Pin 11→Pin 10)	56	60	64	%
					S6 = 1, S2 = 2, S3 = 1 (Pin 9→Pin 10)	56	60	64	
Output Impedance	Z0	1	S7 = 2, S11 = 1 VIN = 15.625kHz, 1.2Vp-p (Fig.6-b) Z0 = (V1 - V2) / V2 × 1000 V1 : S9 = 1, V2 : S9 = 2	S6 = 2, S2 = 1, S3 = 2 (Pin 11→Pin 10)	100	250	400	Ω	
				S6 = 1, S2 = 2, S3 = 1 (Pin 9→Pin 10)	100	250	400		

TEST CIRCUIT

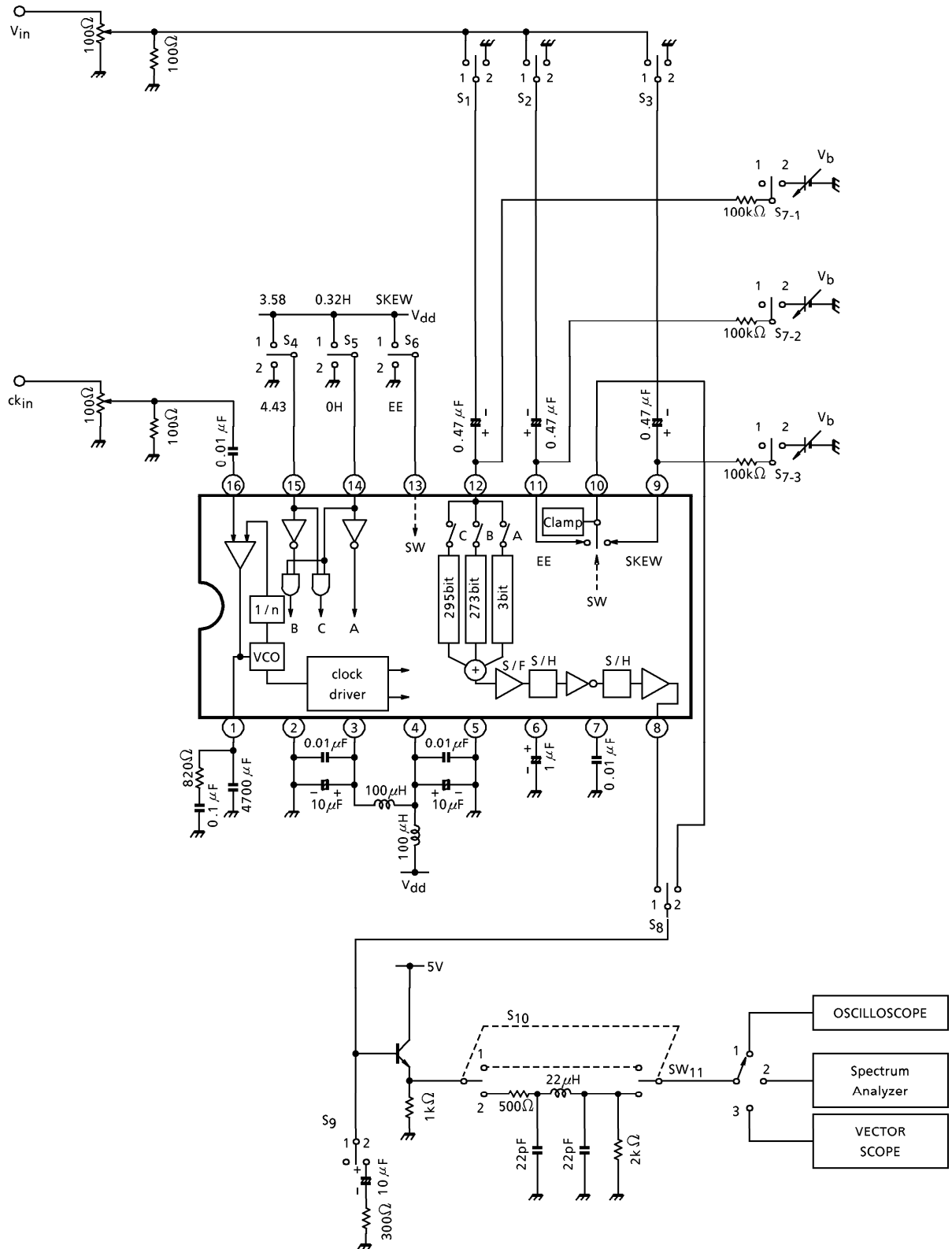


Fig.1

INPUT SIGNAL DC LEVEL

(a) 5 step staircase signal
(Clamp Operation)

(b) Sine wave input
(0.6V_{p-p} input)

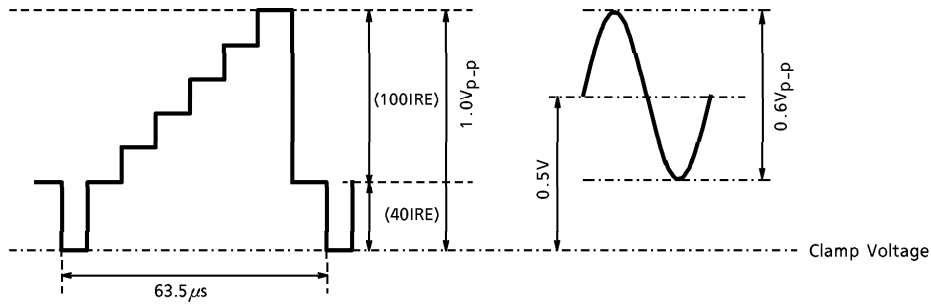


Fig.2

5 STEP STAIRCASE SIGNAL

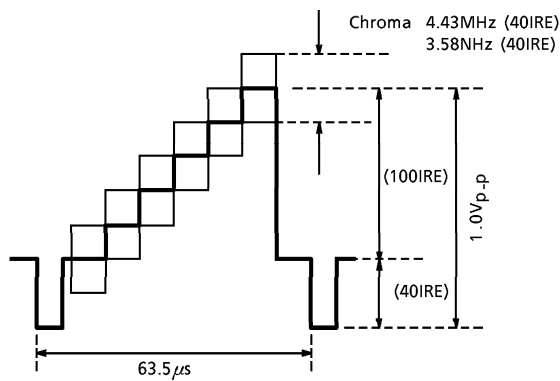


Fig.3

LINEARITY TEST SIGNAL OUTPUT

CHROMA DIFFERENTIAL GAIN

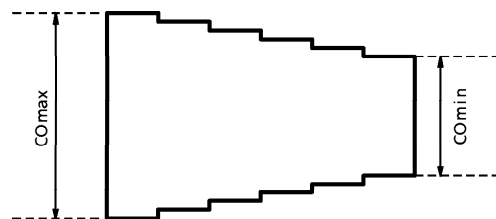
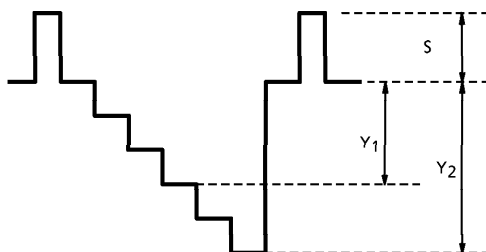


Fig.4

Fig.5

INPUT SIGNAL DC LEVEL

(a) 5 step staircase signal
(Clamp operation)

(b) Sine wave input
(1.2V_{p-p} input)

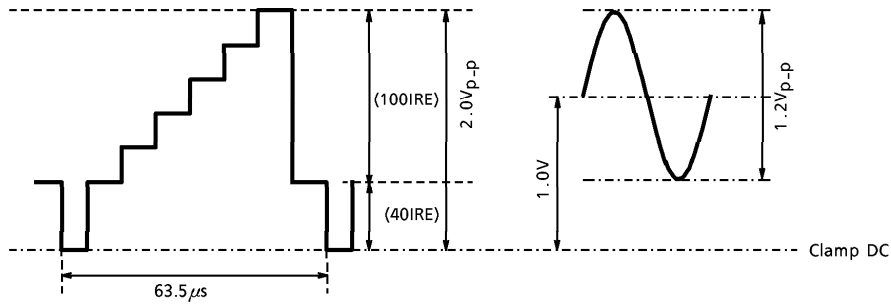


Fig.6

5 STEP STAIRCASE SIGNAL

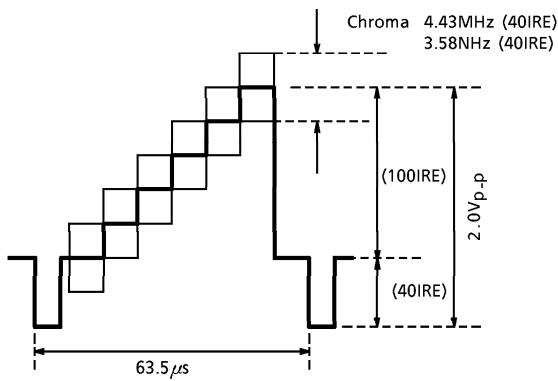
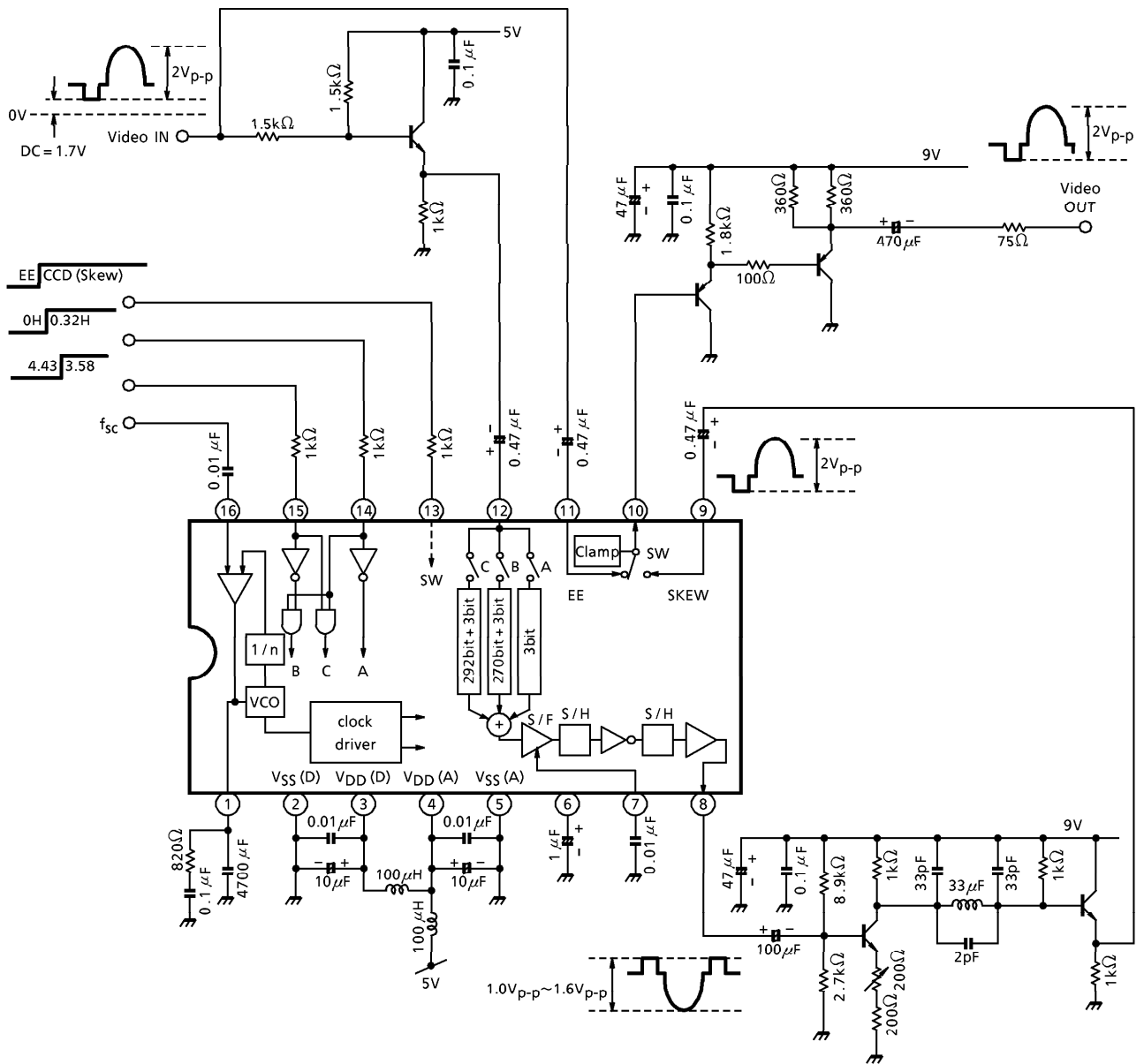


Fig.7

APPLICATION CIRCUIT



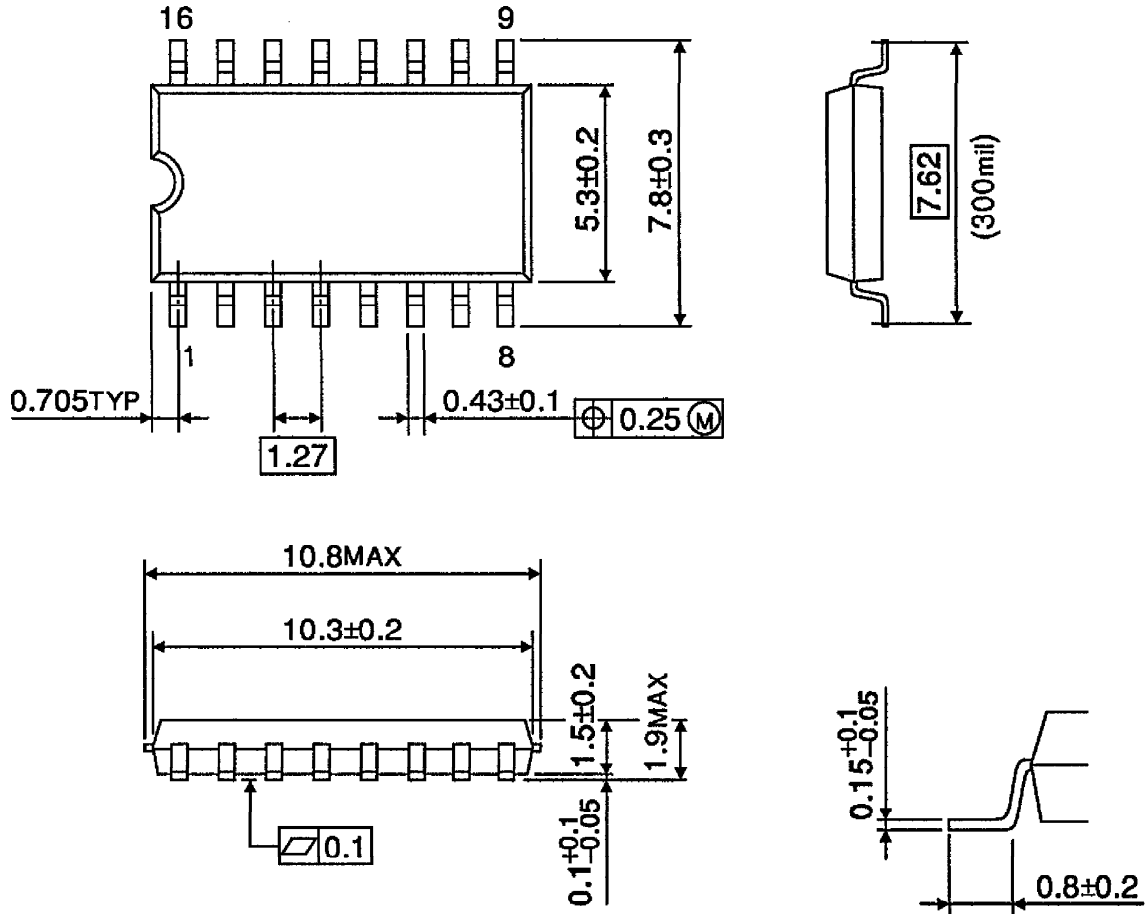
ATTENTION IN TREATMENT

This device is electrostatic sensitive device, so care must be taken in handling and storage to prevent deterioration or damage by means of shorting electrically all pins with use of aluminum foil or conductive mat.

Even in assembled on board, it is necessary to protect against surge or inductive noise from input, output and power supply line.

OUTLINE DRAWING
SOP16-P-300-1.27

Unit : mm



Weight : 0.2g (Typ.)