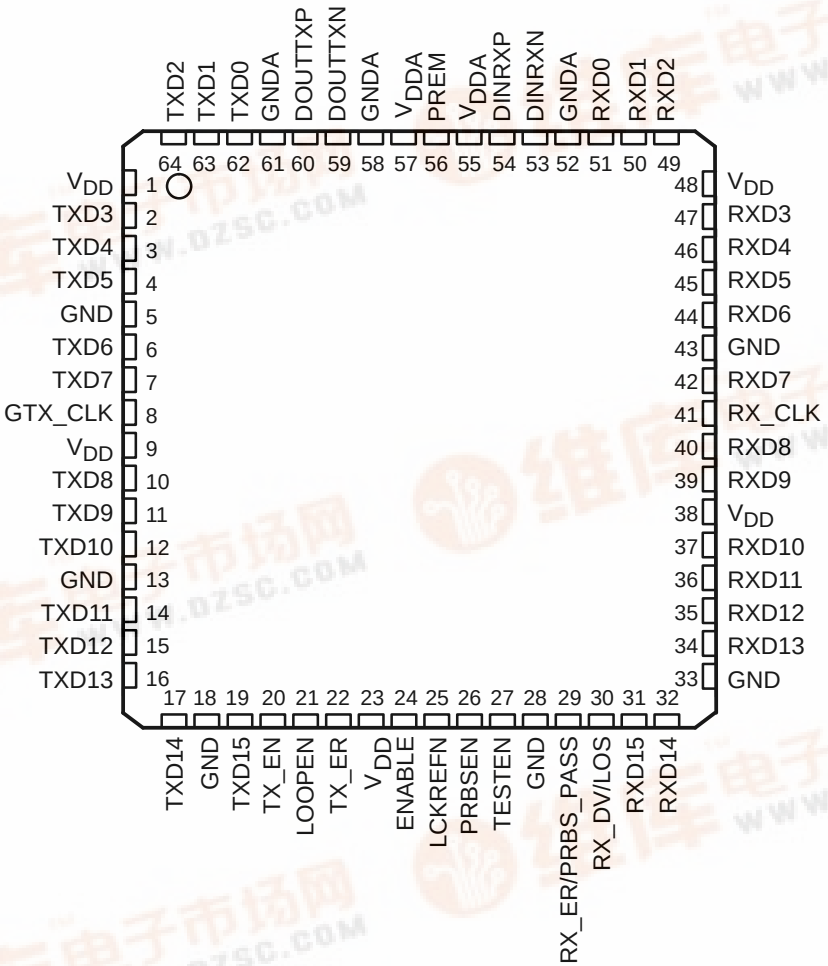
TLK3101
2.5 Gbps to 3.125 Gbps TRANSCEIVER

SCAS649A – AUGUST 2000 – REVISED FEBRUARY 2001

- Hot-Plug Protection
- 2.5 Gigabits to 3.125 Gigabits Per Second (Gbps) Serializer/Deserializer
- High Performance 64-Pin VQFP Thermally Enhanced Package (PowerPAD™)
- 2.5-V Power Supply for Low Power Operation
- PECL Compatible Differential Signalling Serial Interface
- Interfaces to Backplane, Copper Cables, or Optical Converters
- On-Chip 8-Bit/10-Bit Encoding/Decoding, Comma Alignment and Link Synchronization
- On-Chip PLL Provides Clock Synthesis From Low-Speed Reference
- Receiver Differential Input Thresholds 200 mV Min
- Typical Power . . . 450 mW
- Loss of Signal (LOS) Detection
- Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link

RCP PACKAGE
(TOP VIEW)



PowerPAD is a trademark of Texas Instruments.

description

The TLK3101 is a member of the transceiver family of multigigabit transceivers, intended for use in ultrahigh-speed bidirectional point-to-point data transmission systems. The TLK3101 supports an effective serial interface speed of 2.5 Gbps to 3.125 Gbps providing up to 2.5 Gbps of data bandwidth. The TLK3101 is functionally identical to the TLK1501, a 0.6 Gbps to 1.5 Gbps transceiver, and the TLK2501, a 1.6 Gbps to 2.5 Gbps transceiver, providing a wide range of performance solutions with no significant board layout changes.

The primary application of this chip is to provide very high-speed I/O data channels for point-to-point baseband data transmission over controlled impedance media of approximately 50 Ω. The transmission media can be printed-circuit board, copper cables, or fiber-optic cable. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector pins, and transmit/receive pins. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel, which can be a coaxial copper cable, a controlled impedance backplane, or an optical link. It is then reconstructed into its original parallel format. It offers significant power and cost savings over current solutions, as well as scalability for a higher data rate in the future.

The TLK3101 performs the data parallel-to-serial, serial-to-parallel conversion, and clock extraction functions for a physical layer interface device. The serial transceiver interface operates at a maximum speed of 3.125 Gbps. The transmitter latches 16-bit parallel data at a rate based on the supplied reference clock (GTX_CLK). The 16-bit parallel data is internally encoded into 20 bits using an 8-bit/10-bit encoding format. The resulting 20-bit word is then transmitted differentially at 20 times the reference clock (GTX_CLK) rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel data to the extracted reference clock (RX_CLK). It then decodes the 20 bit wide data using 8-bit/10-bit decoding format resulting in 16 bits of parallel data at the receive data pins (RXD0-15). This results in an effective data payload of 2 Gbps to 2.5 Gbps (16 bits data x GTX_CLK frequency).

The TLK3101 is housed in a high-performance, thermally enhanced, 64-pin VQFP PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. It is recommended that the TLK3101 PowerPAD be soldered to the thermal land on the board. All ac performance specifications in this data sheet are measured with the PowerPAD soldered to the test board.

The TLK3101 provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the deserializer allowing the protocol device a functional self-check of the physical interface.

The TLK3101 is designed to be hot plug capable. An on-chip power-on reset circuit holds the RX_CLK low during power up. Also, this circuit holds the parallel side output signal terminals as well as DOUTTXP and DOUTTXN in a high-impedance state.

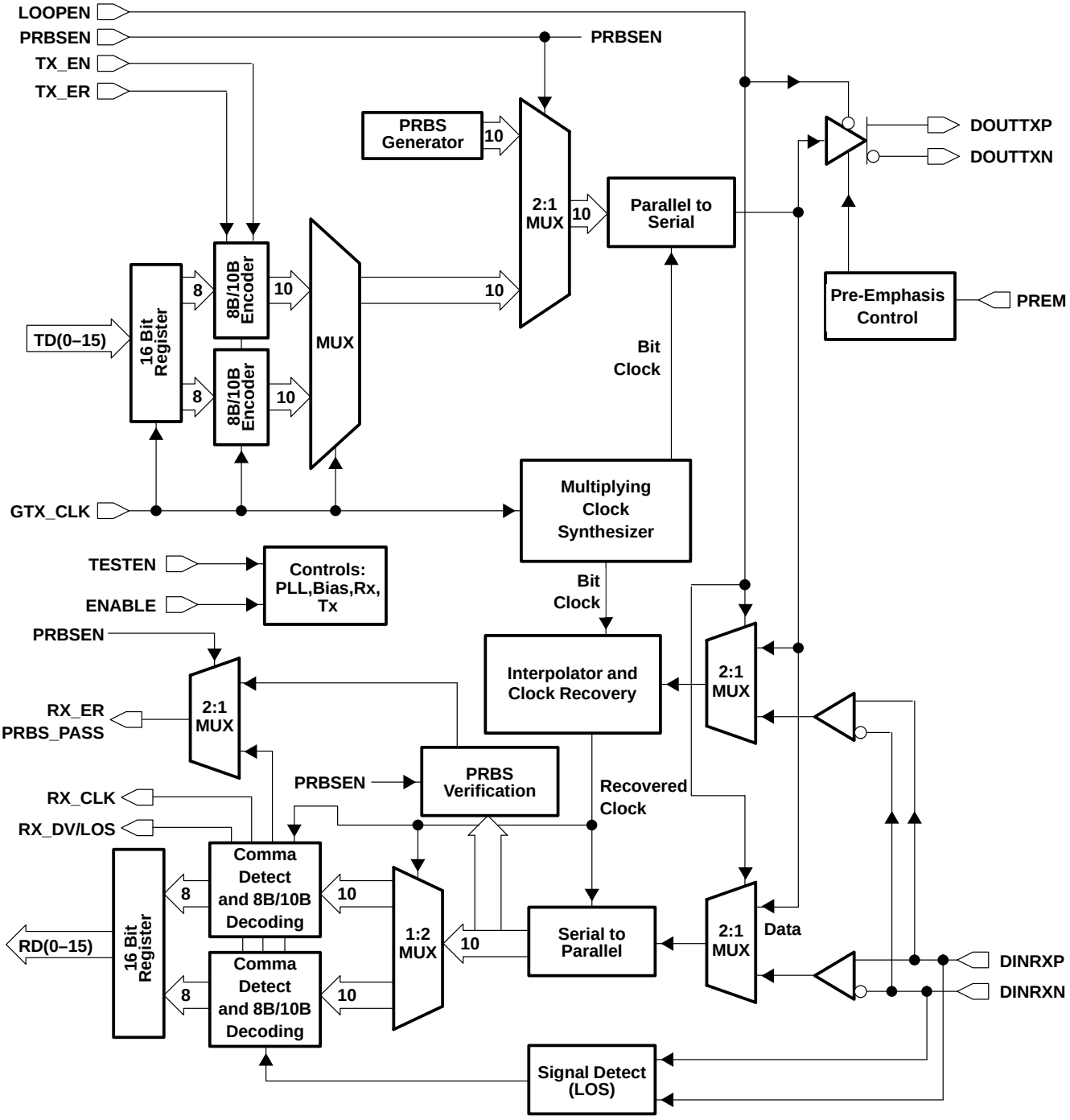
The TLK3101 has a loss of signal detection circuit for conditions where the incoming signal no longer has a sufficient voltage amplitude to keep the clock recovery circuit in lock.

To prevent a data bit error from causing a valid data packet to be interpreted as a comma and thus causing the erroneous word alignment by the comma detection circuit, the comma word alignment circuit is turned off after the link is properly established in the TLK3101.

The TLK3101 allows users to implement redundant ports by connecting receive data bus terminals from two TLK3101 devices together. Asserting LCKREFN to a low state will cause the receive data bus pins, RXD[0:15], RX_CLK, and RX_ER, RX_DV/LOS to go to a high-impedance state. This places the device in a transmit only mode since the receiver is not tracking the data.

The TLK3101 uses a 2.5-V supply. The I/O section is 3 V compatible. With the 2.5-V supply the chipset is very power efficient, consuming less than 450 mW typically. The TLK3101 is characterized for operation from –40°C to 85°C.

functional block diagram



transmit interface

The transmitter portion registers valid incoming 16-bit wide data (TXD[0:15]) on the rising edge of GTX_CLK. The data is then 8-b/10-b encoded, serialized, and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the reference clock (GTX_CLK) by a factor of 10 times creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register which transmits data on both the rising and falling edges of the bit clock providing a serial data rate that is 20 times the reference clock. Data is transmitted LSB (TXD0) first. The transmitter also inserts commas at the beginning of the transmission for byte synchronization.

transmit data bus

The transmit bus interface accepts 16 bit wide single-ended TTL parallel data at the TXD[0:15] pins. Data is valid on the rising edge of GTX_CLK when TX_EN is asserted high and TX_ER is deasserted low. The GTX_CLK is used as the word clock. The data, enable, and clock signals must be properly aligned as shown in Figure 1. Detailed timing information can be found in the TTL input electrical characteristics table.

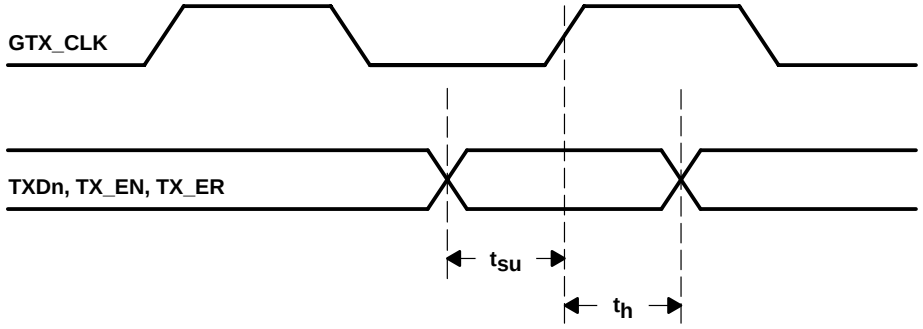


Figure 1. Transmit Timing Waveform

transmission latency

The data transmission latency of the TLK3101 is defined as the delay from the initial 16-bit word load to the serial transmission of bit 0. The transmit latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay will vary slightly. The minimum transmit latency ($T_{latency}$) is 34 bit times; the maximum is 38 bit times. Figure 2 illustrates the timing relationship between the transmit data bus, GTX_CLK and serial transmit pins.

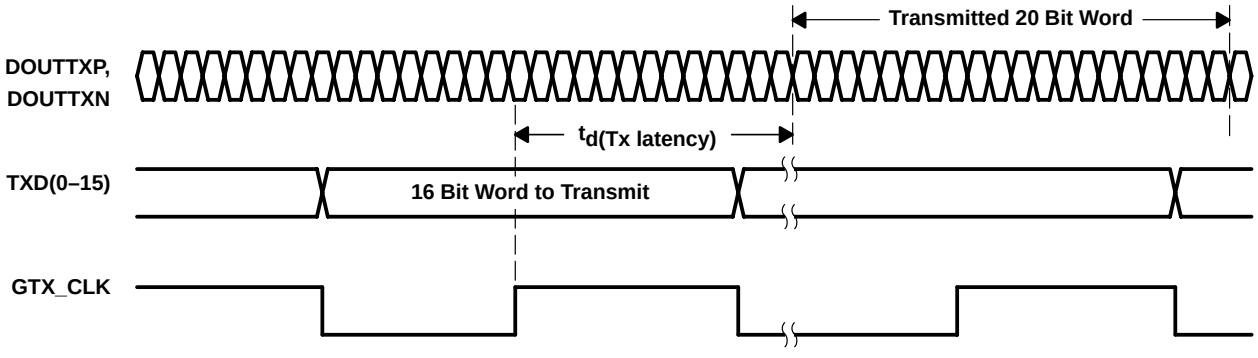


Figure 2. Transmitter Latency

transmit interface (continued)

8-b/10-b encoder

All true serial interfaces require a method of encoding to insure minimum transition density so that the receiving PLL has a minimal number of transitions in which to stay locked on. The encoding scheme maintains the signal DC balance by keeping the number of ones and zeros the same. This provides good transition density for clock recovery and improves error checking. The TLK3101 uses the 8-b/10-b encoding algorithm that is used by fiber channel and gigabit ethernet. This is transparent to the user as the TLK3101 internally encodes and decodes the data such that the user reads and writes actual 16-bit data.

The 8-b/10-b encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transmission characteristics. Since the TLK3101 is a 16 bit wide interface the data is split into two 8-bit wide bytes for encoding. Each byte is fed into a separate encoder. The encoding is dependant upon two additional input signals, TX_EN and TX_ER. When TX_EN is asserted and TX_ER deasserted then the data bit TXD[15:0] are encoded and transmitted normally. When TX_EN is deasserted and TX_ER is asserted, then the encoder will generate a carrier extend consisting of two K23.7 (F7F7) codes. If TX_EN and TX_ER are both asserted then the encoder will generate a K30.7 (FEFE) code. Table 1 provides the transmit data control decoding. Since the data is transmitted in 20 bit serial words, K codes indicating carrier extend and transmit error propagation are transmitted as two 10 bit K-codes.

Table 1. Transmit Data Controls

TX_EN	TX_ER	ENCODED 20 BIT OUTPUT
0	0	IDLE (<K28.5, D5.6> or <K28.5, D16.2>)
0	1	Carrier extend (K23.7, K23.7)
1	0	Normal data character
1	1	Transmit error propagation (K30.7, K30.7)

IDLE insertion

The encoder inserts the IDLE character set when no payload data is available to be sent. IDLE consist of a K28.5 (BC) code and either a D5.6 (C5) or D16.2 (50) character. The K28.5 character is defined by IEEE802.3z as a pattern consisting of 0011111010 (a negative number beginning disparity) with the 7 MSBs (0011111) referred to as the comma character. Since data is latched into the TLK3101 16 bits at a time, The IDLE is converted into two 10-bit codes that are transmitted sequentially. This means IDLE is transmitted during a single GTX_CLK cycle.

PRBS generator

The TLK3101 has a built-in 2^7–1 PRBS (pseudorandom bit stream) function. When the PRBSEN pin is forced high, the PRBS test is enabled. A PRBS is generated and fed into the 10 bit parallel-to-serial converter input register. Data from the normal input source is ignored during the PRBS mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a BERT (bit error rate tester), the receiver of another TLK3101 or can be looped back to the receive input. Since the PRBS is not really random but a predetermined sequence of ones and zeroes the data can be captured and checked for errors by a BERT.

parallel to serial

The parallel-to-serial shift register takes in the 20 bit wide data word multiplexed from the two parallel 8-b/10-b encoders and converts it to a serial stream. The shift register is clocked on both the rising and falling edge of the internally generated bit clock, which is 10 times the GTX_CLK input frequency. The LSB (TXD0) is transmitted first.

transmit interface (continued)

high-speed data output

The high-speed data output driver consists of a voltage mode differential driver for a 50-Ω impedance environment. The magnitude of the signal swing the differential driver pair is compatible with pseudo emitter coupled logic (PECL) levels when ac-coupled. When ac-coupled the TLK3101 can interface to a PECL transmitter and receiver. The line can be directly coupled or ac-coupled. Refer to Figure 18 and Figure 19 for termination details.

The PECL outputs also provide pre-emphasis to compensating for ac loss when driving a cable or PCB backplane over long distance (see Figure 3). The level of preemphasis is controlled by PREM as shown in Table 2.

Table 2. Preemphasis Levels

PREM	PREEMPHASIS LEVEL (%) (Vodp/Vodd –1)†
0	5%
1	20%

† Vodp: Differential voltage swing when there is a transition in the data stream.
Vodd: Differential voltage swing when there is no transition in the data stream.

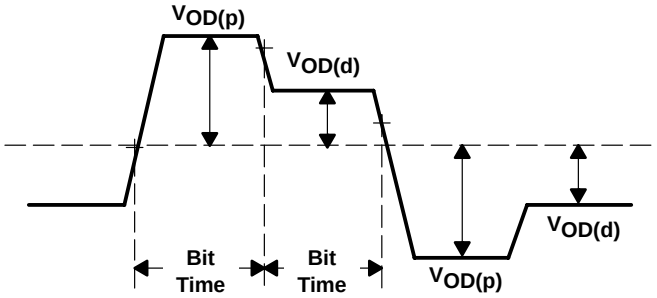


Figure 3. Output Differential Voltage Under Preemphasis (|VTXP – VTXN|)

receive interface

The receiver portion of the TLK3101 accepts 8-b/10-b encoded differential serial data. The interpolator and clock recovery circuit will lock to the data stream and extract the bit rate clock. This recovered clock is used to retime the input data stream. The serial data is then aligned to two separate 10-bit word boundaries, 8-b/10-b decoded and output on a 16 bit wide parallel bus synchronized to the extracted receive clock.

receive data bus

The receive bus interface drives 16 bit wide single-ended TTL parallel data at the RXD[0:15] pins. Data is valid on the rising edge of RX_CLK when RX_DV/LOS is asserted high and RX_ER is deasserted low. The RX_CLK is used as the recovered word clock. The data, enable and clock signals are aligned as shown in Figure 4. Detailed timing information can be found in the TTL output switching characteristics table.

receive data bus (continued)

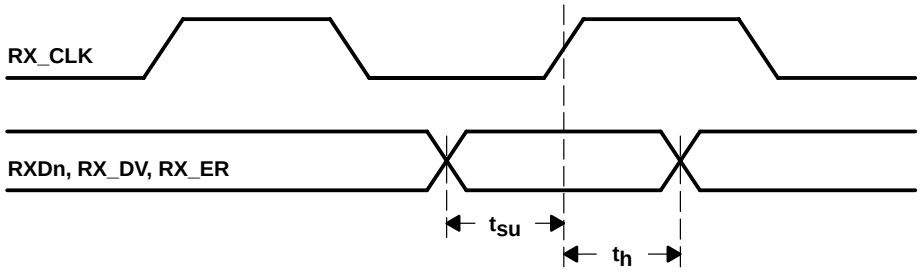


Figure 4. Receive Timing Waveform

data reception latency

The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RXD0 received as first bit. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay will vary slightly. The minimum receive latency ($R_{latency}$) is 76 bit times; the maximum is 107 bit times. Figure 5 illustrates the timing relationship between the serial receive pins, the recovered word clock (RX_CLK), and the receive data bus.

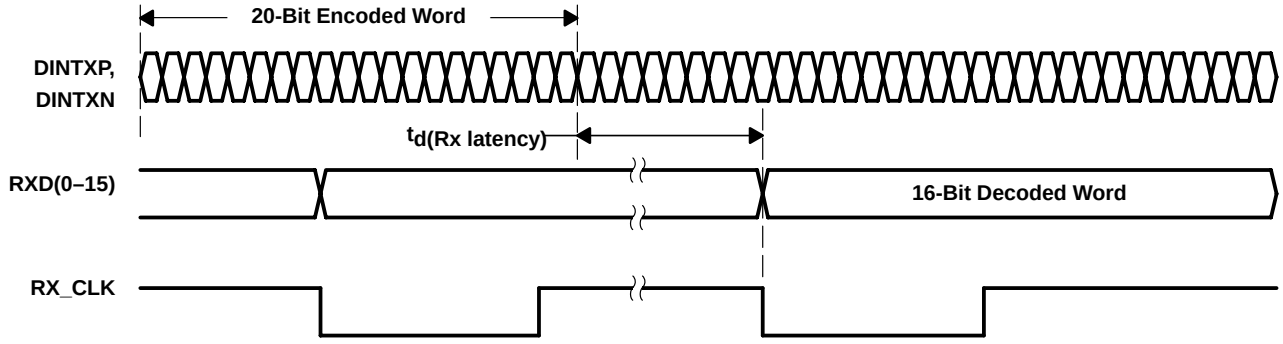


Figure 5. Receiver Latency

serial to parallel

Serial data is received on the DINRXP, DINRXN pins. The interpolator and clock recovery circuit will lock to the data stream if the clock to be recovered is within ±200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. The 10 bit wide parallel data is then multiplexed and fed into two separate 8-b/10-b decoders where the data is then synchronized to the incoming data steam word boundary by detection of the K28.5 synchronization pattern.

receive interface (continued)

common detect and 8-b/10-b decoding

The TLK3101 has two parallel 8-b/10-b decode circuits. Each 8-b/10-b decoder converts 10 bit encoded data (half of the 20 bit received word) back into 8 bits. The comma detect circuit is designed to provide for byte synchronization to an 8-b/10-b transmission code. When parallel data is clocked into a parallel to serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again a way is needed to be able to recognize the byte boundary again. Generally this is accomplished through the use of a synchronization pattern. This is generally a unique pattern of 1s and 0s that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8-bit/10-bit encoding contains a character called the comma (b'0011111' or b'1100000') which is used by the comma detect circuit on the TLK3101 to align the received serial data back to its original byte boundary. The decoder detects the K28.5 comma, generating a synchronization signal aligning the data to their 10 bit boundaries for decoding. It then converts the data back into 8 bit data, removing the control words. The output from the two decoders is latched into the 16 bit register synchronized to the recovered parallel data clock (RX_CLK) and the output is valid on the rising edge of RX_CLK.

It is possible for a single bit error in a data packet to be misinterpreted as a comma on an erroneous boundary. If the erroneous comma were taken as the new byte boundary, all subsequent data would be erroneously decoded until a properly aligned comma was detected. To prevent a data bit error in a data packet from being interpreted as a comma, the comma word alignment circuit is turned off after receiving a properly aligned comma after the link is properly established. The link is established after three idle patterns or one valid data pattern is properly received. The comma alignment circuit is re-enabled when the synchronization state machine detects a loss of synchronization condition (see synchronization and initialization).

Two output signals, RX_DV/LOS and RX_ER, are generated along with the decoded 16-bit data output on the RXD[0:15] pins. The output status signals are asserted according to Table 3. When the TLK3101 decodes normal data and outputs the data on RXD[0:15], RX_DV/LOS is asserted (logic high) and RX_ER is deasserted (logic low). When the TLK3101 decodes a K23.7 code (F7F7) indicating carrier extend, RX_DV/LOS is deasserted and RX_ER is asserted. If the decoded data is not a valid 8-b/10-b code, an error is reported by the assertion of both RX_DV/LOS and RX_ER. If the error was due to an error propagation code, the RXD[15:0] pins will output hex FEFE. If the error was due to an invalid pattern, the data output on RXD is undefined. When the TLK3101 decodes an IDLE code, both RX_DV/LOS and RX_ER are deasserted and a K28.5 (BC) code is output on the RXD[7:0] pins and either a D5.6 (C5) or D16.2 (50) code is output on the RXD[15:8] pins.

Table 3. Receive Status Signals

RECEIVED 20 BIT DATA	RX_DV/LOS	RX_ER
IDLE (<K28.5, D5.6>, <K28.5, D16.2>)	0	0
Carrier extend (K23.7, K23.7)	0	1
Normal data character (DX.Y)	1	0
Receive error propagation (K30.7, K30.7)	1	1

loss of signal detection

The TLK3101 has a loss of signal detection circuit for conditions where the incoming signal no longer has a sufficient voltage level to keep the clock recovery circuit in lock. The signal detection circuit is intended to be an indication of gross signal error conditions such as a detached cable or no signal being transmitted, and not an indication of signal coding health. The TLK3101 reports this condition by asserting, RX_DV/LOS, RX_ER and RXD[0:15] all to a high state. As long as the signal is above 200 mV in differential magnitude, the LOS circuit will not signal an error condition.

receive interface (continued)

power down mode

When the ENABLE pin is deasserted low, the TLK3101 will go into a power down mode. In the power down mode, the serial transmit pins (DOUTTXP, DOUTTXN), the receive data bus pins (RXD[0:15]), and RX_ER will go into a high-impedance state. In the power-down mode the RX_DV/LOS pin acts as an output of the signal detection circuit which remains active. If the signal detection circuit detects a valid differential signal amplitude of >200 mV on each of the serial receive pins (DINRXP, DINRXN), RX_DV/LOS is driven high. If no signal of sufficient amplitude is detected, the signal detection circuit will indicate a loss of signal by driving RX_DV/LOS low. In the power-down condition, the signal detection circuit draws less than 5 mW.

synchronization and initialization

The TLK3101 has a synchronization state machine which is responsible for handling link initialization and synchronization. Upon power up or reset, the state machine enters the acquisition (ACQ) state and searches for IDLE. Upon receiving three consecutive IDLEs or carrier extends, the state machine will enter the synchronization (SYNC) state. If, during the acquisition process, the state machine receives valid data or an error propagation code, it will immediately transition to the SYNC state. The SYNC state is the state for normal device transmission and reception. The initialization and synchronization state diagram is provided in Figure 6.

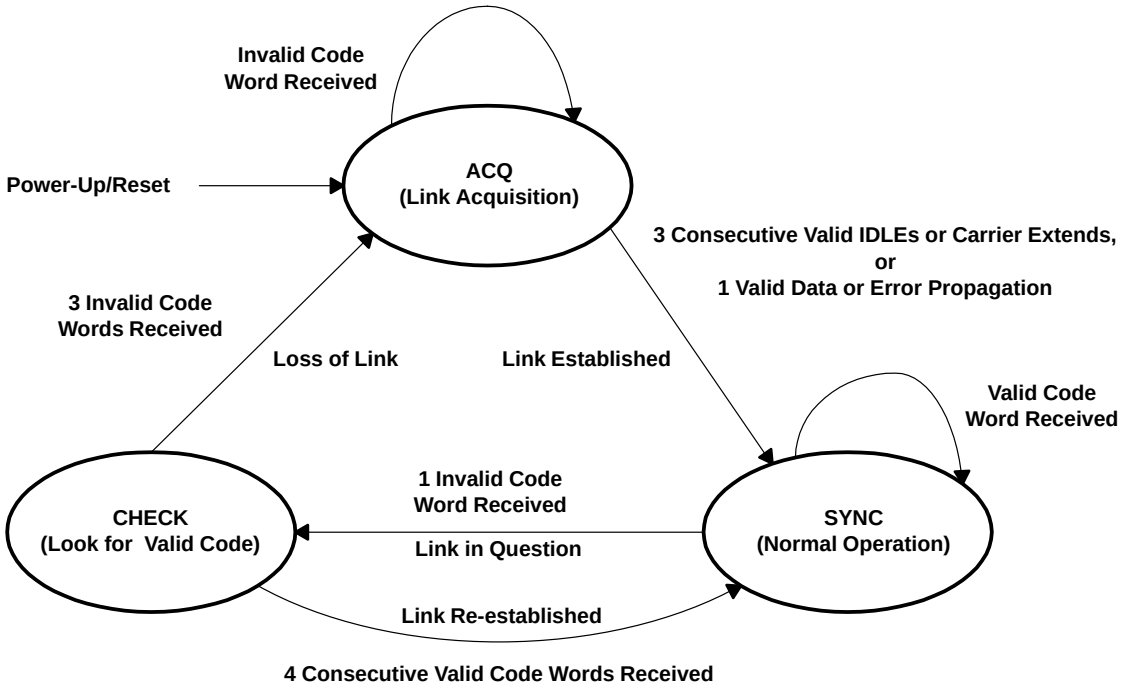


Figure 6. Initialization and Synchronization State Diagram

If, during normal transmission and reception, an invalid code is received, the TLK3101 will notify the attached system or protocol device as described in comma detect and 8-b/10-b decoding. The synchronization state machine will transition to the CHECK state. The CHECK state will determine whether the invalid code received was caused by a spurious event or a loss of the link. If, in the CHECK state, the decoder sees 4 consecutive valid codes, the state machine will determine the link is good and transition back to the SYNC state for normal operation. If, in the CHECK state, the decoder sees three invalid codes (not required to be consecutive), the TLK3101 will determine a loss of the link has occurred and transition the synchronization state machine back to the link acquisition state (ACQ).

synchronization and initialization (continued)

The state of the transmit data bus, control pins, and serial outputs during the link acquisition process is illustrated in Figure 7.

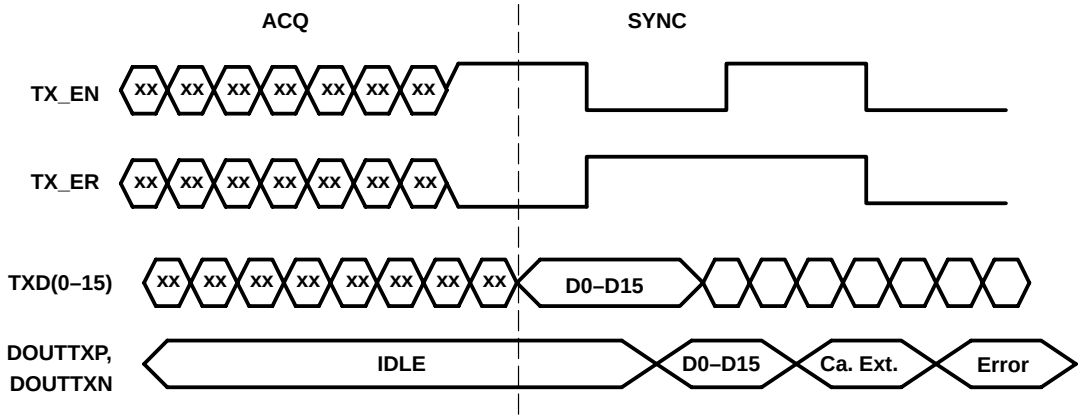


Figure 7. Transmit Side Timing Diagram

The state of the receive data bus, status pins, and serial inputs during the link acquisition process is illustrated in Figure 8 and Figure 9.

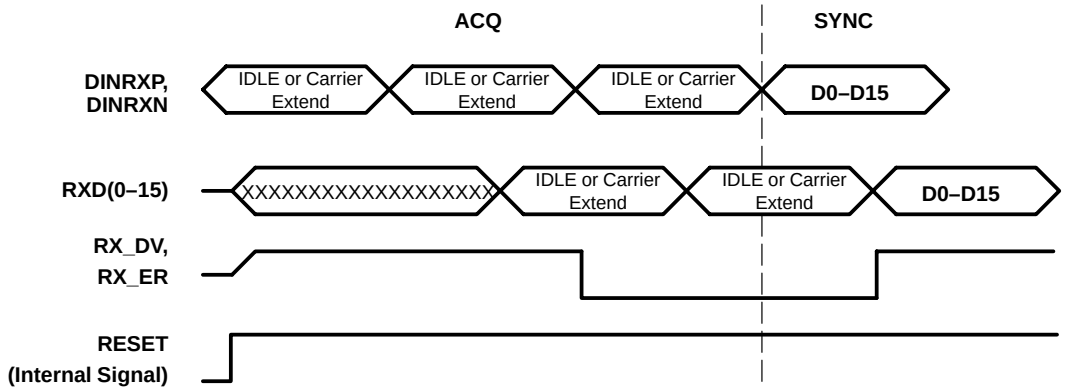


Figure 8. Receive Side Timing Diagram (IDLE or Carrier Extend)

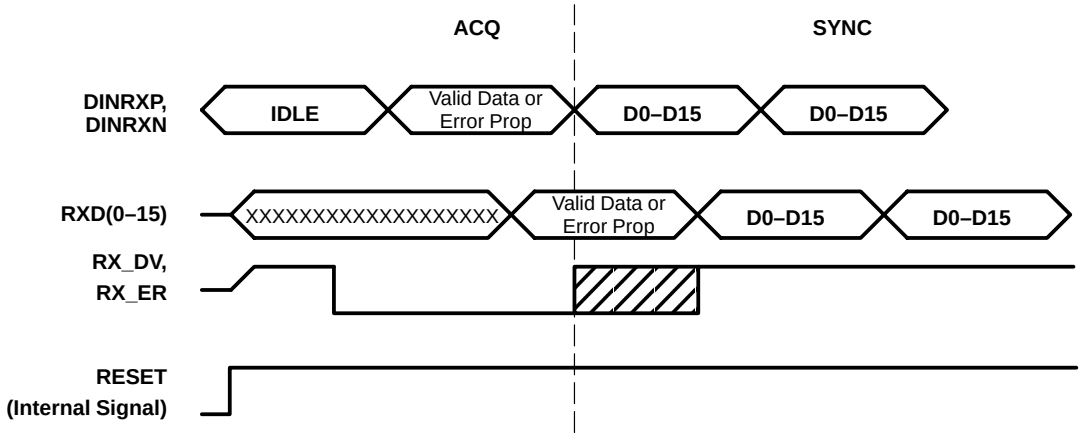


Figure 9. Receive Side Timing Diagram (Valid Data or Error Propagation)

redundant port operation

The TLK3101 allows users to design redundant ports by connecting receive data bus pins from two TLK3101 devices together. Asserting LCKREFN to a low state will cause the receive data bus pins, RXD[0:15], RX_CLK and RX_ER, RX_DV/LOS to go to a high-impedance state.

PRBS verification

The TLK3101 also has a built-in BERT function in the receiver side that is enabled by PRBSEN. It checks for errors and reports the errors by forcing the RX_ER/PRBSPASS pin low.

reference clock input

The reference clock (GTX_CLK) is an external input clock that synchronizes the transmitter interface. The reference clock is then multiplied in frequency 10 times to produce the internal serialization bit clock. The internal serialization bit clock is frequency-locked to the reference clock and used to clock out the serial transmit data on both its rising and falling edges, providing a serial data rate that is 20 times the reference clock.

operating frequency range

The TLK3101 is optimized for operation at a serial data rate of 3.125 Gbit/s. The TLK3101 may operate at a serial data rate between 2.5 Gbit/s to 3.125 Gbit/s. GTX_CLK must be within ±100 PPM of the desired parallel data rate clock.

testability

The TLK3101 has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The ENABLE pin allows for all circuitry to be disabled so that a quiescent current test can be performed. The PRBS function allows for BIST (built-in self-test).

loop-back testing

The transceiver can provide a self-test function by enabling (LOOPEN) the internal loopback path. Enabling this pin will cause serial transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. The external differential output is held in a high-impedance state during the loopback testing.

built-in self-test

The TLK3101 has a BIST (built-in self-test) function. By combining PRBS with loopback, an effective self-test of all the circuitry running at full speed can be realized. The successful completion of the BIST is reported on the RX_ER/PRBS_PASS pin.

power-on reset

Upon application of minimum valid power, the TLK3101 generates a power-on reset. During the power-on reset the RXD, RX_ER and RX_DV/LOS signal pins go to 3-state mode. RX_CLK is held low. The length of the power-on reset cycle is dependent upon the REFCLK frequency but is less than 1-ms in duration.

Terminal Functions

signal

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
DOUTTXP DOUTTXN	60 59	Output†	Serial transmit outputs. DOUTTXP and DOUTTXN are differential serial outputs that interface to copper or an optical I/F module. These terminals transmit NRZ data at a rate of 20 times the GTX_CLK value. DOUTTXP and DOUTTXN are put in a high-impedance state when LOOPEN is high and are active when LOOPEN is low . During power-on-reset these pins are high-impedance.
DINRXP DINRXN	54 53	Input	Serial receive inputs. DINRXP and DINRXN together are the differential serial input interface from a copper or an optical I/F module.
GTX_CLK	8	Input	Reference clock. GTX_CLK is a continuous external input clock that synchronizes the transmitter interface signals TX_EN, TX_ER and TXD. The frequency range of GTX_CLK is 125 MHz to 156.25 MHz. The transmitter uses the rising edge of this clock to register the 16-bit input data (TXD) for serialization.
LCKREFN	25	Input‡	Lock to reference. When LCKREFN is low, the receiver clock is frequency locked to GTX_CLK. This places the device in a transmit only mode, since the receiver is not tracking the data. When LCKREFN is asserted low, the receive data bus pins, RXD[0:15], RX_CLK and RX_ER, RX_DV/LOS are in a high-impedance state. When LCKREFN is deasserted high, the receiver is locked to the received data stream and must receive valid codes from the synchronization state machine before the transmitter is enabled.
TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7 TXD8 TXD9 TXD10 TXD11 TXD12 TXD13 TXD14 TXD15	62 63 64 2 3 4 6 7 10 11 12 14 15 16 17 19	Input	Transmit data bus. These inputs carry the 16-bit parallel data output from a protocol device to the transceiver for encoding, serialization, and transmission. This 16-bit parallel data is clocked into the transceiver on the rising edge of GTX_CLK as shown in Figure 10.
RXD0 RXD1 RXD2 RXD3 RXD4 RXD5 RXD6 RXD7 RXD8 RXD9 RXD10 RXD11 RXD12 RXD13 RXD14 RXD15	51 50 49 47 46 45 44 42 40 39 37 36 35 34 32 31	Output†	Receive data bus. These outputs carry 16-bit parallel data output from the transceiver to the protocol device, synchronized to RX_CLK. The data is valid on the rising edge of RX_CLK as shown in Figure 12. These pins are in high-impedance state during power-on reset.
RX_CLK	41	Output§	Recovered clock. Output clock that is synchronized to RXD, RX_ER, RX_DV/LOS. RX_CLK is the recovered serial data rate clock divided by 20. RX_CLK is held low during power-on reset.

† Hi-Z on power up
‡ Internal pullup
§ Low on power up

Terminal Functions (Continued)

signal (continued)

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
PREM	56	Input‡	Preemphasis control. Selects the amount of preemphasis to be added to the high speed data output drivers. Left low or unconnected, 5% of pre-emphasis is added. Pulled high, 20% of preemphasis is added.
RX_ER/ PRBS_PASS	29	Output†	Receive error. When RX_ER and RX_DV/LOS are asserted, indicates that an error was detected somewhere in the frame presently being output on the receive data bus. When RX_ER is asserted and RX_DV/LOS is deasserted, indicates that carrier extension data is being presented. RX_ER goes to high impedance state during power-on reset. When PRBSEN= low (deasserted), this pin is used to indicate receive error (RX_ER). When PRBSEN = high (asserted), this pin indicates status of the PRBS test results (high=pass).
RX_DV/ LOS	30	Output†	Receive data valid. RX_DV/LOS is output by the transceiver to indicate that recovered and decoded data is being output on the receive data bus. RX_DV/LOS is asserted continuously from the first recovered word of the frame through the final recovered word and is deasserted prior to the first rising edge of RX_CLK that follows the final word. RX_DV/LOS is in high-impedance state during power-on reset. If, during normal operation, the differential signal amplitude on the serial receive pins is below 200 mV, RX_DV/LOS is asserted high along with RX_ER and the receive data bus to indicate a loss of signal condition. If the device is in power-down mode, RX_DV/LOS is the output of the signal detect circuit and is asserted low when a loss of signal condition is detected.
TX_EN	20	Input‡	Transmit enable. TX_EN in combination with TX_ER indicates the protocol device is presenting data on the transmit data bus for transmission. TX_EN must be high with the first word of the preamble and remain asserted while all words to be transmitted are presented on the transmit data bus. TX_EN must be negated prior to the first rising edge of GTX_CLK following the final word of a frame.
TX_ER	22	Input‡	Transmit error coding. When TX_ER and TX_EN are high, indicates that the transceiver generates an error somewhere in the frame presently being transferred. When TX_ER is asserted and TX_EN is deasserted, indicates the protocol device is presenting carrier extension data. When TX_ER is deasserted with TX_EN asserted, indicates that normal data is being presented.

† Hi-Z on power-up
‡ Internal pull-down

test

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
ENABLE	24	Input§	Device enable. When this pin is held low, the device is placed in power-down mode. Only the signal detect circuit on the serial receive pair is active. When asserted high, the transceiver goes into power-on reset before beginning normal operation.
LOOPEN	21	Input‡	Loop enable. When LOOPEN is high, the internal loopback path is activated. The transmitted serial data is directly routed internally to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The DOUTTXP and DOUTTXN outputs are held in a high-impedance state during the loopback test. LOOPEN is held low during standard operational state with external serial outputs and inputs active.
PRBSEN	26	Input‡	PRBS test enable. When asserted high results of pseudorandom bit stream (PRBS) tests can be monitored on the RX_ER/PRBS_PASS pin. A high on PRBS_PASS indicates that valid PRBS is being received.
TESTEN	27	Input‡	Test mode enable. This pin should be left unconnected or tied low.

‡ Internal pulldown
§ Internal pullup

Terminal Functions (Continued)

power

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
V_{DD}	1, 9, 23, 38, 48	Supply	Digital logic power. Provides power for all digital circuitry and digital I/O buffers.
V_{DDA}	55, 57	Supply	Analog power. VDDA provides a supply reference for the high-speed analog circuits, receiver and transmitter
GNDA	52, 58, 61	Ground	Analog ground. GNDA provides a ground reference for the high-speed analog circuits, RX and TX.
GND	5, 13, 18, 28, 33, 43	Ground	Digital logic ground. Provides a ground for the logic circuits and digital I/O buffers.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . –0.3 V to 3 V
Voltage range at TXD, ENABLE, GTX_CLK, TX_EN, TX_ER, LOOPEN, PRBS_PASS . . . . . –0.3 V to 4 V
Voltage range at any other terminal except above . . . . . –0.3 V to V_{DD} + 0.3 V
Package power dissipation, P_D . . . . . See Dissipation Rating Table
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Electrostatic discharge . . . . . HBM:3 kV, CDM: 1.5 kV
Characterized free-air operating temperature range, T_A . . . . . –40°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltages, are with respect to network ground.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
RCP64§	5.25 W	46.58 mW/°C	2.89 W
RCP64¶	3.17 W	23.70 mW/°C	1.74 W
RCP64#	2.01 W	13.19 mW/°C	1.11 W

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).
§ 2 oz. Trace and copper pad with solder
¶ 2 oz. Trace and copper pad without solder
# Standard JEDEC high-K board
For more information, refer to TI application note *PowerPAD Thermally Enhanced Package*, TI literature number SLMA002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage				2.3	2.5	2.7	V
I_{CC}	Supply current	V_{DD} = 2.5V,	Freq = 2.5 Gb/sec,	PRBS pattern		135		mA
		V_{DD} = 2.5V,	Freq = 3.125 Gb/sec,	PRBS pattern		180		
P_D	Power dissipation	V_{DD} = 2.5V,	Freq = 2.5 Gb/sec,	PRBS pattern		337		mW
		V_{DD} = 2.5V,	Freq = 3.125 Gb/sec,	PRBS pattern		450		
		V_{DD} = 2.7V,	Freq = 3.125 Gb/sec,	Worst case pattern			600	
	Shutdown current	Enable = 0,	Vdda + Vdd pins = MAX			20		µA
	PLL start-up lock time	VDD,VDDA = 2.3V,	EN ↑ to PLL acquire			0.1	0.4	ms
	Data acquisition time					1024		bits
T_A	Operating free-air temperature				–40		85	°C

reference clock (GTX_CLK) timing requirements over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f	Frequency	Minimum data rate	TYP–0.01%	125	TYP+0.01%	MHz
		Maximum data rate	TYP–0.01%	156.25	TYP+0.01%	
	Frequency tolerance		–100		100	ppm
	Duty cycle		40%	50%	60%	
	Jitter	Peak to peak			40	ps

TTL input electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL signals: TXD0 ..TXD15, GTX_CLK, LOOPEN, LCKREFN, PRBS_PASS

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	See Figure 10			1.7		3.6	V
V_{IL}	Low-level input voltage	See Figure 10					0.80	V
I_{IH}	Input high current	V_{DD} = MAX,	V_{IN} = 2 V				40	μV
I_{IL}	Input low current	V_{DD} = MAX,	V_{IN} = 0.4 V		–40			μV
C_I		0.8 V to 2 V					4	pF
t_r	Rise time, GTX_CLK, TX_EN, TX_ER, TXD	0.8 V to 2 V,	C = 5 pF,	See Figure 10		1		ns
t_f	Fall time, GTX_CLK, TX_EN, TX_ER, TXD	2 V to 0.8 V,	C = 5 pF,	See Figure 10		1		ns
t_{su}	TXD, TX_EN, TX_ER setup to ↑ GTX_CLK	See Figure 10			1.5			ns
t_h	TXD, TX_EN, TX_ER hold to ↑ GTX_CLK	See Figure 10			0.4			ns

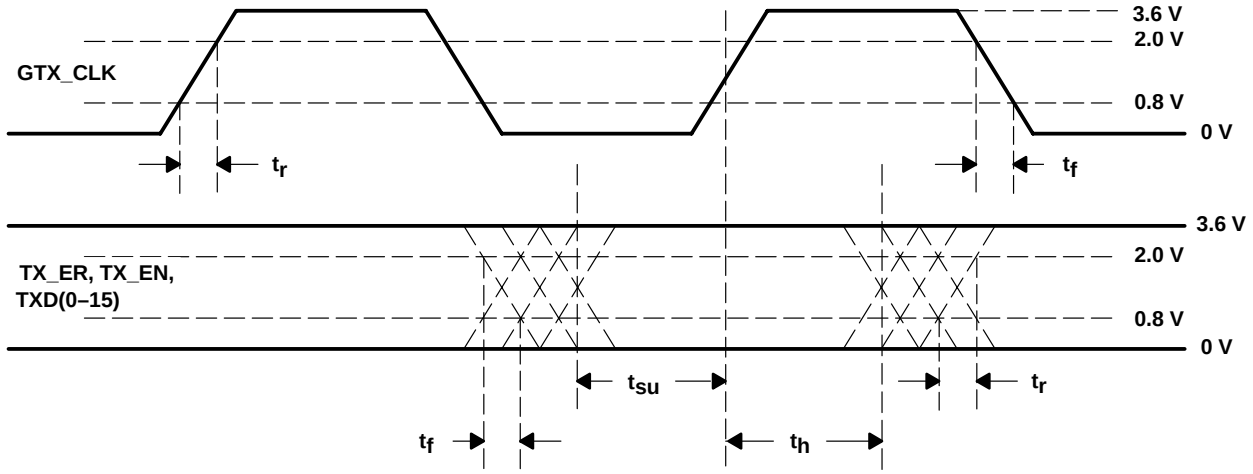


Figure 10. TTL Data Input Valid Levels for AC Measurements

TTL output switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA,	V_{DD} = MIN	2.10	2.3		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA,	V_{DD} = MIN	GND	0.25	0.5	V
$t_{r(slew)}$	Magnitude of RX_CLK, RX_ER, RX_DV/LOS, RXD slew rate (rising)	0.8 V to 2 V,	C = 5 pF, See Figure 11	0.5			V/ns
$t_{f(slew)}$	Magnitude of RX_CLK, RX_ER, RX_DV/LOS, RXD slew rate (falling)	0.8 V to 2 V,	C = 5 pF, See Figure 11	0.5			V/ns
t_{su}	RXD, RX_DV/LOS, RX_ER setup to ↑ RX_CLK	50% voltage swing, See Figure 11	GTX_CLK = 156.25 MHz	2.5			ns
			GTX_CLK = 125 MHz	3			ns
t_h	RXD, RX_DV/LOS, RX_ER hold to ↑ RX_CLK	50% voltage swing, See Figure 11	GTX_CLK = 156.25 MHz	2.5			ns
			GTX_CLK = 125 MHz	3			ns

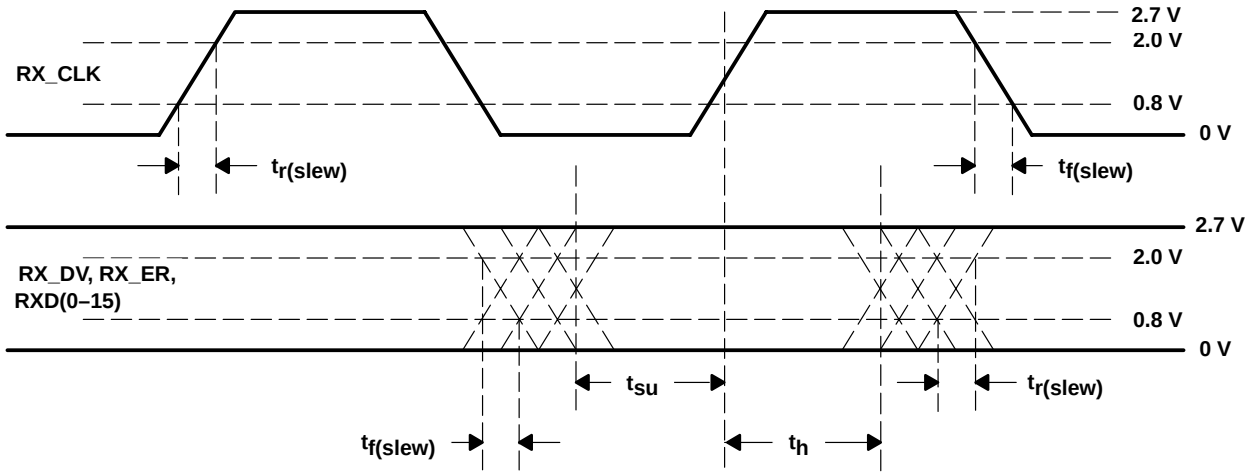


Figure 11. TTL Data Output Valid Levels for AC Measurements

transmitter/receiver characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(p)}$	Preemphasis V_{OD}, direct, $V_{OD(p)}$ = |VTXP – VTXN|	Rt = 50 Ω, PREM = high, dc-coupled, See Figure 12	655	725	795	mV
		Rt = 50 Ω, PREM = low, dc-coupled, See Figure 12	590	650	710	
$V_{OD(pp\_p)}$	Differential, peak-to-peak output voltage with preemphasis	Rt = 50 Ω, PREM = high, dc-coupled, See Figure 12	1310	1450	1590	mV_{p-p}
		Rt = 50 Ω, PREM = low, dc-coupled, See Figure 12	1180	1300	1420	
$V_{OD(d)}$	Deemphais output voltage, |VTXP – VTXN|	Rt = 50 Ω, DC-coupled, See Figure 12	540	600	660	mV
$V_{OD(pp\_d)}$	Differential, peak-to-peak output voltage with de-emphasis	Rt = 50 Ω, dc-coupled, See Figure 12	1080	1200	1320	mV_{p-p}
$V_{(cmt)}$	Transmit common mode voltage range, (VTXP + VTXN)/2	Rt = 50 Ω, See Figure 12	1000	1250	1400	mV
V_{ID}	Receiver input voltage differential, |VRXP – VRXN|		200		1600	mV
$V_{(cmr)}$	Receiver common mode voltage range, (VRXP + VRXN)/2		1000	1250	2250	mV
I_{lkg}	Receiver input leakage current		–10		10	µA
C_i	Receiver input capacitance				2	pF
	Serial data total jitter (peak-to-peak)	Differential output jitter at 3.125 Gbps, Random + deterministic, PRBS pattern		0.20		UI†
		Differential output jitter at 2.5 Gbps, Random + deterministic, PRBS pattern		0.16		UI†
t_t, t_f	Differential output signal rise, fall time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF, See Figure 12		150		ps
	Jitter tolerance	Differential input jitter, random + determinisitc, PRBS pattern at zero crossing	0.60			UI
$t_{d(Tx\ latency)}$	Tx latency	See Figure 2	34		38	bits
$t_{d(Rx\ latency)}$	Rx latency	See Figure 5	76		107	bits

† UI is the time interval of one serialized bit.

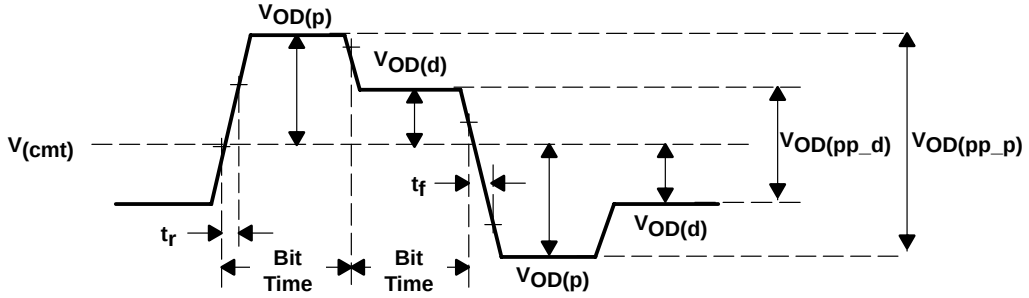
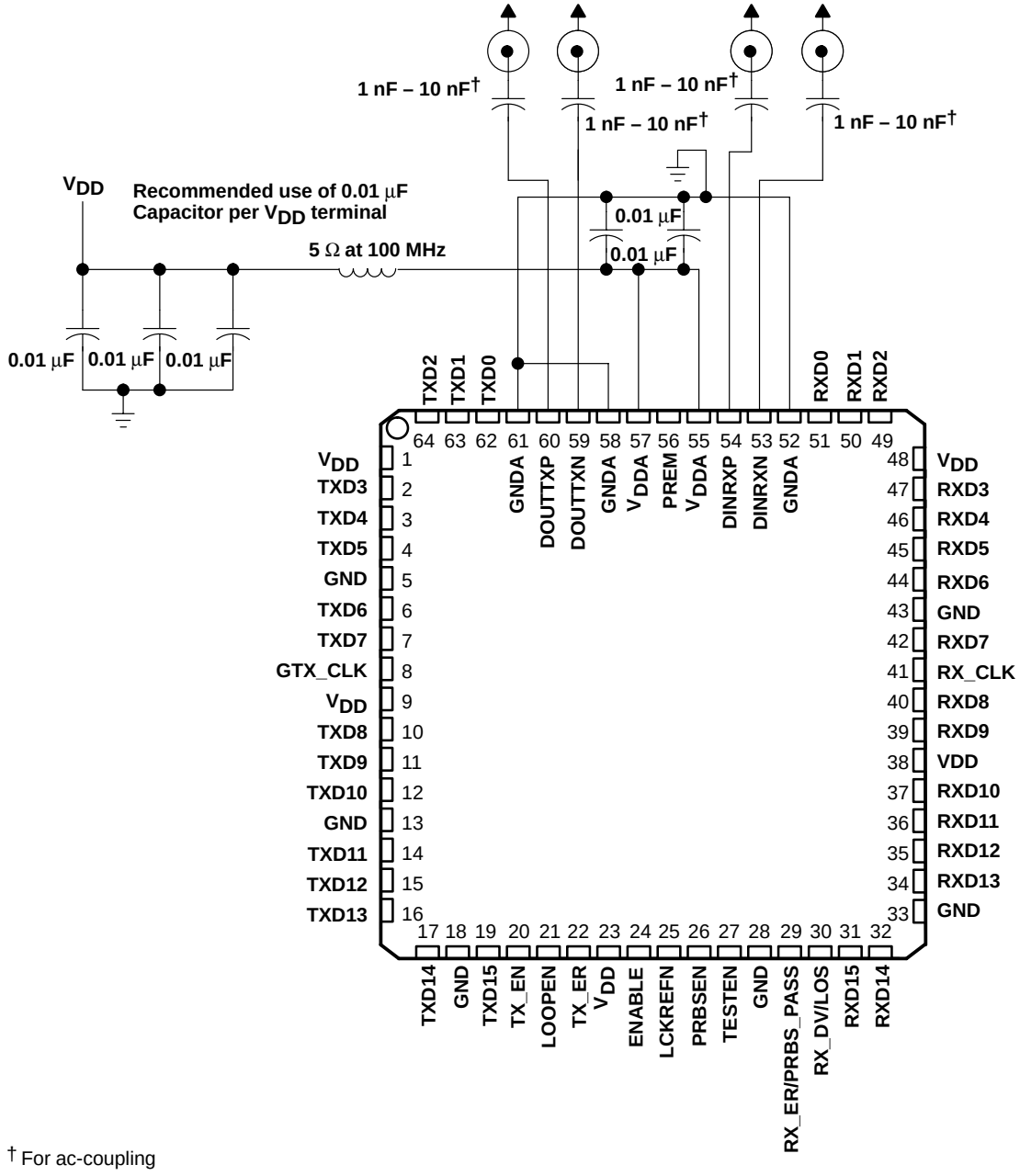


Figure 12. Differential and Common-Mode Output Voltage Definitions (|VTXP – VTXN|)

thermal characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board-mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land		21.47		°C/W
		Board-mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land		42.20		
		Board-mounted, no air flow, JEDEC test board		75.83		
$R_{\theta JC}$	Junction-to-case thermal resistance	Board-mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land		0.38		°C/W
		Board-mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land		0.38		
		Board-mounted, no air flow, JEDEC test board		7.8		



† For ac-coupling

Figure 13. External Component Interconnection

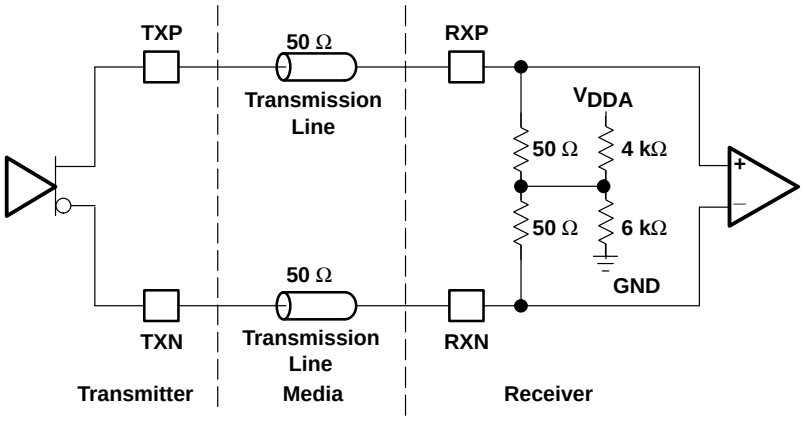


Figure 14. High-Speed I/O Directly-Coupled Mode

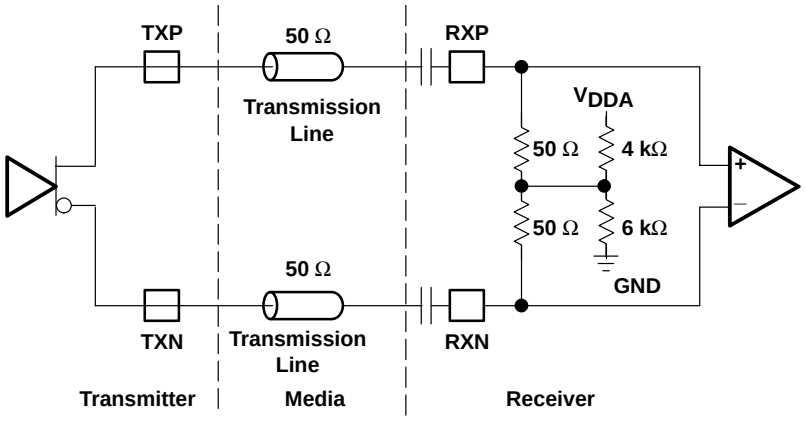


Figure 15. High-Speed I/O AC-Coupled Mode

designing with PowerPAD

The TLK3101 is housed in a high performance, thermally enhanced, 64-pin VQFP (RCP64) PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD to connection etches or vias under the package. It is strongly recommended that the PowerPAD be soldered to the thermal land. The recommended convention, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keep-out area for the 64-pin PFP PowerPAD package is 8 mm $\times$ 8 mm.

A thermal land, which is an area of solder-tinned-copper, is recommended underneath the PowerPAD package. The thermal land will vary in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: http://www.ti.com.

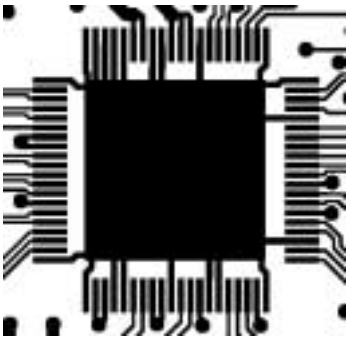


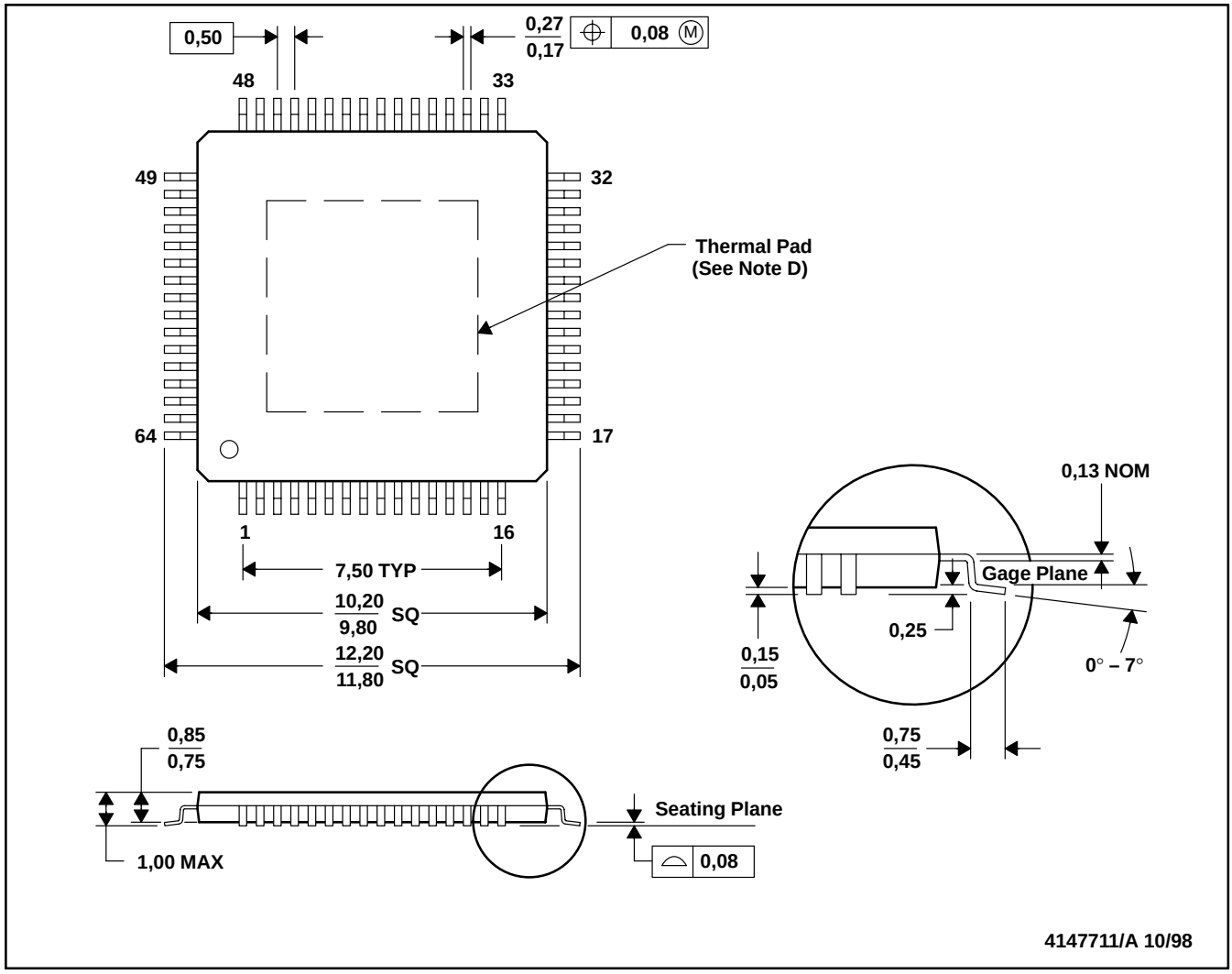
Figure 16. Example of a Thermal Land

For the TLK3101, this thermal land should be grounded to the low impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground pin landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal pins. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low impedance ground plane for the device. More information may be obtained from the TI application note *PHY Layout*, TI literature number SLLA020.

MECHANICAL DATA

RCP (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265