

ERRATA

TO THE TLK2201A, TLK2201AI ETHERNET TRANSCEIVERS DATA SHEET

(TEXAS INSTRUMENTS LITERATURE NO. SLLZ035B, June 2004)

This document is an errata to the TLK2201A data sheet (Literature No. SLLS572).

TLK2201A PLL STARTUP PROBLEM

Applies to TLK2201A devices.

Some TLK2201A have a chance of becoming stuck in a self-oscillation mode. This mode causes the device to send erratic data at a device dependent data rate while ignoring the REF_CLK input. The receiver also runs at a device dependent rate and will not receive data properly.

Conditions of Occurrence:

Condition 1: An unstable REF_CLK input with missing pulses and/or double pulses while erratically changing frequencies

OR

Toggling ENABLE

AND

Condition 2: A device dependent supply voltage and temperature that allow the self-oscillation to begin.

If the REF_CLK is stable before the power supply ramp then there is no problem with PLL startup unless the device is disabled and re-enabled using the ENABLE pin. The supply voltage and temperature is a small voltage/temperature window that allows the self-oscillation to begin. This window shifts from device to device.

Solution / Workarounds:

Avoiding this problem is possible by powering up the TLK2201A after the oscillator is completely stable and neglecting use of the ENABLE pin. If the device has entered the failure mode the PLL must be power cycled or reset to clear the error. Power cycling the device will reset the PLL and is the recommended workaround. Lab data also indicates that toggling the ENABLE pin low for ~1microseconds and then back to high the device will reset the PLL and will usually clear the failure condition, but this sequence can possibly create the failure condition and is not recommended.

TLK2201B device does not have this issue. TLK2201B pin for pin drop in replacement for the TLK2201A and is the recommended solution to this issue.

Symptoms of Recognition:

While in the self-oscillation failure mode one of the two symptom sets will be observed.

Symptom Set 1) Device appears to run at a rate much slower than the rate sent by REF_CLK. TXP/TXN run at a rate completely independent of and asynchronous to the input frequency, and the data sent will not match the data put on TD[0:9] unless it is a static pattern. The receiver runs at an independent rate asynchronous to TXP/TXN and REF_CLK. The data on RD[0:9] clocked out by RBC0 will not match the data received because the deserializer is running at an uncontrolled rate. The rates seen on TXP/TXN are typically something close to 600Mbps. There are usually a number of discrete frequencies between 20 and 58MHz as seen on the RBC0 pin that at which the receiver tends to oscillate. The actual set of frequencies of oscillation as seen on the RBC0 pin are device dependent.

Symptom Set 2) Device appears to be held in reset. All outputs RBC0, RD[0:9], TXP/TXN, etc are held in a High-Z state. This symptom set is actually a special case of symptom set 1, where the internal oscillation frequency is low enough that an internal watchdog circuit detects the frequency is too low and masks the symptoms by turning off all output buffers.

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