

## **TLK2201 PLL Startup Problem**

**Applies to** all TLK2201, TLK1201, and TLK2201JR devices currently in production as of 6/1/03.

The TLK2201 has a very small chance of entering a continuous PLL reset state, which causes bit errors on the receiver and excessive transmit jitter on the high speed output.

### **Conditions of Occurrence:**

- 1) ENABLE pin glitching low or going low for a short period of time (<100 $\mu$ s)  
-OR- a significant event on the reference clock such as loss of clock pulses or frequency change as in a clock distribution chip reset or FPGA power cycle.
- 2) Low PLLVCC power supply. The device is susceptible to this failure mode when the PLLVCC is lower than normal operation conditions such as during a board power up. After the device is in the failure mode raising the voltage will significantly lessen the effects of the mode but will not make the mode completely disappear.

### **Solution / Workarounds:**

If the device has entered the failure mode the PLL must be power cycled or reset to clear the error. Power cycling the device will reset the PLL and is the most robust method. Lab data also indicates that toggling the enable pin low for >100 $\mu$ s and then re-enabling the device when the power supply and REFCLK have reached normal operating conditions will also clear the failure condition. This problem has been fixed in TLK2201A.

### **Symptoms of Recognition:**

If the transceiver has bit errors on the receiver and or an abnormal amount of jitter with the jitter characteristic seen in figure 2. Although both are symptoms of failure the transmitter output often shows the effects more dramatically than the receiver.

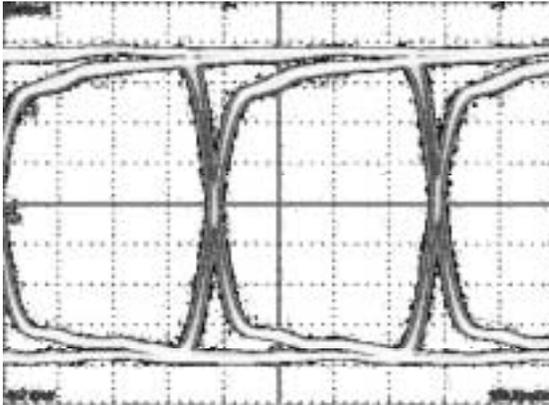


Figure 1: Normal Data Eye

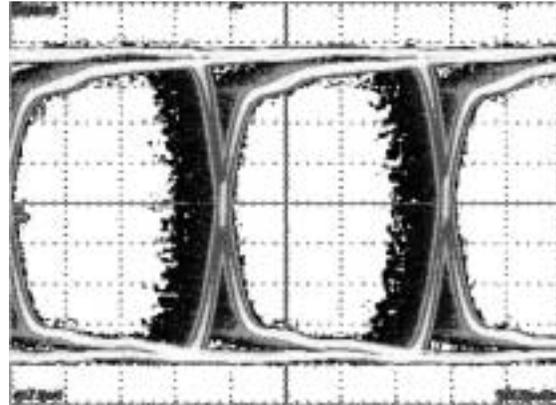


Figure 2: Data Eye in Failure Mode

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