

TOSHIBA

TLP215, TLP216

TOSHIBA PHOTOCOUPLER GaAs IRED & PHOTO-IC

TLP215, TLP216

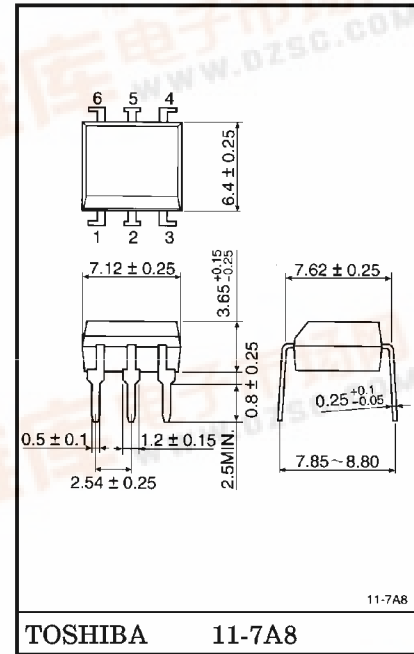
Unit in mm

- DIGITAL LOGIC INTERFACE
- MICROPROCESSOR SYSTEM INTERFACE
- ISOLATED BUS DRIVER
- LINE RECEIVER
- GROUND LOOP ELIMINATION

The TOSHIBA TLP215 and TLP216 are logic-in and logic-out type photocouplers. Both types consist of three chips : a GaAs infrared LED, LS TTL level logic IC LED driver, and photo detector which incorporates both a photo diode and TTL level logic I.C.

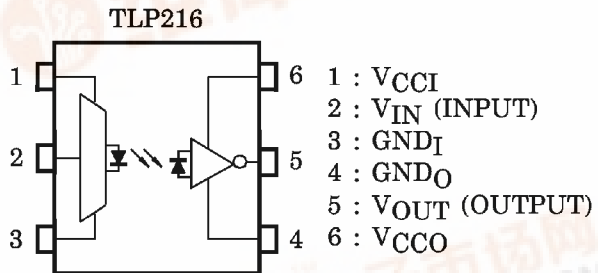
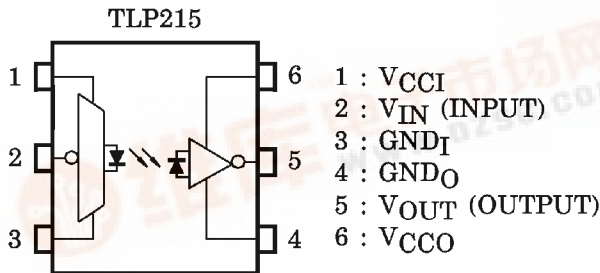
- TLP215 : Buffer Logic Type
- TLP216 : Inverter Logic Type

- Supply Voltage : $V_{CC} = 4.5 \sim 5.5V$
- Switching Speed : $t_{pHL}, t_{pLH} = 5\mu s$ (MAX.)
- Guaranteed Performance Over Temperature : $-25 \sim 80^{\circ}C$
- Isolation Voltage : 2500Vrms (MIN.)
- UL Recognized : UL1577, File No. E67349



Weight : 0.42g

PIN CONFIGURATIONS (TOP VIEW)



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TRUTH TABLE

TLP215

INPUT	OUTPUT
H	H
L	L

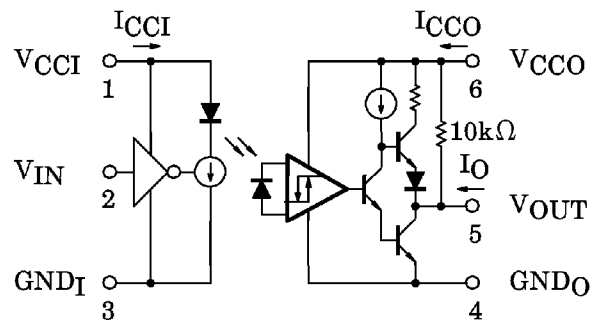
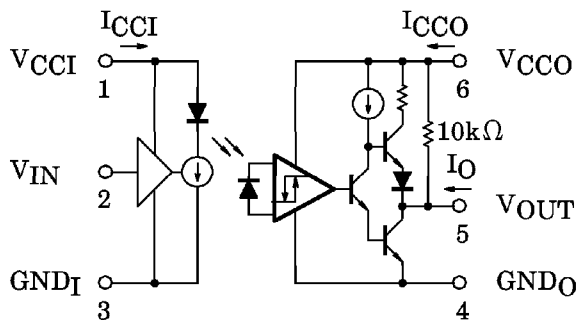
BUFFER LOGIC

TLP216

INPUT	OUTPUT
H	L
L	H

INVERTER LOGIC

SCHEMATIC



A 0.1 μ F bypass capacitor must be connected between pin 1 and 3, and between pin 4 and 6.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Supply Voltage (Note 1)	V _{CCI}	-0.5~7	V
	Input Voltage	V _{IN}	-0.5~7	V
DETECTOR	Supply Voltage (Note 1)	V _{CCO}	-0.5~7	V
	Output Voltage	V _{OUT}	-0.5~7	V
	Output Current	I _{OUT}	40 / -25	mA
	Output Power Dissipation (Note 2)	P _O	100	mW
Operating Temperature Range		T _{opr}	-40~85	°C
Storage Temperature Range		T _{stg}	-55~125	°C
Solder Temperature (10sec.)**		T _{sol}	260	°C
Isolation Voltage (AC, 1 min., R.H. ≤ 60%, Ta = 25°C) (Note 3)		B _V S	2500	V _{rms}

(Note 1) Max. 1min.

(Note 2) Derate 1.8mW / °C above 70°C.

(Note 3) Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

** Soldering portion of lead : up to 2mm from the body of the device.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{CCL} V _{CCO}	4.5	5	5.5	V
Input Voltage High	V _{IH}	2	—	V _{CC}	V
Input Voltage Low	V _{IL}	0	—	0.8	V
Output Current High	I _{OH}	—	—	-400	μA
Output Current Low	I _{OL}	—	—	8	mA
Fan Out (TTL Load)	N	—	—	4	—
Operating Temperature	T _{opr}	-25	—	85	°C

TLP215

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $T_a = -25 \sim 85^\circ\text{C}$, V_{CCI} , $V_{CCO} = 5\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.*	MAX.	UNIT
Input Supply Voltage	V_{CCI}	—	4.5	5	5.5	V
Output Supply Voltage	V_{CCO}	—	4.5	5	5.5	V
Low Level Input Voltage	V_{IL}	—	—	—	0.8	V
High Level Input Voltage	V_{IH}	—	2.0	—	—	V
Low Level Output Voltage	V_{OL}	$I_{OL} = 8.0\text{mA}$, $V_{IL} = 0.8\text{V}$ $V_{CCO} = 4.5\text{V}$	—	0.3	0.5	V
High Level Output Voltage	V_{OH}	$I_{OH} = -400\mu\text{A}$, $V_{IH} = 2\text{V}$ $V_{CCO} = 4.5\text{V}$	2.7	3.6	—	V
Low Level Input Current	I_{IL}	$V_{CCI} = 5.5\text{V}$, $V_{IL} = 0.4\text{V}$	—	-0.2	-0.4	mA
High Level Input Current	I_{IH}	$V_{CCI} = 5.5\text{V}$, $V_{IH} = 2.7\text{V}$	—	—	20	μA
Input Current at Maximum Input Voltage	I_I	$V_{CCI} = 5.5\text{V}$, $V_{IH} = 6\text{V}$	—	—	0.4	mA
Input Low Level Supply Current	I_{CCLI}	$V_{CCI} = 5.5\text{V}$, $V_{IL} = \text{GND}$	—	7	10	mA
Input High Level Supply Current	I_{CCHI}	$V_{CCI} = 5.5\text{V}$, $V_{IH} = 4.5\text{V}$	—	4	10	mA
Output Low Level Supply Current	I_{CCLO}	$V_{CCO} = 5.5\text{V}$, $V_{IL} = \text{GND}$	—	4	6.0	mA
Output High Level Supply Current	I_{CCHO}	$V_{CCO} = 5.5\text{V}$, $V_{IH} = 4.5\text{V}$	—	4.5	6.0	mA
Low Level Short Circuit Output Current (Note 4)	I_{OSL}	$V_{CCO} = 5.5\text{V}$, $V_{IL} = \text{GND}$ $V_{OUT} = 5.5\text{V}$	25	55	—	mA
High Level Short Circuit Output Current (Note 4)	I_{OSH}	$V_{CCO} = 5.5\text{V}$, $V_{IH} = 4.5\text{V}$ $V_{OUT} = 0\text{V}$	-10	-25	—	mA
Resistance (Input-Output)	R_S	$V_S = 500\text{V}$, R.H. $\leq 60\%$ $T_a = 25^\circ\text{C}$	5×10^{10}	10^{14}	—	Ω
Capacitance (Input-Output)	C_S	$V_S = 0$, $f = 1\text{MHz}$ $T_a = 25^\circ\text{C}$ (Note 3)	—	1.0	—	pF

* All typical values at $T_a = 25^\circ\text{C}$

TLP215

SWITCHING CHARACTERISTICS (Unless otherwise specified, $T_a = 25 \sim 85^\circ\text{C}$, $V_{CCI} = V_{CCO} = 5\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.*	MAX.	UNIT
Propagation Delay Time (L→H) (Note 5)	t_{pLH}	1	$R_L = 2\text{k}\Omega$, $C_L = 15\text{pF}$	—	0.5	5	μs
Propagation Delay Time (H→L) (Note 5)	t_{pHL}			—	0.5	5	μs
Output Rise Time (10–90%)	t_r		$R_L = 2\text{k}\Omega$, $C_L = 15\text{pF}$ $T_a = 25^\circ\text{C}$	—	35	—	ns
Output Fall Time (10–90%)	t_f			—	20	—	ns
Common Mode Transient Immunity at Logic High Output (Note 6)	C_{MH}	2	$V_{CM} = 50\text{V}$ $V_{OUT}(\text{Min.}) = 2\text{V}$ $T_a = 25^\circ\text{C}$	1000	—	—	$\text{V} / \mu\text{s}$
Common Mode Transient Immunity at Logic Low Output (Note 6)	C_{ML}		$V_{CM} = 50\text{V}$ $V_{OUT}(\text{Max.}) = 0.8\text{V}$ $T_a = 25^\circ\text{C}$	–1000	—	—	$\text{V} / \mu\text{s}$

* All typical values are at $T_a = 25^\circ\text{C}$

TLP216

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $T_a = -25 \sim 85^\circ\text{C}$, V_{CCI} , $V_{CCO} = 5\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.*	MAX.	UNIT
Input Supply Voltage	V_{CCI}	—	4.5	5	5.5	V
Output Supply Voltage	V_{CCO}	—	4.5	5	5.5	V
Low Level Input Voltage	V_{IL}	—	—	—	0.8	V
High Level Input Voltage	V_{IH}	—	2.0	—	—	V
Low Level Output Voltage	V_{OL}	$I_{OL} = 8.0\text{mA}$, $V_{IH} = 2\text{V}$ $V_{CCO} = 4.5\text{V}$	—	0.3	0.5	V
High Level Output Voltage	V_{OH}	$I_{OH} = -400\mu\text{A}$ $V_{IL} = 0.8\text{V}$, $V_{CCO} = 4.5\text{V}$	2.7	3.6	—	V
Low Level Input Current	I_{IL}	$V_{CCI} = 5.5\text{V}$, $V_{IL} = 0.4\text{V}$	—	-0.2	-0.4	mA
High Level Input Current	I_{IH}	$V_{CCI} = 5.5\text{V}$, $V_{IH} = 2.7\text{V}$	—	—	20	μA
Input Current at Maximum Input Voltage	I_I	$V_{CCI} = 5.5\text{V}$, $V_{IH} = 6\text{V}$	—	—	0.4	mA
Input Low Level Supply Current	I_{CCLI}	$V_{CCI} = 5.5\text{V}$, $V_{IL} = \text{GND}$	—	4	10	mA
Input High Level Supply Current	I_{CCHI}	$V_{CCI} = 5.5\text{V}$, $V_{IH} = 4.5\text{V}$	—	7	10	mA
Output Low Level Supply Current	I_{CCLO}	$V_{CCO} = 5.5\text{V}$, $V_{IH} = 4.5\text{V}$	—	4	6.0	mA
Output High Level Supply Current	I_{CCHO}	$V_{CCO} = 5.5\text{V}$, $V_{IL} = \text{GND}$	—	4.5	6.0	mA
Low Level Short Circuit Output Current (Note 4)	I_{OSL}	$V_{CCO} = 5.5\text{V}$, $V_{IH} = 4.5\text{V}$ $V_{OUT} = 5.5\text{V}$	25	55	—	mA
High Level Short Circuit Output Current (Note 4)	I_{OSH}	$V_{CCO} = 5.5\text{V}$, $V_{IL} = \text{GND}$ $V_{OUT} = 0\text{V}$	-10	-25	—	mA
Resistance (Input-Output)	R_S	$V_S = 500\text{V}$, R.H. $\leq 60\%$ $T_a = 25^\circ\text{C}$	5×10^{10}	10^{14}	—	Ω
Capacitance (Input-Output)	C_S	$V_S = 0$, $f = 1\text{MHz}$ $T_a = 25^\circ\text{C}$ (Note 3)	—	1.0	—	pF

* All typical values are at $T_a = 25^\circ\text{C}$

TLP216

SWITCHING CHARACTERISTICS (Unless otherwise specified, $T_a = -25 \sim 85^\circ\text{C}$, $V_{CCI} = V_{CCO} = 5\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.*	MAX.	UNIT
Propagation Delay Time (L→H) (Note 7)	t_{pLH}	1	$R_L = 2\text{k}\Omega$, $C_L = 15\text{pF}$	—	0.5	5	μs
Propagation Delay Time (H→L) (Note 7)	t_{pHL}			—	0.5	5	μs
Output Rise Time (10–90%)	t_r		$R_L = 2\text{k}\Omega$, $C_L = 15\text{pF}$ $T_a = 25^\circ\text{C}$	—	35	—	ns
Output Fall Time (10–90%)	t_f			—	20	—	ns
Common Mode Transient Immunity at Logic High Output (Note 8)	C_{MH}	2	$V_{CM} = 50\text{V}$ $V_{OUT}(\text{Min.}) = 2\text{V}$ $T_a = 25^\circ\text{C}$	–1000	—	—	$\text{V} / \mu\text{s}$
Common Mode Transient Immunity at Logic Low Output (Note 8)	C_{ML}		$V_{CM} = 50\text{V}$ $V_{OUT}(\text{Max.}) = 0.8\text{V}$ $T_a = 25^\circ\text{C}$	1000	—	—	$\text{V} / \mu\text{s}$

* All typical values are at $T_a = 25^\circ\text{C}$

(Note 4) Duration of output short circuit time should not exceed 10ms

(Note 5) The t_{pLH} propagation delay is measured from the point on the trailing edge of the input pulse to the 1.3V point on the leading edge of the output pulse.
The t_{pHL} propagation delay is measured from the point on the leading edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.

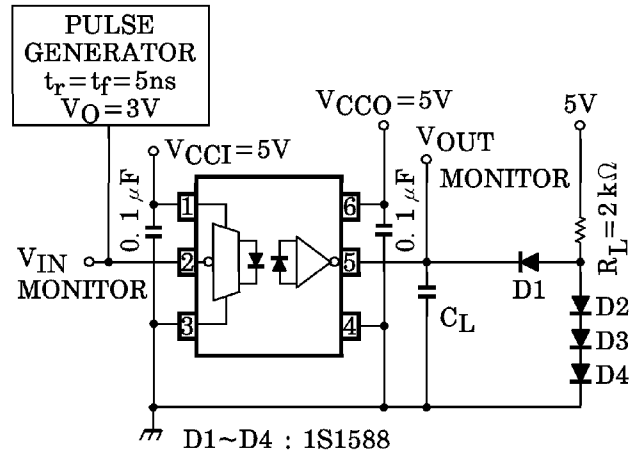
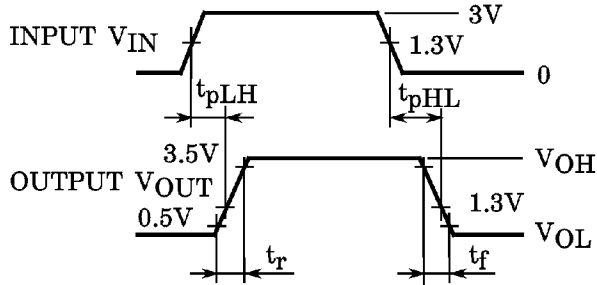
(Note 6) C_{ML} is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_{OUT} < 0.8\text{V}$).
 C_{MH} is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_{OUT} > 2.0\text{V}$).

(Note 7) The t_{pLH} propagation delay is measured from the point on the trailing edge of the input pulse to the 1.3V point on the leading edge of the output pulse.
The t_{pHL} propagation delay is measured from the point on the leading edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.

(Note 8) C_{ML} is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_{OUT} < 0.8\text{V}$).
 C_{MH} is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_{OUT} > 2.0\text{V}$).

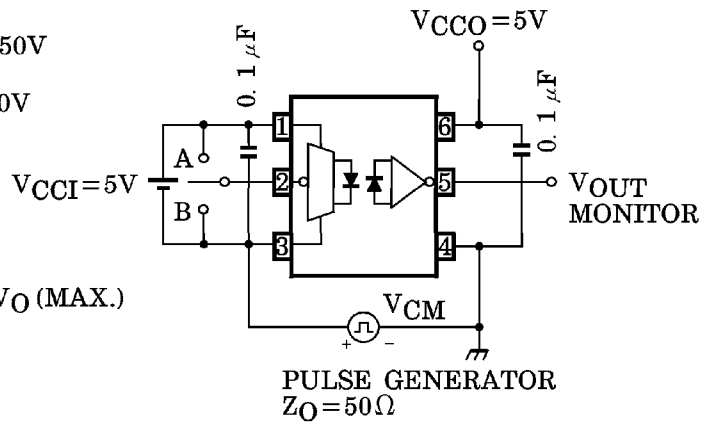
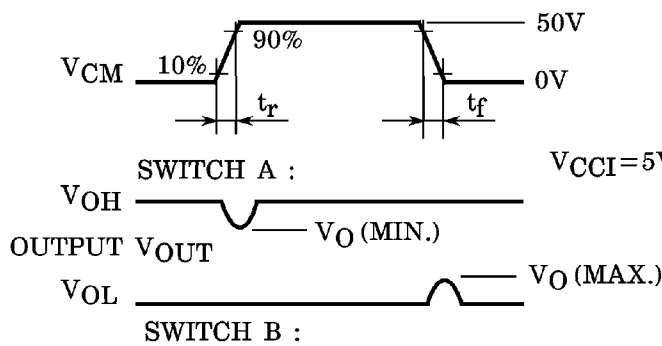
(Note 9) A ceramic capacitor ($0.1\mu\text{F}$) should be connected from pin 1 to pin 3, and from pin 4 to pin 6 (V_{CC} -GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the switching property. The total lead length between capacitor and coupler should not exceed 1cm.

TEST CIRCUIT 1 : t_{pLH} , t_{pHL} , t_r and t_f (TLP215)



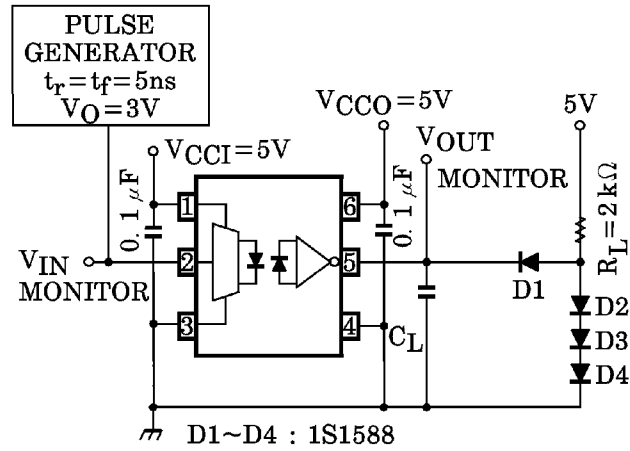
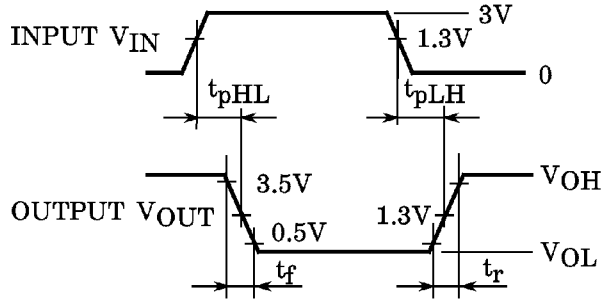
C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 2 : Common Mode Transient Immunity (TLP215)



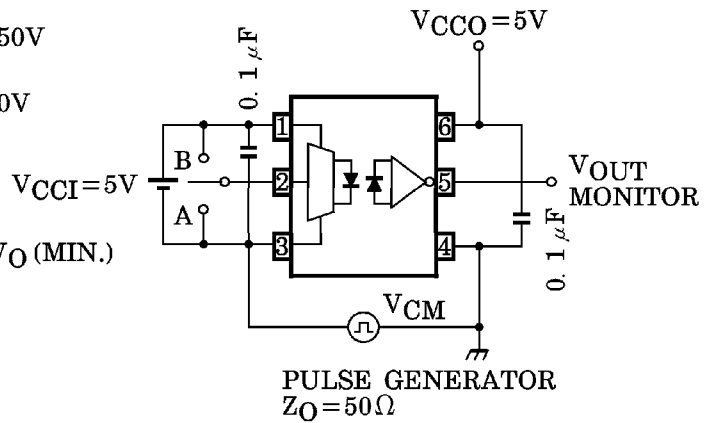
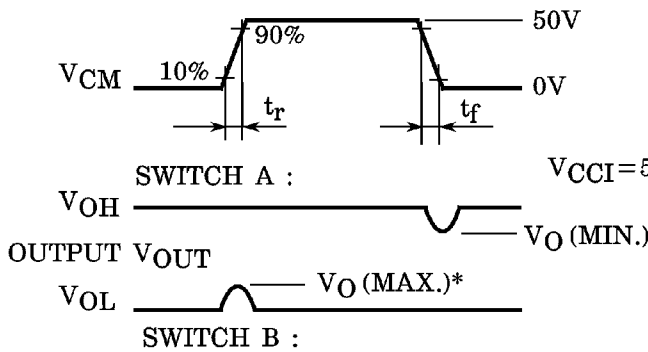
$$CM_H = \frac{45(V)}{t_r(\mu s)}, \quad CM_L = \frac{45(V)}{t_f(\mu s)}$$

TEST CIRCUIT 3 : t_{pHL} , t_{pHL} , t_r and t_f (TLP216)



C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 4 : Common Mode Transient Immunity (TLP216)



$$CM_H = \frac{45 (V)}{t_f (\mu s)}, \quad CM_L = \frac{45 (V)}{t_r (\mu s)}$$