2.7 V TO 5.5 V, HIGH-SPEED LOW-POWER RECONFIGURABLE ANALOG-TO-DIGITAL CONVERTER WITH 4-INPUT, DUAL S/H, PARALLEL INTERFACE, AND POWER DOWN

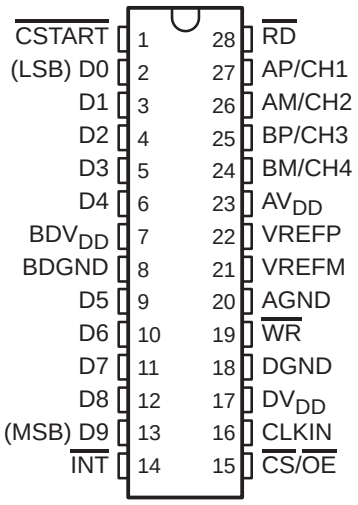
SLAS162 – SEPTEMBER 1998

- 2 MSPS Max Throughput at 10 Bit (Single Channel), ±1 LSB DNL, ±1 LSB INL MAX
- 3 MSPS Max Throughput at 8 Bit (Single Channel), ±1 LSB DNL, ±1 LSB INL MAX
- 7 MSPS Max Throughput at 4 Bit (Single Channel), ±0.4 LSB DNL, ±0.4 LSB INL MAX
- No Missing Code for External Clock Up to 15 MHz at 5.5 V, 12 MHz at 2.7 V
- ENOB 9.4 Bit, SINAD 57.8 dB, SFDR –70.8 dB, THD –68.8 dB, at fi = 800 kHz, 10 Bit
- Wide Input Bandwidth for Undersampling (75 MHz at 1 dB, >120 MHz at –3 dB) at R_S = 1 kΩ
- Software Programmable Power Down, (1 μA), Auto Powerdown (120 μA)
- Single Wide Range Supply 2.7 VDC to 5.5 VDC
- Low Supply Current 11 mA at 5.5 V, 10 MHz; 7 mA at 2.7 V, 8 MHz Operating
- Simultaneous Sample and Hold:
  Dual Sample and Hold Matched Channels
  Multi Chip Simultaneous Sample and Hold Capable
- Programmable Conversion Modes:
  Interrupt-Driven for Shorter Latency
  Continuous Modes Optimized for MIPS Sensitive DSP Solutions
- Built-In Internal/System Mid-Scale Error Calibration
- Built-In Mux With 2 Differential or 4 Single-Ended Input Channels
- Low Input Capacitance (10 pF Max Fixed, 1 pF Max Switching)
- DSP/μP-Compatible Parallel Interface

applications

- Portable Digital Radios
- Personal Communication Assistants
- Cellular
- Pager
- Scanner
- Digitizers
- Process Controls
- Motor Control
- Remote Sensing
- Automotive
- Servo Controls
- Cameras

DW OR PW PACKAGE
(TOP VIEW)



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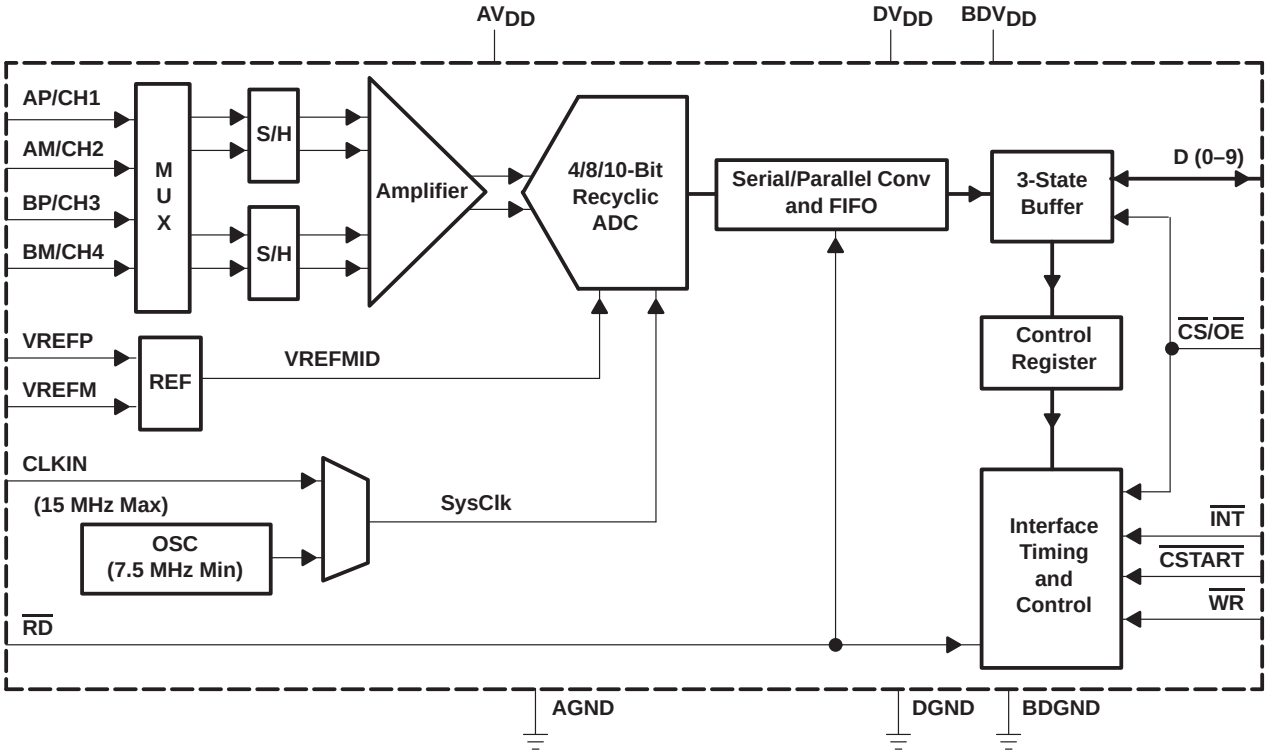
functional block diagram



description

The TLV1562 is a 10-bit CMOS low-power, high-speed programmable resolution analog-to-digital converter based on a low-power recyclic architecture. The unique architecture delivers a throughput up to 2 MSPS (million samples per second) at 10-bit resolution. The programmable resolution allows a higher conversion throughput as a tradeoff of lower resolution. A high speed 3-state parallel port directly interfaces to a digital signal processor (DSP) or microprocessor (μP) system data bus. D0 through D9 are the digital output terminals with D0 being the least significant bit (LSB). The TLV1562 is designed to operate for a wide range of supply voltages (2.7 V to 5.5 V) with very low power consumption (11 mA maximum at 5.5 V, 10 MHz CLKIN). The power saving feature is further enhanced with a software power-down feature (1 μA maximum) and auto power-down (1 μA maximum) feature.

Many programmable features make this device a flexible general-purpose data converter. The device can be configured as either four single-ended inputs to maximize the capacity or two differential inputs to improve noise immunity. The internal system clock (SYSCLK) may come from either an internally generated OSC or an external clock source (CLKIN). Four different modes of conversion are available for different applications. The interrupt driven modes are mostly suitable for asynchronous applications, while the continuous modes take advantage of the high speed nature of a pipelined architecture. A pair of built-in sample-and-hold amplifiers allow simultaneous sampling of two input channels. This makes the TLV1562 perfect for communication applications. Conversion is started by the $\overline{RD}$ signal, which can also be used for reading data, to maximize the throughput. Conversion can be started either by the $\overline{RD}$ or $\overline{CSTART}$ signal when the device is operating in the interrupt-driven modes. The dedicated conversion start pin, $\overline{CSTART}$, provides a mechanism to simultaneously sample and convert multiple channels when multiple converters are used in an application.

description (continued)

The converter incorporates a pair of differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. Other features such as low input capacitance (10 pF) and very wide input bandwidth (75 MHz) make this device a perfect digital signal processing (DSP) companion for mobile communication applications. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

The features that make this device truly a DSP friendly converter include: 1) programmable continuous conversion modes, 2) programmable 2s complement output code format, and 3) programmable resolution. The TLV1562 is offered in both 28-pin TSSOP and SOIC packages. The TLV1562C is characterized for operation from 0°C to 70°C. The TLV1562I is characterized for operation over the full industrial temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	
	28-TSSOP (25 MIL PITCH) (PW)	28-SOIC (50 MIL PITCH) (DW)
0°C to 70°C	TLV1562CPW	TLV1562CDW
–40°C to 85°C	TLV1562IPW	TLV1562IDW

Terminal Functions

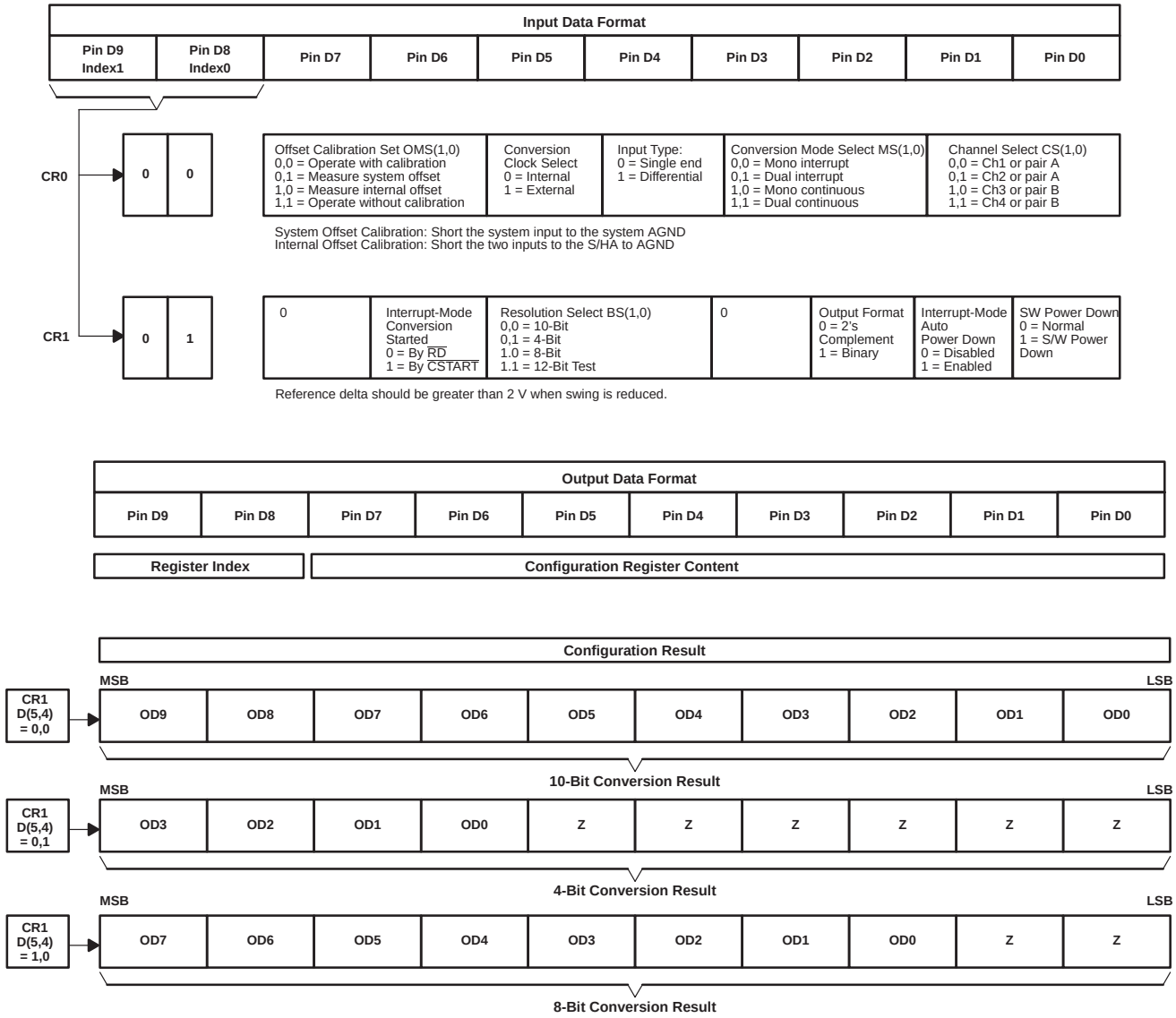
TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	20	I	Analog ground return for the internal circuitry. Unless otherwise noted, all analog voltage measurements are with respect to AGND.
AM/CH2	26	I	Differential channel A input minus or single-ended channel 2
AP/CH1	27	I	Differential channel A input plus or single-ended channel 1
AV_{DD}	23	I	Positive analog supply voltage
BDGND	8	I	Digital ground return for the I/O buffers. Unless otherwise noted, all digital interface voltage measurements are with respect to DGND.
BDV_{DD}	7	I	Positive digital supply voltage for I/O buffers
BM/CH4	24	I	Differential channel B input minus or single-ended channel 4
BP/CH3	25	I	Differential channel B input plus or single-ended channel 3
CLKIN	16	I	External clock input. (1 MHz to 15 MHz)
$\overline{CS}/\overline{OE}$	15	I	Chip select. A high-to-low transition on this input resets the internal counters and controls and enables the output data bus D(0–9) and control inputs ($\overline{RD}$, $\overline{WR}$) within a maximum setup time. A low-to-high transition disables the output data bus D(9–0) and $\overline{WR}$ within a maximum setup time. This signal also serves as an output enable signal when the device is programmed into both mono and dual interrupt-driven modes using $\overline{CSTART}$ as the start of conversion signal.
$\overline{CSTART}$	1	I	Conversion start signal. A falling edge starts the sampling period and a rising edge starts the conversion. This signal acts without $\overline{CS}$ activated. $\overline{CSTART}$ connects to DV_{DD} via a 10-kΩ pull-up resistor if not used.
D(0–4)	2–6	I/O	The lower bits of the 3-state parallel data bus. Bidirectional. The data bus is 3-stated except when $\overline{RD}$ or $\overline{WR}$ is low when $\overline{CS}$ is low.
D(5–9)	9–13	I/O	The higher bits of the 3-state parallel data bus. Bidirectional. The data bus is 3-stated except when $\overline{RD}$ or $\overline{WR}$ is low when $\overline{CS}$ is low. When the host processor writes to the converter, D(9,8) are used as an index to the internal registers.
DGND	18	I	Digital ground return for the internal digital logic circuitry
DV_{DD}	17	I	Positive digital supply voltage
$\overline{INT}$	14	O	Interrupt output. The falling edge of $\overline{INT}$ signals the end of conversion. This output goes from a high impedance state to low logic level on the fifth falling edge of the system clock and remains low until reset by the rising edge of $\overline{CS}$ or $\overline{RD}$. $\overline{INT}$ requires connection of a 10-kΩ pull-up resistor.
$\overline{RD}$	28	I	Processor read strobe or synchronous start of conversion/sampling. The falling edge of $\overline{RD}$ is used to 1) start the conversion in interrupt-driven mode (if $\overline{RD}$ is programmed as the start conversion signal); 2) start both conversion and next sampling plus release of the previous conversion data in both continuous modes. The rising edge of $\overline{RD}$ serves as a read strobe and data is 3-stated (approximately 10 ns at 50 pF bus loading) after this edge. Connection of a 10-kΩ pull-up resistor is optional.
VREFM	21	I	The lower voltage reference value is applied to this terminal.
VREFP	22	I	The upper reference voltage value is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the VREFM terminal.
$\overline{WR}$	19	I	Processor write strobe. Active low. Connection of a 10-kΩ pull-up resistor is optional.

detailed description

The TLV1562 analog-to-digital converter is based on an advanced low power recyclic architecture. Two bits of the conversion result are presented per system clock cycle. A total of 5 system clock (SYSCLK) cycles is required to complete the conversion. The serial conversion results are converted to a parallel word for output. The device supports both interrupt-driven (typically found in a SAR type ADC) and continuous (natural for a pipeline type ADC) modes of conversion. An innovative conversion scheme makes this device perfect for power sensitive applications with uncompromised speed.

control register

The TLV1562 is software configurable. The first two bits, MSBs (D9,8), are used to address the register set. The rest of the 8 bits are used as data. There are two control registers, CR0 and CR1, for user configuration. All of these register bits are written to the control register during a write cycle. A description of the control registers and the input/output data formats are shown in Figure 1.



NOTE: Z indicates bits write zero read zero back.

Figure 1. Input/Output Data Formats

NOTE:

Channel select bits CR0.(1,0), CS(1,0) are ignored when the device is in the dual (interrupt or continuous) modes using differential inputs, since both differential input pairs are automatically selected. CR0.0 (i.e., CS0 bit) is used to determine if channels 1 and 3 or channels 2 and 4 are selected if single-ended input mode is used.

detailed description (continued)

Table 1. Select Input Channels

CR0.4 (INPUT TYPE)	CR0.(3,2) (CONVERSION MODE SELECT)	CR0.(1,0) (CHANNEL SELECT)	CHANNEL(S) SELECTED	NOTE
0 (Single-ended)	00 or 10	0,0	CH1	Single channel
0 (Single-ended)	00 or 10	0,1	CH2	Single channel
0 (Single-ended)	00 or 10	1,0	CH3	Single channel
0 (Single-ended)	00 or 10	1,1	CH4	Single channel
1 (Differential)	00 or 10	0,X	Differential pair A	Single channel
1 (Differential)	00 or 10	1,X	Differential pair B	Single channel
0 (Single-ended)	01 or 11	X,0	Both CH1 and CH3	Dual channels
0 (Single-ended)	01 or 11	X,1	Both CH2 and CH4	Dual channels
0 (Single-ended)	01 or 11	X,0	Both CH1 and CH3	Dual channels
0 (Single-ended)	01 or 11	X,1	Both CH2 and CH4	Dual channels
1 (Differential)	01 or 11	X,X	Both differential pairs A and B	Dual channels

configure the device

The device can be configured by writing to control registers CR0 and CR1. A read register is carried out by auto-sequence when the device is put into the software power-down state. CR0 is read first and then CR1 at the next two $\overline{RD}$ rising edges after the device is in the software power-down state. The falling edge of $\overline{RD}$ has no meaning and does not trigger a conversion in the software power-down state.

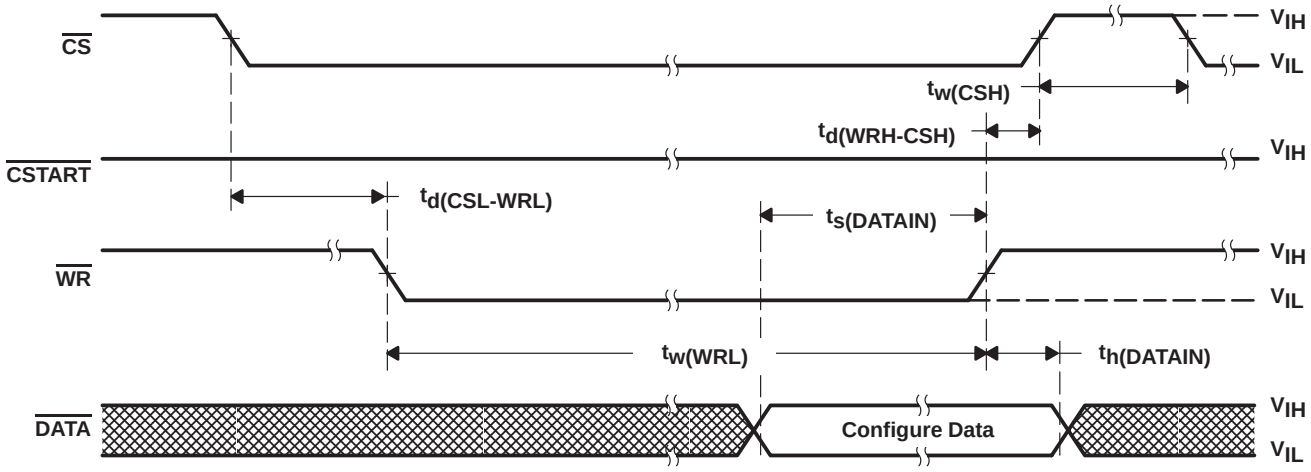


Figure 2. Configuration Cycle Timing

detailed description (continued)

The following examples show how to program configuration registers CR0 and CR1 for different settings.

Example 1:

REGISTER	INDEX										COMMENT
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
CR0	0	0	1	1	0	1	0	0	0	0	Mono interrupt mode, use $\overline{RD}$, write 0D0h to ADC
CR1	0	1	0	0	0	0	0	0	0	0	Use 2s complementary output, use $\overline{RD}$, write 104h to ADC

Example 2:

CR0	0	0	1	1	0	1	0	0	0	0	Mono interrupt mode, use $\overline{CSTART}$, write 0D0h to ADC
CR1	0	1	0	1	0	0	0	0	0	0	Use 2s complementary output, write 144h to ADC

Example 3:

CR0	0	0	1	1	0	1	0	1	0	0	Dual interrupt mode, use $\overline{CSTART}$ only, write 0D4h to ADC
CR1	0	1	0	1	0	0	0	0	0	0	Use 2s complementary output, write 144h to ADC

Example 4:

CR0	0	0	1	1	0	1	1	0	0	0	Mono continuous mode, use $\overline{RD}$ only, write 0D8h to ADC
CR1	0	1	0	0	0	0	0	0	0	0	Use 2s complementary output, write 104h to ADC

Example 5:

CRO	0	0	1	1	0	1	1	1	0	0	Dual continuous mode, use $\overline{RD}$ only, write 0DCh to ADC
CR1	0	1	0	0	0	0	0	1	0	0	Binary output, write 104h to ADC

analog input

input types

The four analog inputs can be configured as two pairs of differential inputs or four single-ended inputs by setting the control register 0 bit 4 input type selection (dual or single channel).

differential input (CR0.4=1)

Up to two channels are available when the TLV1562 is programmed for differential input. The output data format is bipolar when the device is operated in differential input mode.

single-ended input (CR0.4=0)

Up to four channels are available when the TLV1562 is programmed for single-ended input. The output data format is unipolar when the device is operated in single-ended input mode.

detailed description (continued)

input signal range

The analog input signal range for a specific supply voltage AV_{DD} ranges from (AV_{DD} – 1.9 V) to 0.8 V.

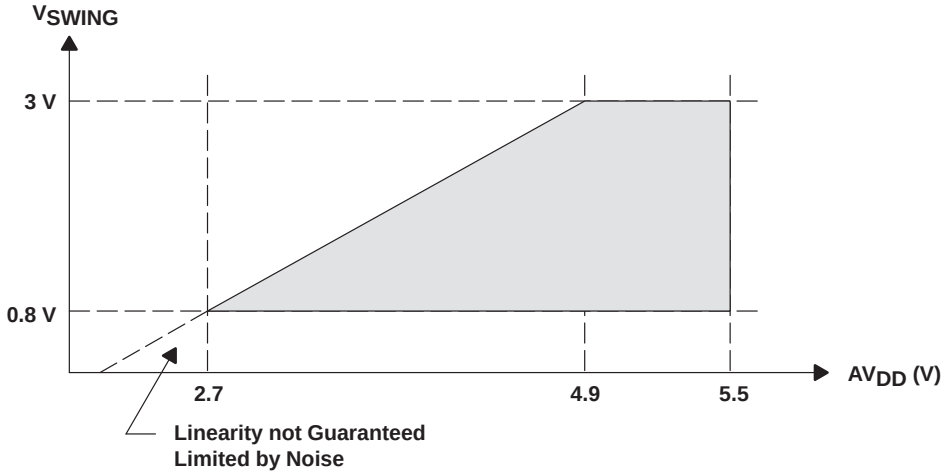


Figure 3. Analog Input Range vs AV_{DD}

$VREFCM + 0.5 \times V_{SWING} \leq AV_{DD} - 1\ V$
$VREFCM - 0.5 \times V_{SWING} \geq 0.8\ V$

Where:

VREFCM = (VREFP + VREFM)/2 is the common mode reference voltage.
V_{SWING} = dynamic range of the input signal,
V_{SWING} = VINP – VINM,
And the common mode input voltage is:
VINCM = (VINP + VINM)/2,

MAX V_{SWING} = MIN [(AV_{DD} – 1.9 V), 3 V]

For single-ended input, the analog input range is between VREFP and VREFM. So the range of single-ended VIN is:

3 V	if AV_{DD} = 3 V
1 V	if AV_{DD} = 3 V
0.8 V	if AV_{DD} = 2.7 V

For differential input, the input common mode voltage VINCM can be between AV_{DD} and AGND as long as 3 V ≥ (VINP–VINM) ≥ 0.8 V.
This means VINCM ≥ 0.4 V.

So the range of differential analog input voltage, (VINP–VINM) is:

3 V	if AV_{DD} = 3 V
1 V	if AV_{DD} = 3 V
0.8 V	if AV_{DD} = 2.7 V

detailed description (continued)

equivalent input impedance

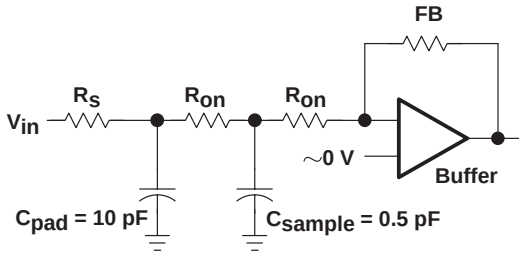


Figure 4. Equivalent Input Circuit

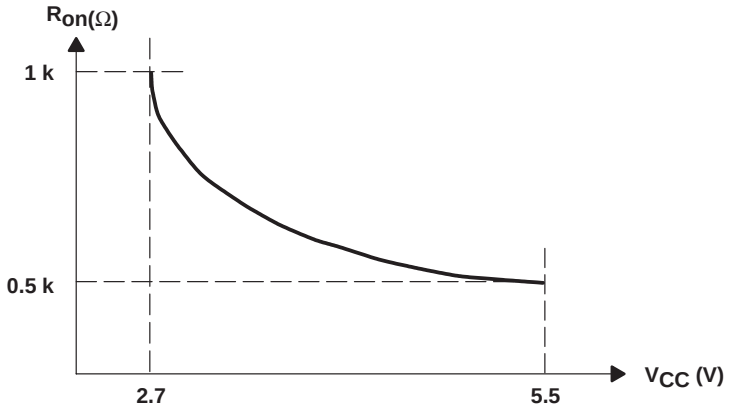


Figure 5. Input Mux On Resistance vs Analog Supply Voltage

Req = Vin/Ieq = (Q/Cin)/(Q/T) = T/Cin = 1/(fs × Csample) = 1/(2 MHz × 0.5 pF) = 1 MΩ

Where f_S is the sampling frequency, and f_c is the conversion frequency

$f_S = f_c/5$ when the device is in one channel/continuous conversion mode,

$f_S = f_c/10$ when the device is in one channel/continuous conversion mode,

f_S = Conversion trigger strobe frequency when the device is in interrupt mode ($\overline{RD}$ or $\overline{CSTART}$)

Csample = Input capacitance = 0.5 pF

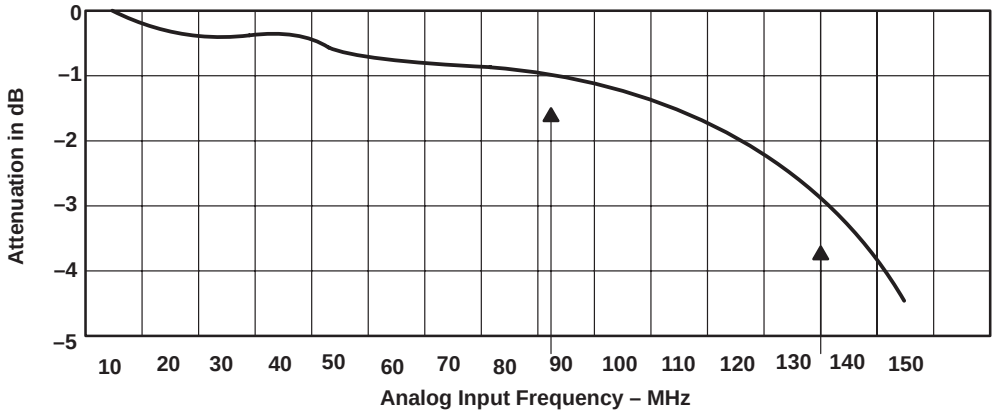
Cparasitic = Parasitic capacitance = 0.5 pF

Cpad = Input PAD capacitance = 10 pF

Ron = Mux switch on series resistance = 1 kΩ at 2.7 V

Rs = Source output resistance = 1 kΩ

input bandwidth (full power 0 dB input, BW at –1 dB)

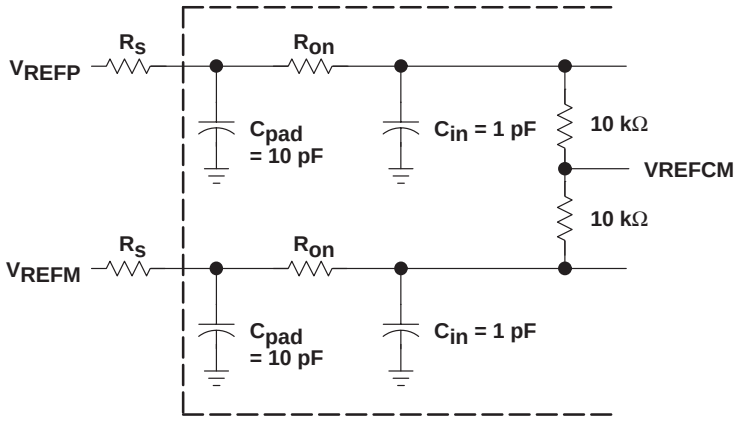


BW = 1/[2 × π × (Rtotal y Cac)]
= 1/[2 × π × ((Ron + Rs) × (Csample + Cparasitic))]
= 1/[2 × π × (2K × 1 pF)]
= 79.6 MHz (Theoretical Max)

Figure 6. Typical Analog Input Frequency Input Bandwidth

reference voltage inputs

The TLV1562 has two reference input pins: REFP and REFM. The voltage levels applied to these pins establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively. The values of VREFP, VREFM, and the analog input should not exceed the positive supply or be less than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than VREFP and is at zero when the input signal is equal to or lower than VREFM. The internal resistance from VREFP to VREFM may be as low as 20 kΩ (±10%).



The reference voltages must satisfy the following conditions:
$VREFP \leq AV_{DD} - 1$ V,
AGND + 0.9 V < VREFM and
3 V ≥ (VREFP – VREFM) ≥ 0.8 V

Figure 7. Equivalent Circuit for Reference input

sampling/conversion

All of the sampling, conversion, and data output in the device are started by a trigger. This trigger can be the $\overline{RD}$ or $\overline{CSTART}$ signal depending on the mode of conversion and configuration. The falling edge of the $\overline{RD}$ signal and the rising edge of the $\overline{CSTART}$ signal are extremely important since they are used to start the conversion. These edges need to stay as close to the falling edges of the external clock, if they are used as SYSCLK. The minimum setup time with respect to the rising edge of the external SYSCLK should be 5 ns minimum. When the internal SYSCLK is used, this is not an issue, since these two edges start the internal clock automatically; therefore, the setup time is always met.

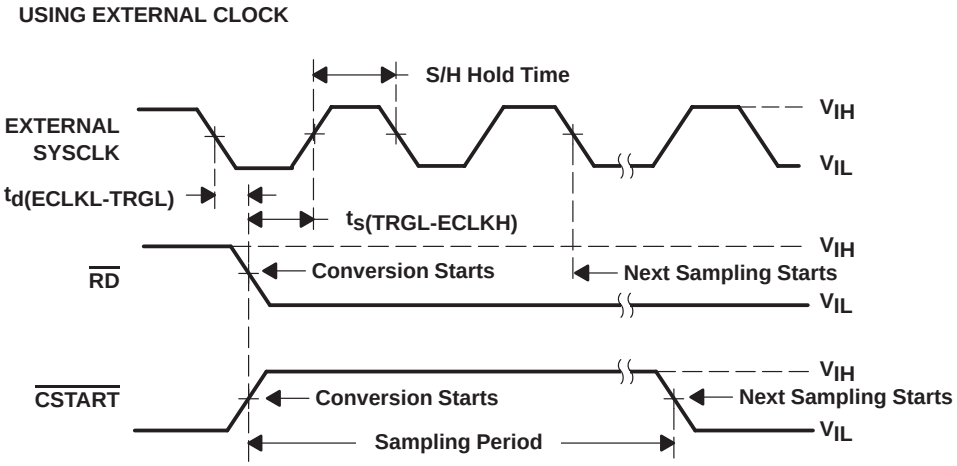


Figure 8. Conversion Trigger Timing – External Clock

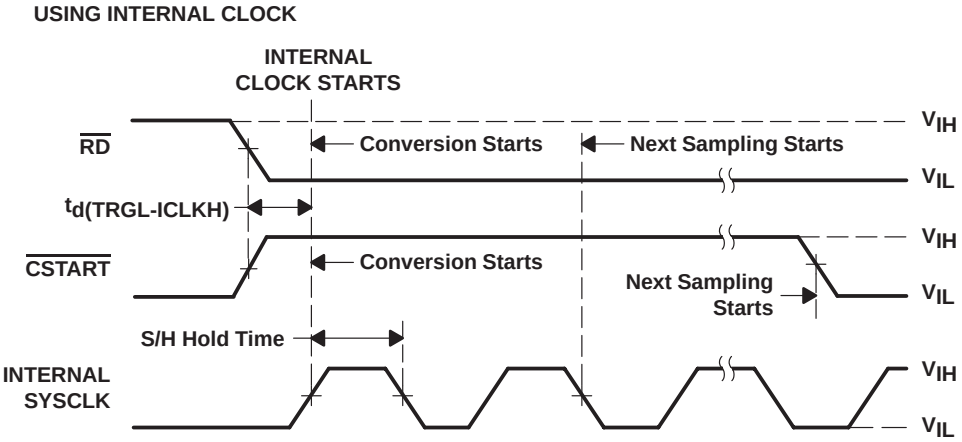


Figure 9. Conversion Trigger Timing – Internal Clock

Table 2. Conversion Trigger Edge

CONVERSION MODE	CONVERSION TRIGGER	START OF SAMPLING	START OF CONVERSION	CONVERSION TIME (INTERNAL CLK)	CONVERSION TIME (EXTERNAL CLK)	INTERRUPT CANCELED BY	DATA OUT
Mono Interrupt	$\overline{RD}$	$\overline{WR}$ ↑‡ or 2 SYSCLK from $\overline{RD}$ ↓	$\overline{RD}$ ↓	6 SYSCLK	5 SYSCLK	$\overline{RD}$ ↑	41 ns§ from $\overline{INT}$ low
	$\overline{CSTART}$†	$\overline{CSTART}$ ↓	$\overline{CSTART}$ ↑	6 SYSCLK	5 SYSCLK	$\overline{RD}$ ↓	41 ns§ from $\overline{RD}$ low
Dual Interrupt	$\overline{CSTART}$	$\overline{CSTART}$ ↓	$\overline{CSTART}$ ↑	12 SYSCLK	10 SYSCLK	First $\overline{RD}$ ↓	41 ns§ from $\overline{RD}$ low
Mono Continuous	$\overline{RD}$	$\overline{WR}$ ↑‡ or 2 SYSCLK from $\overline{RD}$ ↓	$\overline{RD}$ ↓	6 SYSCLK	5 SYSCLK	N/A	41 ns§ from $\overline{RD}$ low
Dual Continuous	$\overline{RD}$	$\overline{WR}$ ↑‡ or 7 SYSCLK from $\overline{RD}$ ↓	$\overline{RD}$ ↓	12 SYSCLK	10 SYSCLK	N/A	41 ns§ from $\overline{RD}$ low

† $\overline{CSTART}$ works with or without $\overline{CS}$ active.

‡ The first sampling period starts at the last $\overline{RD}$ low of the previous cycle or $\overline{WR}$ high of the configuration cycle. $\overline{RD}$ low is the falling edge of $\overline{RD}$ and $\overline{WR}$ high is the rising edge of the $\overline{WR}$ signal. (Minimum sample/hold amp settling time = one SYSCLK, approximately 100 ns min, at Rs ≤ 1 kΩ).

§ Output data enable time is dependent on bus loading and supply voltage (BDV_{DD}). For BDV_{DD} = 5 V, the enable time is 19 ns at 25 pF, 23 ns at 50 pF, and 25 ns at 100 pF. For BDV_{DD} = 2.7 V, the enable time is 37 ns at 25 pF, 41 ns at 50 pF, and 56 ns at 100 pF.

The TLV1562 provides four types of conversion modes. The two interrupt-driven conversion modes are asynchronous and are simple one-shot conversions. The auto-powerdown conversion feature can be enabled when interrupt-driven conversion modes are used. The other two continuous conversion modes are synchronous with the $\overline{RD}$ signal (as a clock) from the processor and are more suitable for repetitive signal measurement. These different modes of conversion offer a tradeoff between simplicity and speed.

detailed description (continued)

Table 3. Maximum Conversion Speed (for 1 LSB INL and DNL at 10 bit)

CONVERSION MODE		CR0.(3,2)	MAXIMUM CONVERSION THROUGHPUT†	
			EXTERNAL CLOCK (10 MHz)	INTERNAL CLOCK (8 MHz)
Mono interrupt-driven conversion mode	$\overline{RD}$	00	1.5 MSPS	1.1 MSPS
	$\overline{RD}$ with auto power down		0.82 MSPS	0.68 MSPS
	$\overline{CSTART}$		1.5 MSPS	1.1 MSPS
	$\overline{CSTART}$ with auto power down		0.82 MSPS	0.68 MSPS
Dual interrupt-driven conversion mode‡	$\overline{CSTART}$	01	1.5 MSPS	0.91 MSPS
	$\overline{CSTART}$ with auto power down		1.05 MSPS	0.83 MSPS
Mono continuous conversion mode	$\overline{RD}$	10	2 MSPS§	1.33 MSPS§
Dual continuous conversion mode	$\overline{RD}$	11	2 MSPS¶	1.33 MSPS¶

† Speed is calculated for 5-V with a 2-V reference
(5.5 V to 3 V, I-temperature and C-temperature: 2 MSPS at 10 bit, 3 MSPS at 8 bit, 7 MSPS at 4 bit;
3 V to 2.7 V, C-temperature: 2 MSPS at 10 bit, 2.5 MSPS at 8 bit, 7 MSPS at 4 bit;
3 V to 2.7 V, I-temperature: 1.6 MSPS at 10 bit, 2.5 MSPS at 8 bit, 7 MSPS at 4 bit).
Higher throughput is possible when the linearity requirement is relaxed.
‡ Dual interrupt mode is available to 8-bit or 10-bit resolution and single-ended input type.
§ Throughput from single selected channel.
¶ Combined throughputs from a pair of selected channels.

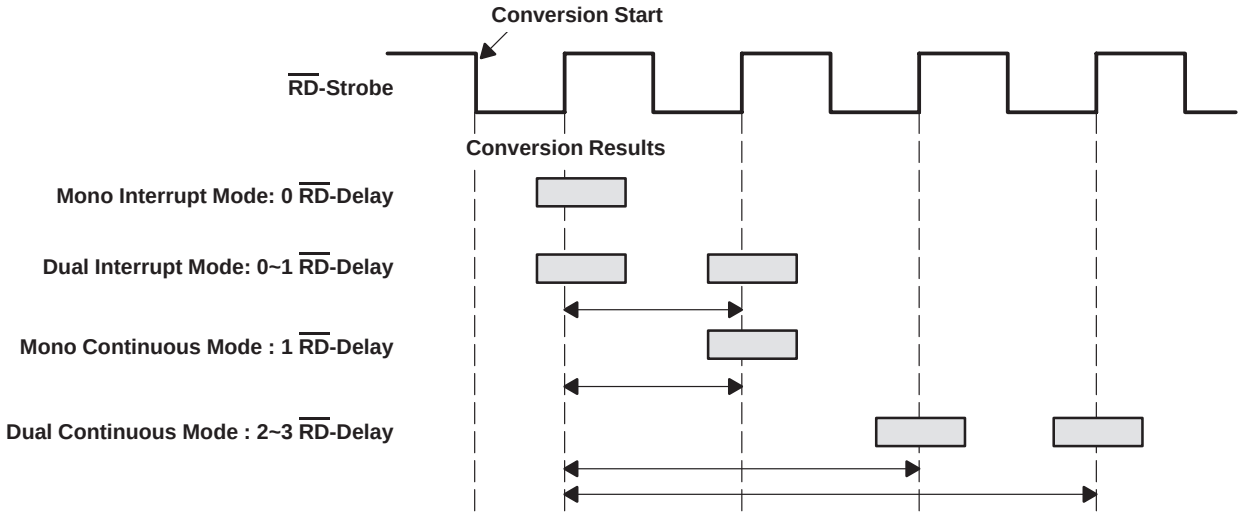


Figure 10. Digital Delays for Different Conversion Modes

mono interrupt-driven mode (CR0.(3,2) = 0,0)

The mono interrupt-driven conversion mode provides a one-shot conversion. Sampling, conversion, and data output are all performed in a single cycle. The analog signal is sampled 2 SYSCLKs after the falling edge of $\overline{RD}$ (or the rising edge of $\overline{WR}$ if this is the first sample after configuration) and then converted on the falling edge of $\overline{RD}$. Once the data is ready, $\overline{INT}$ falls and the data is output to the bus. The rising edge of $\overline{RD}$ cancels $\overline{INT}$ and initiates a read of the data. The data bus is 3-stated when $\overline{RD}$ goes high. It is not necessary to configure the converter for each cycle or toggle $\overline{CS}$ between cycles.

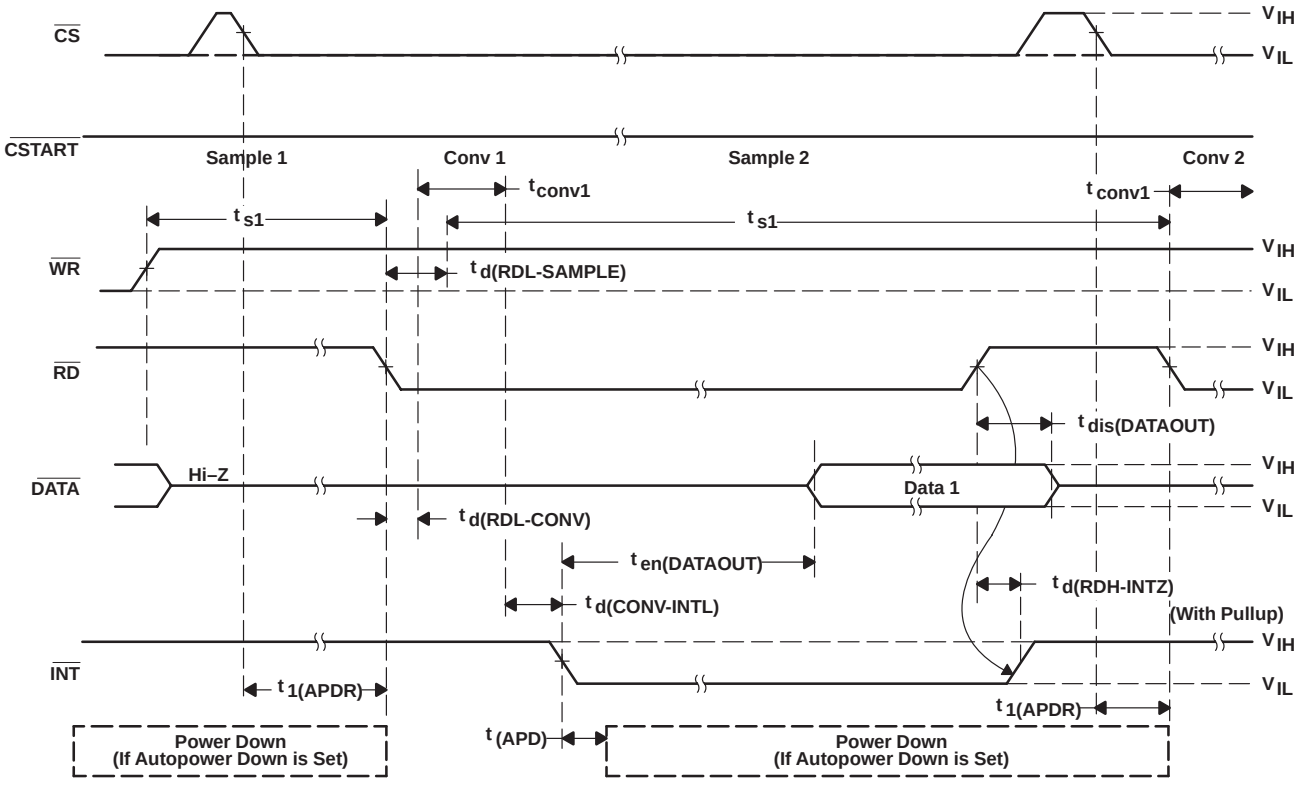


Figure 11. Mono Interrupt-Driven Mode Using $\overline{RD}$

Conversion can also be started with $\overline{\text{CSTART}}$. This is useful when an application requires multiple TLV1562s for simultaneous samplings and conversions. The falling edge of $\overline{\text{CSTART}}$ starts the sampling and the rising edge of $\overline{\text{CSTART}}$ starts the conversion. Once the data is ready $\overline{\text{INT}}$ falls. $\overline{\text{INT}}$ is terminated by the following falling edge of $\overline{\text{RD}}$ which also outputs the data to the bus. On the rising edge of $\overline{\text{RD}}$, the data is read and the data bus is 3-stated.

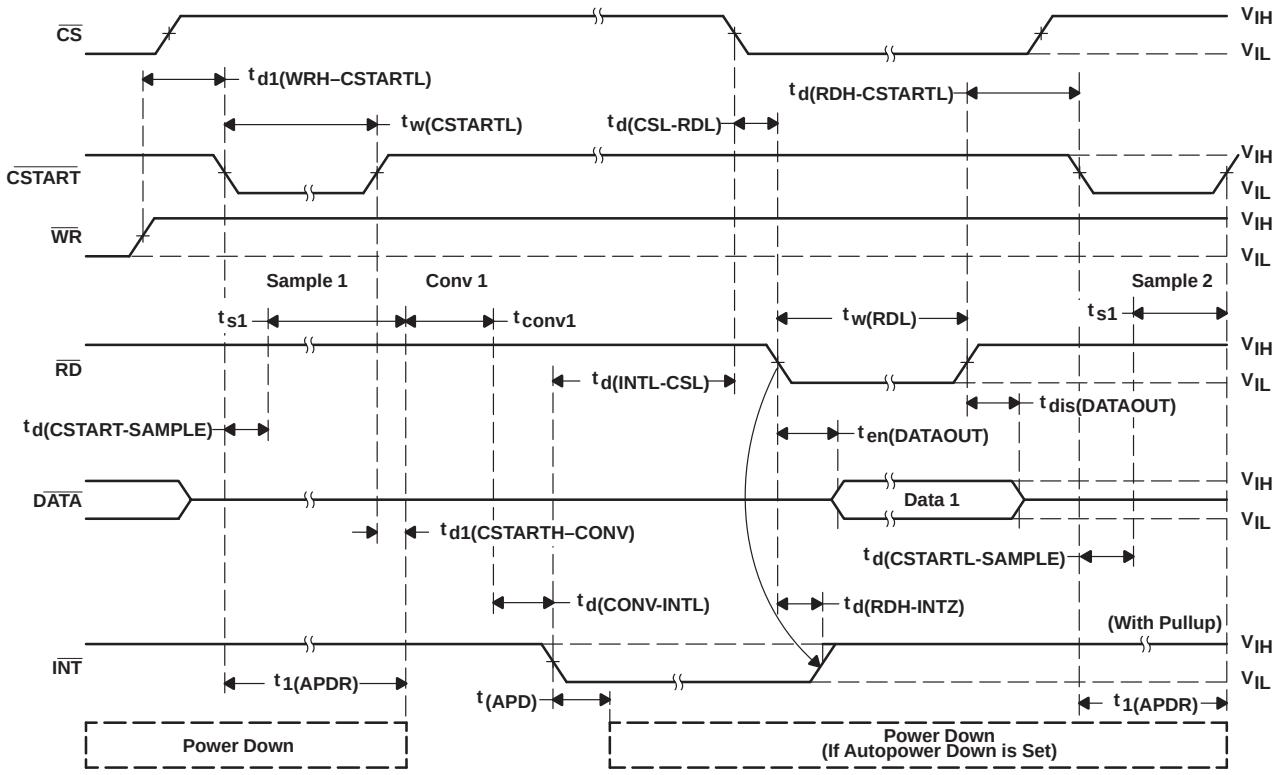


Figure 12. Mono Interrupt-Driven Mode Using $\overline{\text{CSTART}}$

dual interrupt-driven mode (CR0.(3,2) = 0,1)

The dual interrupt-driven conversion mode provides a similar one-shot conversion, sampling, and conversion but also samples both selected channels simultaneously. Conversion can only be started with the $\overline{\text{CSTART}}$ signal. The falling edge of $\overline{\text{CSTART}}$ starts the sampling of both of the input channels selected, and the rising edge of $\overline{\text{CSTART}}$ starts the conversion. Since it takes two consecutive conversions internally, the conversion time required is doubled (10 SYSCLK cycles). Once the data are ready, $\overline{\text{INT}}$ falls. $\overline{\text{INT}}$ is terminated by the first falling edge of $\overline{\text{RD}}$, which also outputs the first data to the bus. On the rising edge of $\overline{\text{RD}}$, data is read and the data bus is 3-stated. The second $\overline{\text{RD}}$ falling edge outputs the second data to the bus and then reads it on the rising edge and 3-states the bus. It is not necessary to configure the converter for each cycle or toggle $\overline{\text{CS}}$ between cycles.

NOTE: Dual interrupt mode is available to 10-bit or 8-bit resolution and single-ended input type.

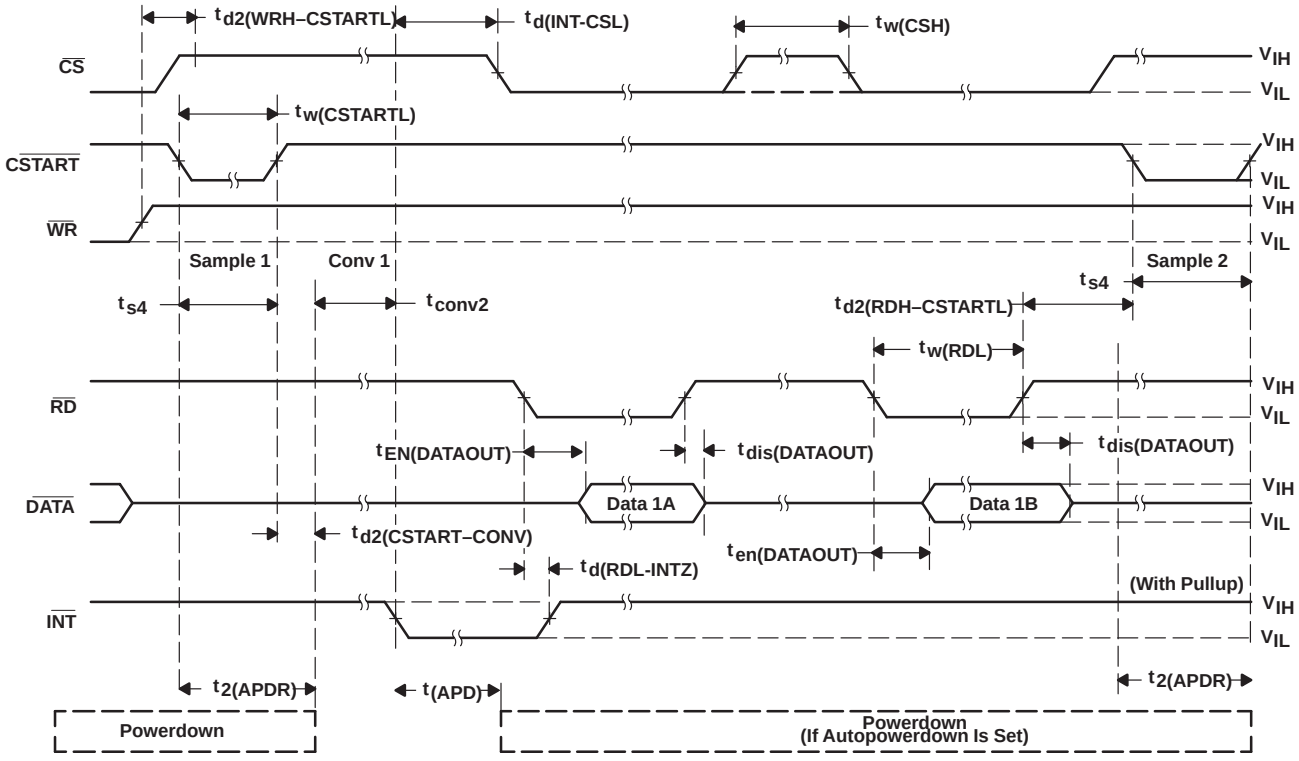


Figure 13. Dual Interrupt Conversion Mode
(Conversion can only be started with $\overline{\text{CSTART}}$ for the dual interrupt mode)

mono continuous mode (CR0.(3,2) = 1,0)

The mono continuous mode of conversion is synchronous with the $\overline{RD}$ signal. Its cycle time is approximately 5 SYSCLK cycles when an external SYSCLK is used (6 SYSCLK cycles when an internal SYSCLK is used). In the mono continuous mode, the TLV1562 is always sampling the input regardless of the state of other control signals when it is not in the hold state (the first half SYSCLK cycle after each falling edge of $\overline{RD}$). This simplifies control of the ADC. There is no need to generate any special signal to start the sampling.

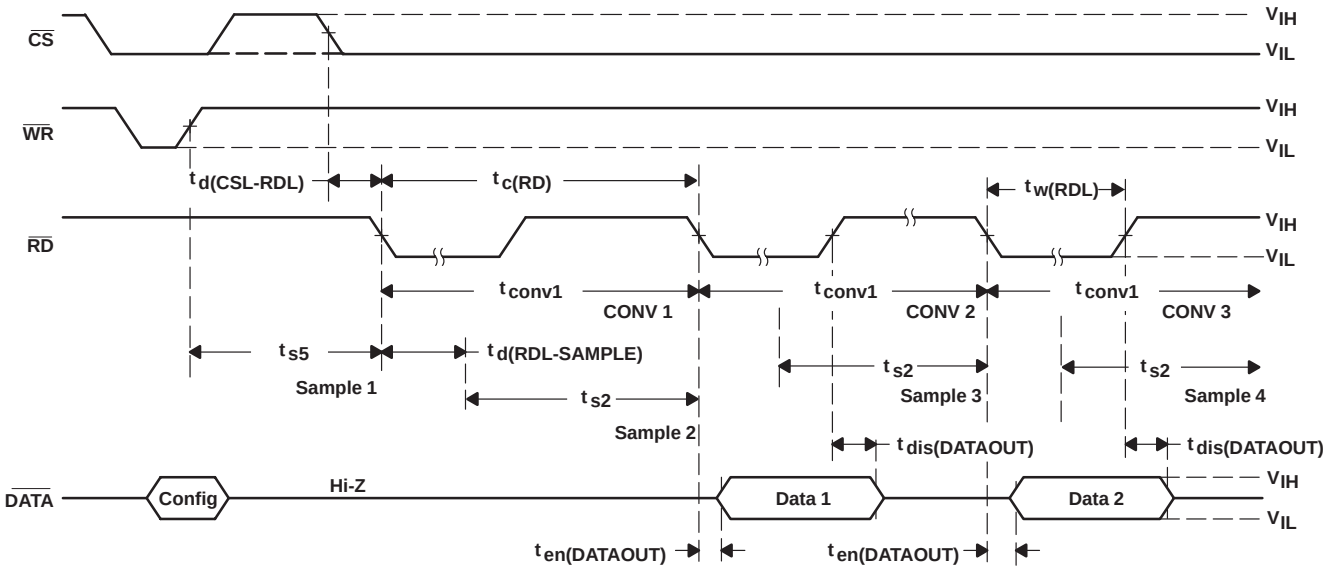


Figure 14. Mono Continuous Mode

dual continuous mode (CR0.(3,2) = 1,1)

When the TLV1562 operates in the dual continuous mode, it samples and then holds two preselected channels (differential or single ended) simultaneously as $\overline{RD}$ clocks. These samples are then converted in sequence. This is designed to optimize the DSP MIPS for communication applications. Its cycle time is approximately 10 SYSCLK cycles when an external SYSCLK is used (12 SYSCLK cycles when an internal SYSCLK is used). When operating in the dual continuous mode, the TLV1562 is always sampling the input regardless of the state of the other control signals when it is not in the hold state. This simplifies control of the ADC. There is no need to generate any special signal to start the sampling. The TLV1562 goes into hold mode on the odd number (starting from the rising edge of $\overline{WR}$) falling edge of $\overline{RD}$ for one SYSCLK clock cycle.

A two-depth FIFO is used (only in the dual continuous mode) to ensure the output correlation. Thus on every alternate $\overline{RD}$ edge, the result of the previous two conversions is read out. This allows a slower $\overline{RD}$ clock frequency (slower than 1/5 of the SYSCLK frequency). Each dual continuous mode cycle (while $\overline{CS}$ remains active low) must have an even number of $\overline{RD}$ cycles to ensure the FIFO operates properly.

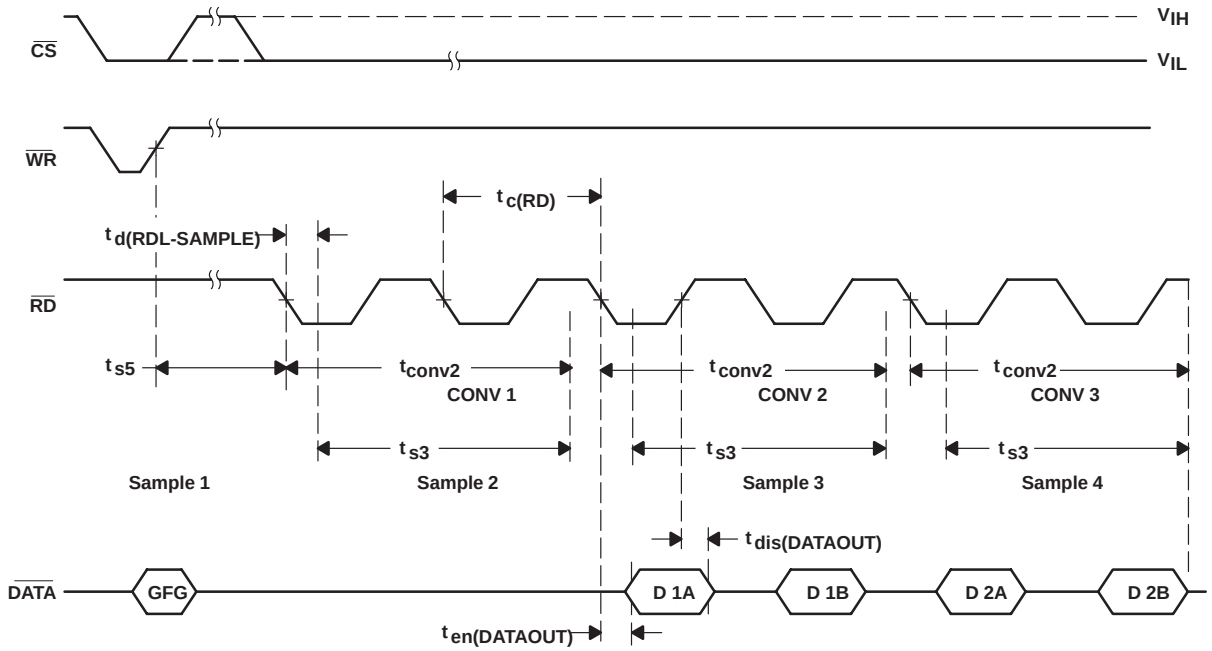


Figure 15. Dual Continuous Mode

system clock source

The TLV1562 uses multiple clocks for different internal tasks. SYSCLK is used for most conversion subtasks. The source of SYSCLK is programmable via control register 0, bit 5 (CR0.5). The source of SYSCLK is changed at the rising edge of $\overline{WR}$ of the cycle when CR0.5 is programmed.

internal oscillator (CR0.5 = 0, SYSCLK = internal OSC)

The TLV1562 has a built-in 8-MHz oscillator. When the internal OSC is selected as the source of SYSCLK, the internal clock starts with a delay (one half of the OSC clock period max) after the falling edge of the conversion trigger ($\overline{RD}$ or $\overline{CSTART}$).

external clock input (CR0.5 = 1, SYSCLK = External Clk)

The TLV1562 is designed to operate with an external clock input (CMOS/TTL) with a frequency from 100 kHz to 14 MHz. When an external clock is used as the source of SYSCLK, the setup time from the falling edge of $\overline{RD}$ to the rising edge of SYSCLK, $t_{s(TRGL-ECLKH)}$ is 5 ns minimum. The internal OSC is shut down when the external clock mode is selected.

host processor interface

parallel processor interface

The TLV1562 provides a generic high-speed parallel interface that is compatible with high-performance DSPs and general-purpose microprocessors. These include D(0,9), $\overline{RD}$, $\overline{WR}$, and $\overline{INT}$. $\overline{RD}$ transitions from high to low to signal the end of acquisition. The parallel I/O has its own power supply to minimize digital noise.

output data format

The output data format is unipolar binary (1023 to 0) when the device is operated in the single-ended input mode and is bipolar (511 to –512) when the device is operated in differential input mode. The output code format can be either binary or 2s compliment. The output data format is controlled by CR1.2.

power down

The device offers two different power-down modes: Auto power-down mode for interrupt-driven conversions and software power-down mode for all conversion modes. All configuration information is kept intact when the device is in software or auto power-down mode.

auto-power down for interrupt-driven conversion modes

When auto-power down is enabled, the device turns off the analog section (the converter except for the reference network) at the falling edge of $\overline{INT}$ and resumes after the falling edge of $\overline{CS}$ (if $\overline{RD}$ is the conversion trigger) or $\overline{CSTART}$ (if $\overline{CSTART}$ is the conversion trigger). The reference current and I/O are kept alive to ensure a fast recovery. Average power consumption can be reduced by accessing the converter less often. Special requirements for using this feature are:

- It is necessary to toggle $\overline{CS}$ between cycles so the converter knows when to resume.
- There is an additional delay to a conversion after the device is accessed due to the auto-power-down control. Therefore, the time between $\overline{RD}$ (or $\overline{CSTART}$) triggers is longer (longer $\overline{RD}$ or $\overline{CSTART}$ high time).

software power down (CR.10 = 1, software power down enabled)

In addition to the auto-power-down feature, the device has a software powerdown feature to further reduce power consumption when the device is idle. Writing a 1 to control register bit CR1.0 puts the TLV1562 into software power-down mode in 200 ns after $\overline{CS}$ is up. The device consumes less than 1 μA when in the power-down mode. Writing a 0 to control register bit CR1.0 wakes up the device. Conversion can start 1 μs after the device is resumed. $\overline{CS}$ must be high when the device is in power-down mode. Software power-down operation is slower than auto-power down but is more flexible and consumes almost no power.

Table 4. TLV1562 Powerdown Features

FUNCTION BLOCK/POWERDOWN MODE	SOFTWARE POWERDOWN		AUTO POWERDOWN	
DIGITAL CONTROL VOLTAGE LEVEL	CMOS	TTL	CMOS	TTL
Converter analog section	Inactive	Inactive	Inactive	Inactive
Reference current (amps)	Inactive	Inactive	Active	Active
Digital I/O buffers	Active	active	Active	Active
Estimated supply current, I_{CC}	1 μA	80 μA	120 μA	200 μA
Power-down time	200 ns	200 ns	200 ns	200 ns
Resume time	1 μs	1 μs	700 ns	700 ns
Maximum throughput†	1.2/0.7 MSPS‡	1.2/0.7 MSPS‡	1 MSPS	1 MSPS

† Dual interrupt, 10-bit, 5-V AV_{DD}, 10-MHz external clock, and 2 V (REFP–REFM).

‡ This assumes the TLV1562 is software powered down between every cycle. In reality this is not the case since auto-power down makes much more sense in this case. So the realistic maximum throughput for software power down will be close to the maximum throughput without powerdown which is 1.2 MSPS for dual-interrupt mode (and 1.5 MSPS if mono-interrupt mode is used). But this really depends on how long the device is powered down.

mid-scale error calibration

The device has a ±5% maximum full-scale error, mid-scale error, and zero-scale error due to the gain error in the sample and hold amplifier.

The TLV1562 is capable of calibrating the mid-scale error. There are two calibration modes: system mid-scale error calibration and internal mid-scale error calibration as described below.

NOTE:
Set register CR0.(7,6) = 1,1 when the device is not in mid-scale error calibration mode.

These mid-scale error calibrations affect the ADCs transfer characteristics as shown in Figure 16. The absolute error at code 512 is zero-out (this is the reference point for mid-scale error calibration). The calibration also makes the FS error and ZS error equal.

internal mid-scale error calibration (CR0.(7,6) = 1,0)

The internal mid-scale error calibration mode is set by writing to the configuration registers with CR0.(7,6) set to 10. The ADC analog inputs are internally shorted to mid-voltage (REFP+REFM)/2 when the mid-scale error calibration mode is enabled. One conversion (initiated by the falling edge of $\overline{RD}$) is performed to calculate the offset. The result of this conversion is stored in the mid-scale error register and is subtracted from all subsequent conversions thus removing any offset. Internal calibration removes any offsets internal to the device. Internal mid-scale error calibration reduces the mid-scale error to ±2.5% FS single ended inputs (0.3% FS differential inputs).

system mid-scale error calibration (CR0.(7,6) = 0,1)

System mid-scale error calibration is set by writing to the configuration registers with CR0.(7,6) set to 01. The analog input to be calibrated is externally connected to the voltage corresponding to mid-code. For differential operation, this is achieved by shorting the two inputs together; for a single-ended input this is achieved by connecting the analog input to the system mid-voltage, (SYSTEM_REFP + SYSTEM_REFM)/2. One conversion (initiated by $\overline{RD}$ falling edge) is performed to calculate the offset. The result of this conversion is stored in the mid-scale error register and is subtracted from all subsequent conversions thus removing any offset. System mid-scale error calibration removes the offset of not only the ADC but any offsets in the entire analog circuitry driving the ADC input. System mid-scale error calibration reduces the mid-scale error to ±0.4% FS single ended inputs (0.25% FS differential inputs).

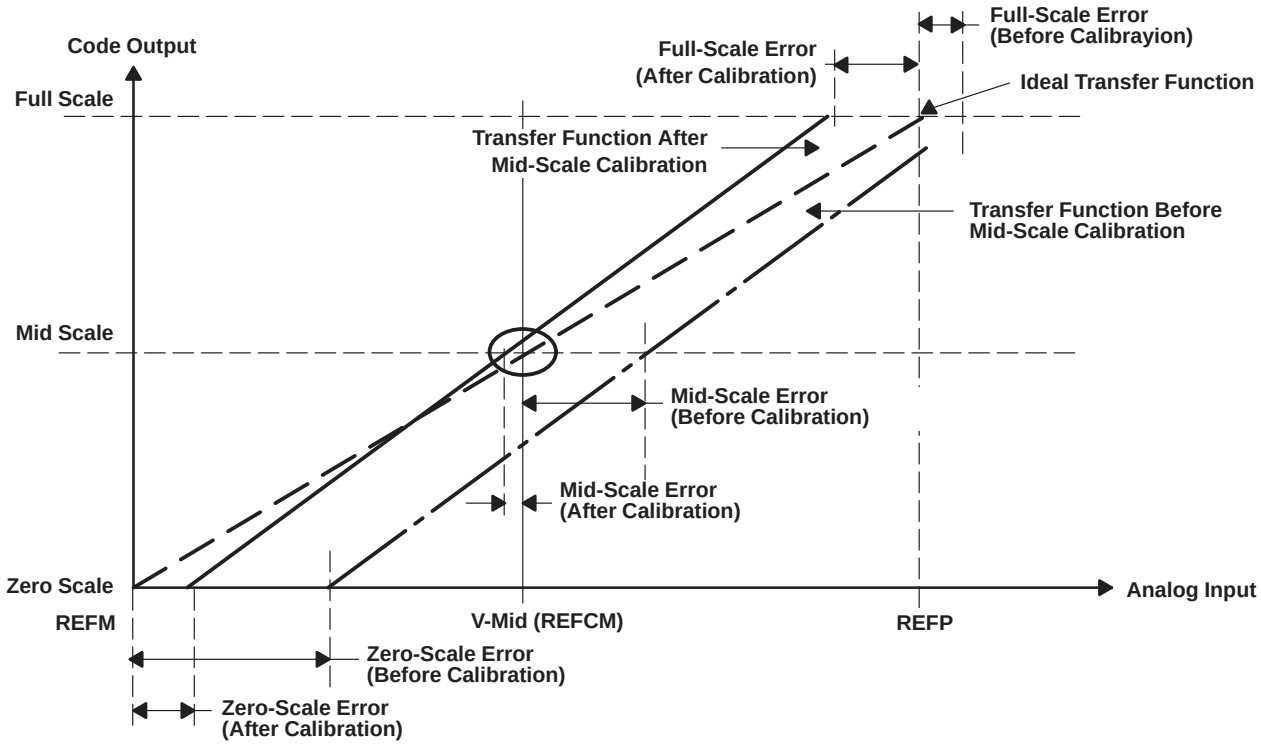


Figure 16. Mid-Scale Error Calibration

resume normal conversion from mid-scale error calibration modes

A follow on write operation sets CR0.(7,6) to 00 which resumes the normal conversion mode. Typically mid-scale error calibration needs to be performed only once after power up. If however the operation mode is changed from single ended to differential, then preferably mid-scale error calibration should be performed again.

The user writes a bit to enable mid-scale error calibration. Inputs to the ADC are internally shorted therefore the offset value can be converted to a digital word. The result (a digital word representing the offset) is stored in a latch. This offset value is then subtracted from the digital output of all conversions except when in mid-scale error calibration mode.

system design consideration regarding to mid-scale error calibration

Mid-scale error calibration may limit the dynamic range of the ADC. If the offset is negative and has a magnitude x, then the range of the converter codes is x to 1023. If the offset is positive and has a magnitude of x, then the range of converter codes is 1 to 1023 –x. Thus the ADCs dynamic range is reduced by x (say x = 20 codes) on either side of the range effectively with mid-scale error calibration. However this should not be a limitation for most users.

APPLICATION INFORMATION

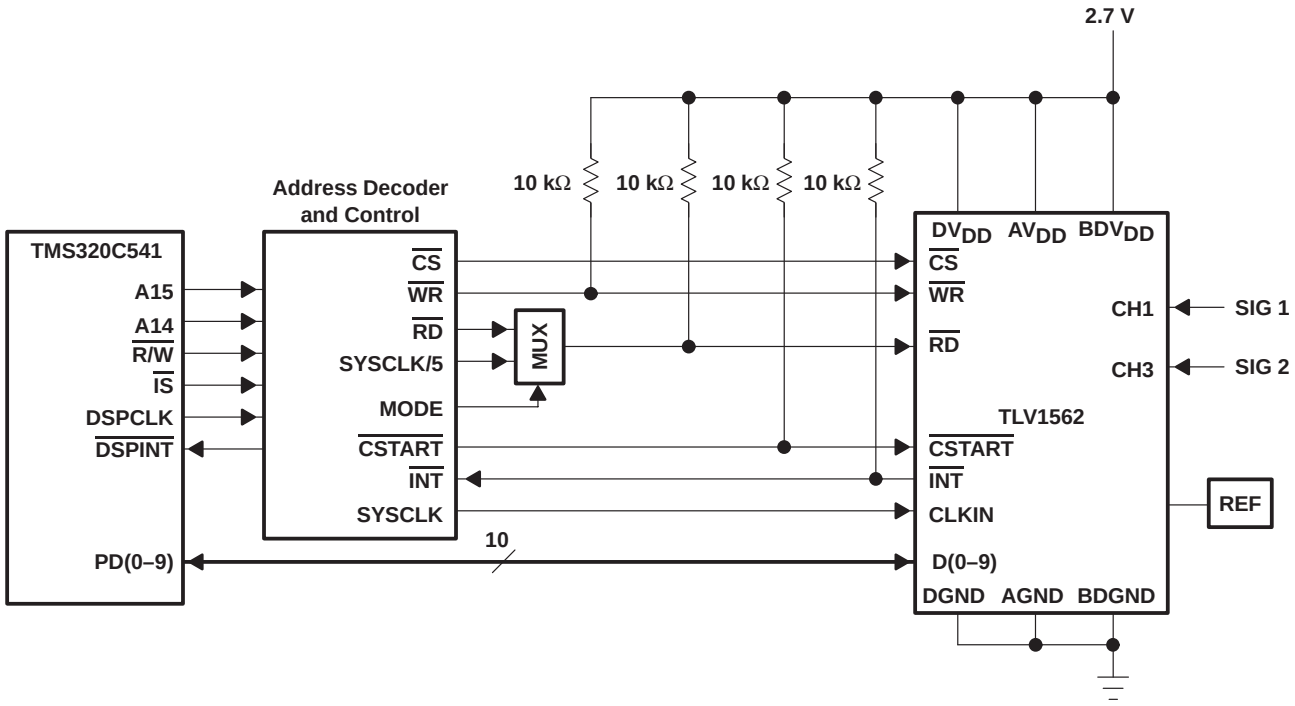


Figure 17. Typical Interface to a TMS320 DSP

APPLICATION INFORMATION

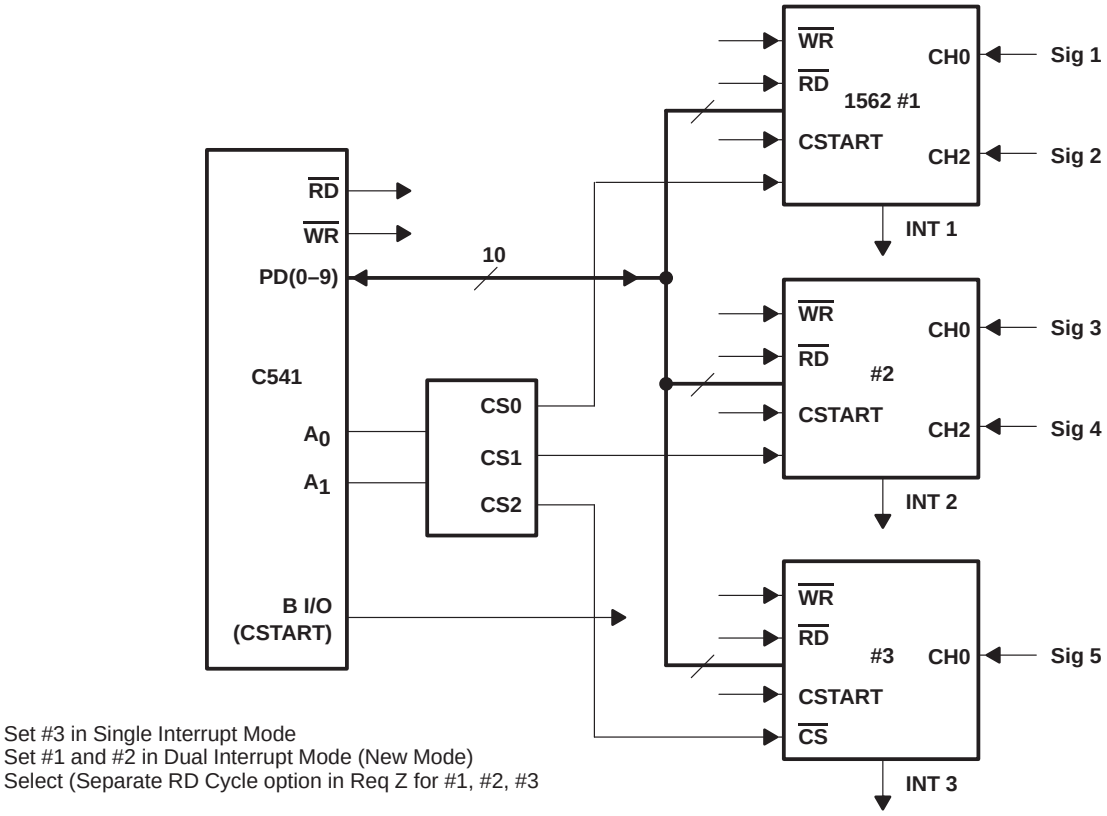
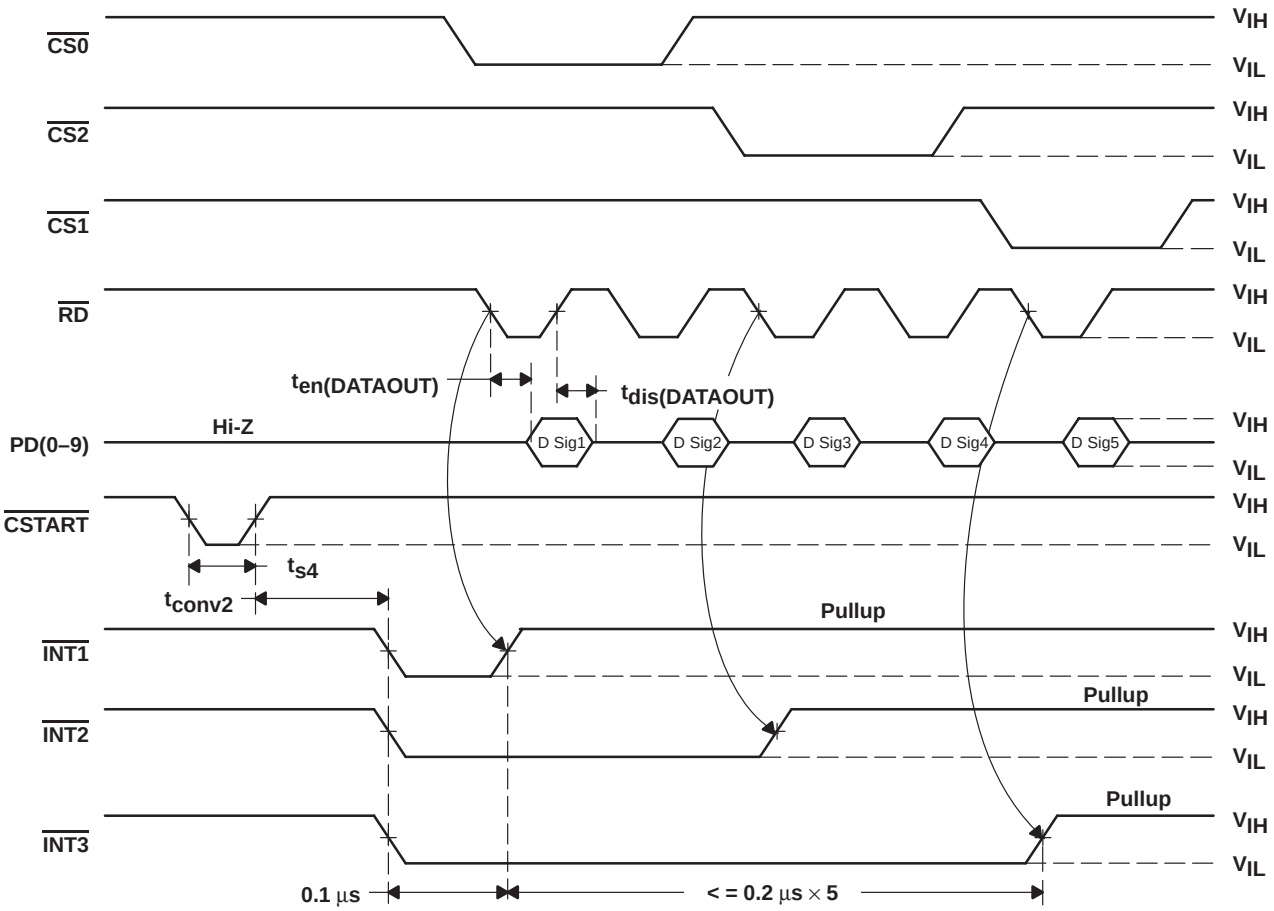


Figure 18. Multiple Chips Simultaneous Sampling/Conversion Application

APPLICATION INFORMATION



† If CLK = 10 MHz

Figure 19. Multiple Chips Simultaneous Sampling/Conversion Application System Timing

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range: AV_{DD} (see Note 1) . . . . . –0.5 V to 6.5 V
BDV_{DD}, DV_{DD} (see Note 2) . . . . . –0.5 V to 6.5 V
AV_{DD} to DV_{DD} or BDV_{DD} . . . . . –6.5 V to 6.5 V
Voltage range between AGND and $\overline{DGND}$ or $\overline{BDGND}$ . . . . . –0.3 V to 0.5 V
Digital input voltage range, CLKIN, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{CSTART}$ (see Note 2) . . . . . –0.3 V to DV_{DD} +0.3 V
Digital data input voltage range (see Note 2) . . . . . –0.3 V to DV_{DD} +0.3 V
Digital data output voltage range (see Note 2) . . . . . –0.3 V to DV_{DD} +0.3 V
Analog output voltage range, $\overline{INT}$ (see Note 2) . . . . . –0.1 V to AV_{DD}+ 0.1 V
Reference input voltage range, REFP (see Note 1) . . . . . –0.1 V to AV_{DD}+ 0.1 V
Reference input voltage range, REFM (see Note 1) . . . . . –0.3 V to 0.3 V
Peak input current (any input) . . . . . 20 mA
Peak total input current (all inputs) . . . . . –30 mA
Operating free-air temperature range, T_A: TLV1562C . . . . . –0°C to 70°C
TLV1562I . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Measured with respect to AGND with REF – and GND wired together (unless otherwise noted).
2. Measured with respect to DGND.

recommended operating conditions

PARAMETERS		MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD}, BDV_{DD}, DV_{DD} (see Note 3)		2.7		5.5	V
Positive external reference voltage input, VREFP (see Note 4)		AGND +1.7		AV_{DD} – 1	V
Negative external reference voltage input, VREFM (see Note 4)		AGND +0.9		AV_{DD} – 1	V
Differential reference voltage input, (VREFP–VREFM) (see Note 4)		0.8		MIN of AV_{DD} – 1.9 or 3	V
Single-ended analog input voltage, (AIN – AGND) (see Note 4)		VREFM		VREFP	V
Differential analog input voltage, (AINP–AINM)		0.8		3	V
Common mode analog input voltage, (AINP+AINM)/ 2		AGND		AV_{DD}	V
External SYSCLK 40/60 cycle time, $t_{c(EXTSYSCLK)}$		0.067		1	µs
External SYSCLK pulse duraton high, $t_{wH(EXTSYSCLK)}$		40%		60%	t_c(EXT SYSCLK)
External SYSCLK pulse duration low, $t_{wL(EXTSYSCLK)}$		40%		60%	t_c(EXT SYSCLK)
High-level digital and control input voltage, V_{IH}		2.1			V
Low-level digital and control input voltage, V_{IL}				0.8	V
Operating free-air temperature, T_A	TLV1562C	0		70	°C
	TLV1562I	–40		85	°C

NOTES: 3. The absolute difference between AV_{DD}, BDV_{DD} and DV_{DD} should be less than 0.5 V.
4. Analog input voltages greater than that applied to VREFP convert as all ones (111111111111), while input voltages less than that applied to VREFM convert as all zeros (000000000000).

electrical characteristics over recommended operating free-air temperature range, differential input, AV_{DD} = DV_{DD} =BDV_{DD} = 3 V, VREFP – VREFM = 1 V, external SYSCLK = 10 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Digital high-level output voltage	BDV_{DD} = 5.5 V, I_{OH} = –0.2 mA	2.4			V
		BDV_{DD} = 2.7 V, I_{OH} = –20 μA	BDV_{DD}–0.1			
V_{OL}	Digital low-level output voltage	BDV_{DD} = 5.5 V, I_{OL} = 0.8 mA			0.4	V
		BDV_{DD} = 2.7 V, I_{OL} = 20 μA			0.1	
I_{OZ}	Off-state output current (high-impedance state)	V_O = BDV_{DD}, $\overline{CS}$ = BDV_{DD}		0.005	1	μA
		V_O = BDGND, $\overline{CS}$ = BDV_{DD}	–1	–0.005		
I_{IH}	High-level input current	V_I = BDV_{DD}		0.005	1	μA
I_{IL}	Low-level input current	V_I = BDGND		–0.005	1	μA
I_{DD}	Total operating supply current, (from AV_{DD}, DV_{DD}, and BDV_{DD})	$\overline{CS}$ at BDGND, AV_{DD} = 5.5 V, SYSCLK = 10 MHz		8.5	11	mA
		$\overline{CS}$ at BDGND, AV_{DD} = 2.7 V, SYSCLK = 8 MHz		5	7	
	Total auto-powerdown supply current (from AV_{DD}, DV_{DD}, and BDV_{DD})	$\overline{CS}$ at BDGND, AV_{DD} = 5.5 V, SYSCLK = 10 MHz, CMOS control level, Auto powerdown = 1		85	120	μA
		$\overline{CS}$ at BDGND, AV_{DD} = 5.5 V, SYSCLK = 10 MHz, TTL control level, Auto powerdown = 1		200	300	
	Total S/W powerdown supply current (from AV_{DD}, DV_{DD}, and BDV_{DD})	$\overline{CS}$ at BDGND, AV_{DD} = 5.5 V, SYSCLK = 10 MHz, CMOS control level, S/W powerdown = 1		0.2	1	μA
		$\overline{CS}$ at BDGND, AV_{DD} = 5.5 V, SYSCLK = 10 MHz, TTL control level, S/W powerdown = 1		60	80	
	Selected channel leakage current	Selected channel at AV_{DD}		0.25	1	μA
		Selected channel at AGND		0.25	–1	
	Maximum static analog reference current into REFP	VREFP = AV_{DD} – 1.9 V, AV_{DD} = 5.5 V, VREFM = AGND + 0.9 V, SYSCLK = 10 MHz		150	180	μA
	Reference input impedance	V_{DD} = 5.5 V, $\overline{CS}$ = 0, SCLK = 10 MHz	17	25	30	kΩ
	Output capacitance				5	pF
C_i	Input capacitance	Analog inputs fixed		9	10	pF
		Analog inputs switching		0.5	1	
		Control inputs		20	25	
R_{ON}	Input MUX ON resistance	V_{DD} = 5.5 V			0.5	kΩ
		V_{DD} = 2.7 V			1	

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

timing requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Delay time, $\overline{CS}\downarrow$ to $\overline{WR}\downarrow$, $t_{d(CSL–WRL)}$		2		4	ns
Delay time, $\overline{RD}\uparrow$ to $\overline{CSTART}\downarrow$, $t_{d1(RDH – CSTARTL)}$		100			ns
Delay time, $\overline{RD}\uparrow$ to $\overline{CSTART}\downarrow$, $t_{d2(RDH – CSTARTL)}$		300			ns
Delay time, $\overline{WR}\uparrow$ to $\overline{CSTART}\downarrow$, $t_{d1(WRH – CSTARTL)}$		100			ns
Delay time, $\overline{WR}\uparrow$ to $\overline{CSTART}\downarrow$, $t_{d2(WRH – CSTARTL)}$		300			ns
Delay time, $\overline{CS}\downarrow$ to $\overline{RD}\downarrow$, $t_{d(CSL–RDL)}$		2		4	ns
Pulse duration, $\overline{CS}$ high, $t_{w(CSH)}$		50			ns
Setup time, data valid to $\overline{WR}\uparrow$, $t_{su(DATAIN)}$		5			ns
Hold time, $\overline{WR}\uparrow$ to data invalid, $t_{h(DATAIN)}$		10			ns
Pulse duration, RD low, $t_{w(RDL)}$	Interrupt modes	50			ns
	Continuous modes	200			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WRL)}$		50			ns
Delay time, $\overline{WR}\uparrow$ to $\overline{CS}\uparrow$, $t_{d(WRH–CSH)}$		4			ns
Delay time, $\overline{RD}\uparrow$ to $\overline{CS}\uparrow$, $t_{d(RDH–CSH)}$		4			ns
Delay time, external SYSCLK$\downarrow$ to $\overline{RD}\downarrow$, $\overline{CSTART}\uparrow$, $t_{d(ECLKL–TRGL)}$		0	2		ns
Setup time, $\overline{RD}\downarrow$, $\overline{CSTART}\uparrow$, to external SYSCLK$\uparrow$, $t_{su(TRGL–ECLKH)}$		5	6		ns
Pulse duration, CSTART low, $t_{w(CSTARTL)}$	Auto power down = 1	800			ns
	Auto power down = 0	100			
Delay time, $\overline{INT}\downarrow$ to $\overline{CS}\downarrow$, $t_{d(INTL–CSL)}$		10			ns
Conversion time, mono continuous/interrupt mode, t_{conv1}	External SYSCLK, 10 bit		5	5.5	SYSCLK
	Internal SYSCLK, 10 bit			6	
	External SYSCLK, 8 bit		4	4.5	
	Internal SYSCLK, 8 bit			5	
	External SYSCLK, 4 bit		2	2.5	
	Internal SYSCLK, 4 bit			3	
Conversion time, dual continuous/interrupt mode, t_{conv2}	External SYSCLK, 10 bit		10	11	SYSCLK
	Internal SYSCLK, 10 bit			12	
	External SYSCLK, 8 bit		8	9	
	Internal SYSCLK, 8 bit			10	
	External SYSCLK, 4 bit		4	5	
	Internal SYSCLK, 4 bit			6	
Cycle time, continuous mode $\overline{RD}$, $t_{c(RD)}$	External SYSCLK, 10 bit		5	5.5	SYSCLK
	Internal SYSCLK, 10 bit		6		
	External SYSCLK, 8 bit		4	4.5	
	Internal SYSCLK, 8 bit		5		
	External SYSCLK, 4 bit		2	2.5	
	Internal SYSCLK, 4 bit		3		
Mono interrupt mode sampling time or first cycle (mono interrupt or continous mode) sampling time, t_{s1}		0.2		1000	µs
Dual interrupt mode sampling time or first cycle (dual interrupt or continuous mode) sampling time, t_{s4}		0.3		1000	µs
Mono continuous mode sampling time, t_{s2}			3		SYSCLK
Dual continuous mode sampling time, t_{s3}			7		SYSCLK
Continuous mode first sampling time, $t_{(SAMPE5)}$		0.45			µs
Data rise time, $t_{r(DATAOUT)}$		3	5	10	ns

timing requirements (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data fall time, $t_{f(DATAOUT)}$		2	4	8	ns
Control signal rise time, $\overline{RD}$, $\overline{RW}$, $\overline{CSTART}$, $\overline{CS}$, and DATA, $t_{r(I/O)}$		2		1000	ns
Control signal fall time, $\overline{RD}$, $\overline{RW}$, $\overline{CSTART}$, $\overline{CS}$, and DATA, $t_{f(I/O)}$		2		1000	ns

operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Integral linearity error, center best fit (see Note 5)	f_I = 800 kHz at 10 bit 2 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V VREFM = 1.5 V, mono continuous		±0.6	±1	LSB
	f_I = 800 kHz at 10 bit 2.5 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, mono continuous	–1.5	±0.85	±1.5	
	f_I = 800 kHz at 10 bit 2.8 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, mono continuous		±1.5		
	f_I = 800 kHz at 10 bit 2 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, mono continuous		±0.6	±1	
	f_I = 800 kHz at 8 bit 3 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, mono continuous		±0.6	±1	
	f_I = 800 kHz at 8 bit 3.5 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, mono continuous		±0.65	±1	
	f_I = 800 kHz at 8 bit 3.75 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, mono continuous		±1		
	f_I = 800 kHz at 4 bit 7 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, mono continuous		±0.2	±0.4	
Differential linearity error	f_I = 800 kHz at 10 bit 2 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, mono continuous		±0.5	±1	LSB
	f_I = 800 kHz at 10 bit 2.5 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, mono continuous	–0.85	±0.5	1.5	
	f_I = 800 kHz at 10 bit 2.8 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, mono continuous		±0.9	1.5	
	f_I = 800 kHz at 10 bit 2 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, mono continuous		±0.6	±1	
	f_I = 800 kHz at 8 bit 3 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, mono continuous		±0.5	±1	
	f_I = 800 kHz at 8 bit 3.5 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, mono continuous	–0.8	±0.5	1	
	f_I = 800 kHz at 8 bit 3.75 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, mono continuous		±1	1	
	f_I = 800 kHz at 4 bit 7 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, mono continuous		±0.2	±0.4	

NOTE 5: Linear error is the maximum deviation from the best straight line through the A/D transfer characteristics.

operating characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Mid-scale error (see Note 6)	Before calibration			±5	%FS
	After system calibration, single-ended input			±0.4	
	After system calibration, differential input			±0.25	
	After internal calibration, single-ended input			±2.5	
	After internal calibration, differential input			±0.3	
Offset error (see Note 6)	Before calibration			±5	%FS
Gain error (see Note 6)	Before calibration			±5	%FS
Total unadjusted error (see Note 7)	Before calibration			±5	%FS
Delay time, $\overline{RD}\downarrow$, $\overline{CSTART}\uparrow$ to external SYSCLK$\uparrow$, $t_{d(TRGL–ICLKH)}$		2ns		0.5	SYSCLK
Delay time, $\overline{RD}\downarrow$ to start of conversion $t_{d(RDL–CONV1)}$				2	ns
Internal OSC frequency		7.5			MHz
Delay time, $\overline{RD}\uparrow$ to $\overline{INT}\uparrow$, $t_{d(RDH–INTZ)}$	1-kΩ pullup resistor, 10 pF, BDV_{DD} = 5 V, use $\overline{RD}$			10	ns
Disable time, $\overline{RD}\uparrow$ to data invalid, $t_{dis(DATAOUT)}$	At 25 pF, BDV_{DD} = 5 V			4	ns
	At 50 pF, BDV_{DD} = 5 V			5	
	At 100 pF, BDV_{DD} = 5 V			7	
	At 25 pF, BDV_{DD} = 2.7 V			7	
	At 50 pF, BDV_{DD} = 2.7 V			10	
	At 100 pF, BDV_{DD} = 2.7 V			14	
Enable time, $\overline{INT}\downarrow$ to data valid, $t_{en(DATAOUT)}$	At 25 pF, BDV_{DD} = 5 V			20	ns
	At 50 pF, BDV_{DD} = 5 V			25	
	At 100 pF, BDV_{DD} = 5 V			30	
	At 25 pF, BDV_{DD} = 2.7 V			37	
	At 50 pF, BDV_{DD} = 2.7 V			41	
	At 100 pF, BDV_{DD} = 2.7 V			56	
Delay time, mono interrupt mode power-up time, $t_{1(APDR)}$	Auto powerdown = 1	700			ns
	Auto powerdown = 0	0			
Delay time, dual interrupt mode power-up time, $t_{2(APD)}$	Auto powerdown = 1	1000			ns
	Auto powerdown = 0	0			
Delay time, INT$\downarrow$ to powerdown, $t_{(APD)}$	Auto powerdown = 1	200			ns
	Auto powerdown = 0	0			
Delay time, end of conversion to $\overline{INT}\downarrow$, $t_{d(CONV-INTL)}$		5		10	ns
Delay time, $\overline{RD}\downarrow$ to $\overline{INT}$ Hi-Z, $t_{d(RDL-INTZ)}$	1-kΩ pullup resistor, 10 pF, BDV_{DD} = 5 V, Use $\overline{CSTART}$			10	ns
Delay time, $\overline{CSTART}\uparrow$ to start of conversion 1, $t_{d1(CSTARTH-CONV)}$		2	4		ns
Delay time, $\overline{CSTART}\uparrow$ to start of conversion 2, $t_{d2(CSTARTH-CONV)}$		0.2		1000	µs
Delay time, $\overline{RD}\downarrow$ to sample, $t_{d(RDL-SAMPLE)}$			2		SYSCLK

NOTES: 6. Zero error is the difference between 000000000000 and the converted output for zero input voltage: full-scale error is the difference between 111111111111 and the converted output for full-scale input voltage
7. Total unadjusted error comprises linearity, zero, and full-scale errors

operating characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

ac specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
10-Bit Mode						
ENOB	Effective number of bits	f_I = 800 kHz, at 10 bit 2 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, Mono continuous	8.97	9.4		Bits
		f_I = 800 kHz, at 10 bit 1.6 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, Mono continuous	8.8	8.91		
THD	Total harmonic distortion	f_I = 800 kHz, at 10 bit 2 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, Mono continuous		–68.8	–64.5	dB
		f_I = 800 kHz, at 10 bit 1.6 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, Mono continuous		–66.8	–64.5	
SNR	Signal-to-noise ratio	f_I = 800 kHz, at 10 bit 2 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, Mono continuous	56.4	58.1		dB
		f_I = 800 kHz, at 10 bit 1.6 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, Mono continuous	54.4	55.6		
SINAD	Signal-to-noise ratio +distortion	f_I = 800 kHz, at 10 bit 2 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, Mono continuous	56.2	57.8		dB
		f_I = 800 kHz, at 10 bit 1.6 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, Mono continuous	54.2	55.3		
SFDR	Spurious free dynamic range	f_I = 800 kHz, at 10 bit 2 MSPS, AV_{DD} = 5 V, VREFP = 3.5 V, VREFM = 1.5 V, Mono continuous		–70.3	–67.5	dB
		f_I = 800 kHz, at 10 bit 1.6 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, Mono continuous		–69.1	–66.5	
8-Bit Mode						
ENOB	Effective number of bits	f_I = 800 kHz, at 8 bit 3 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, Mono continuous		7.93		Bits
THD	Total harmonic distortion			–64		dB
SNR	Signal-to-noise ratio			49.2		dB
SINAD	Signal-to-noise ratio +distortion			49		dB
SFDR	Spurious free dynamic range			–65		dB
4-Bit Mode						
ENOB	Effective number of bits	f_I = 800 kHz, at 4 bit 7 MSPS, AV_{DD} = 3 V, VREFP = 1.7 V, VREFM = 0.9 V, Mono continuous		3.97		Bits
THD	Total harmonic distortion			–29		dB
SINAD	Signal-to-noise ratio + distortion			26		dB
SINAD	Signal-to-noise ratio + distortion			24		dB
SFDR	Spurious free dynamic range			–30.5		dB
Analog input						
	Cross talk rejection			68		dB
	Full-power bandwidth, –3 dB			120		MHz
	Full-power bandwidth, –1 dB			75		MHz

TYPICAL CHARACTERISTICS

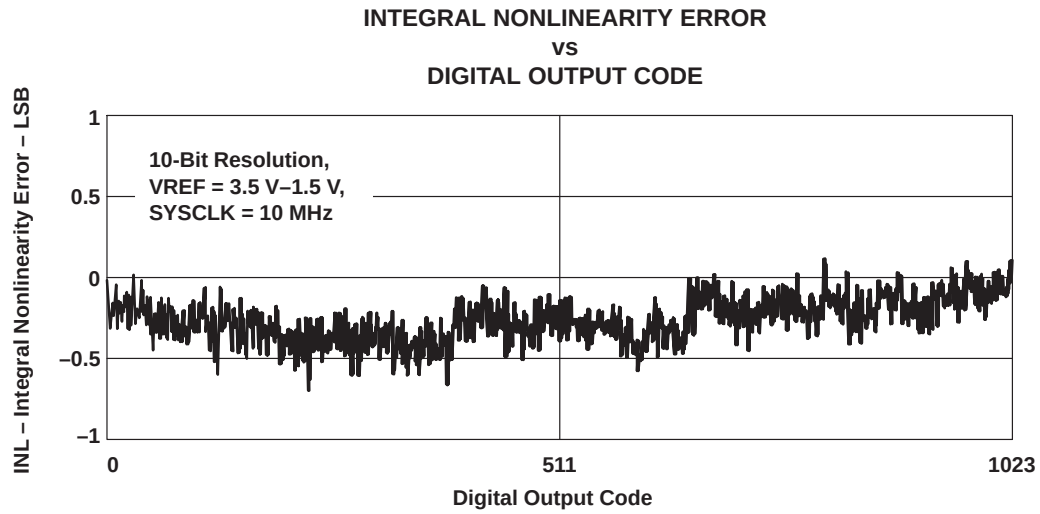


Figure 20

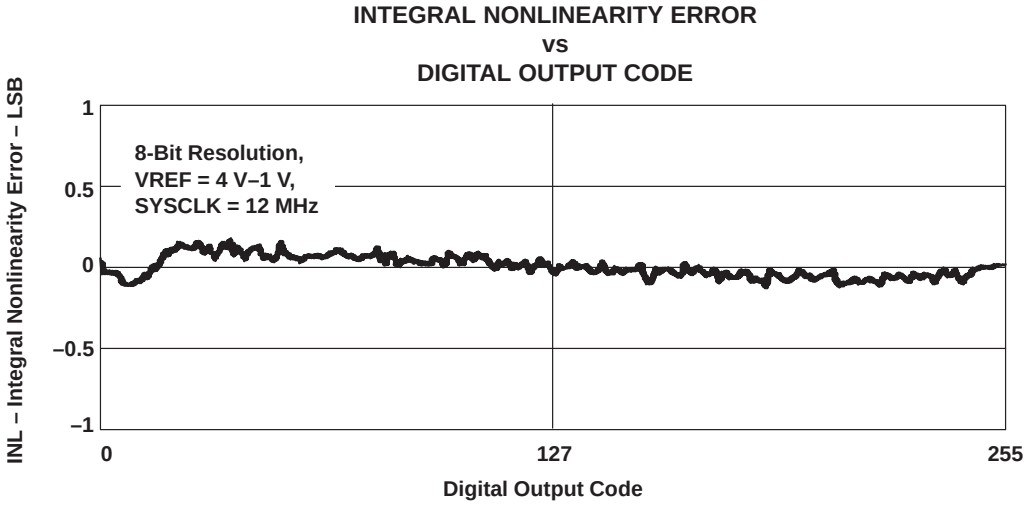


Figure 21

TYPICAL CHARACTERISTICS

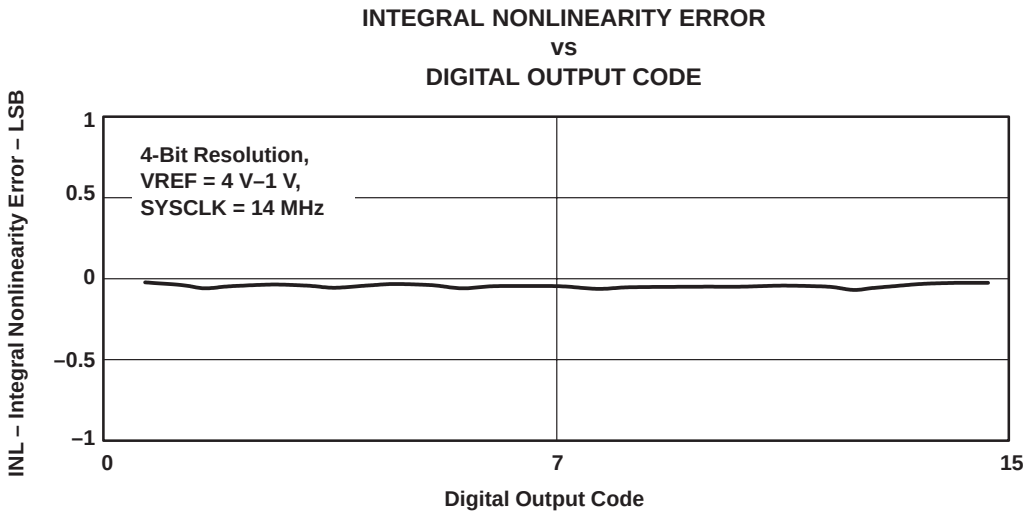


Figure 22

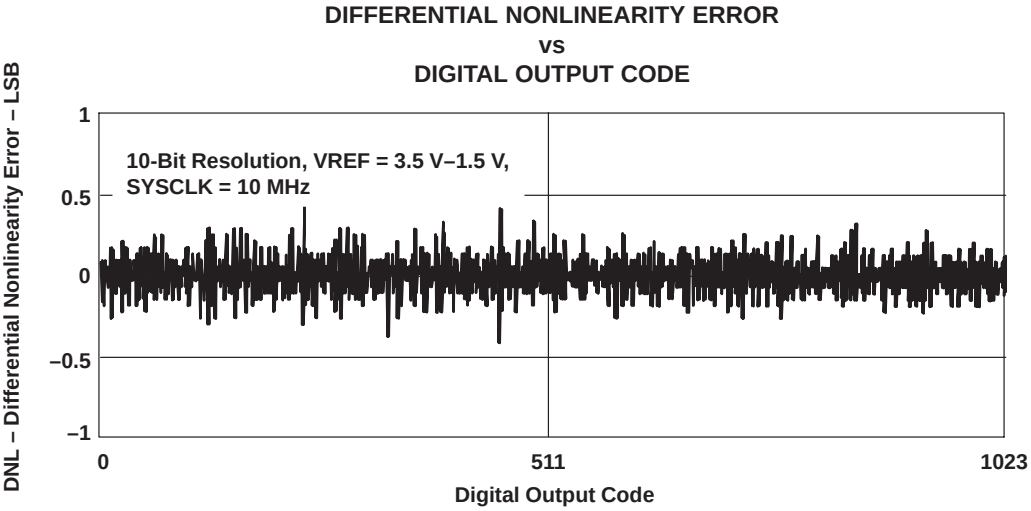


Figure 23

TYPICAL CHARACTERISTICS

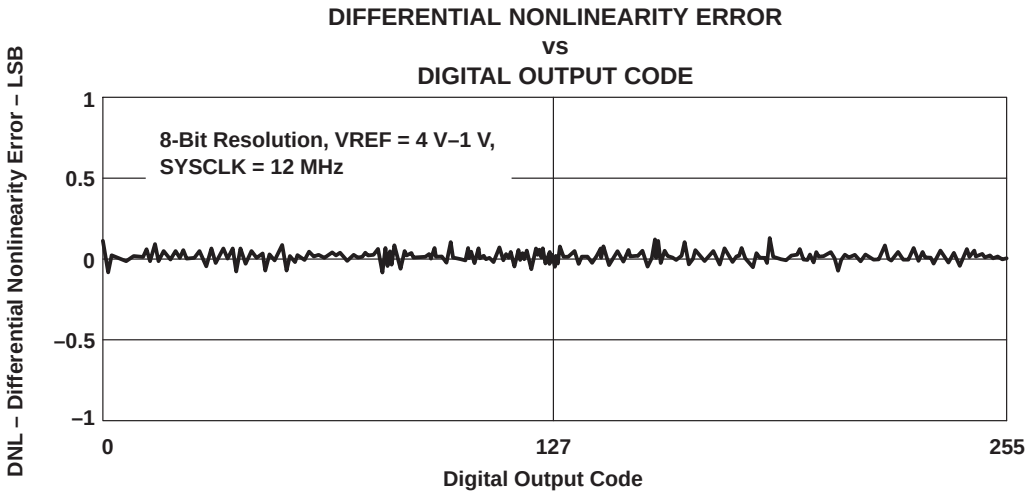


Figure 24

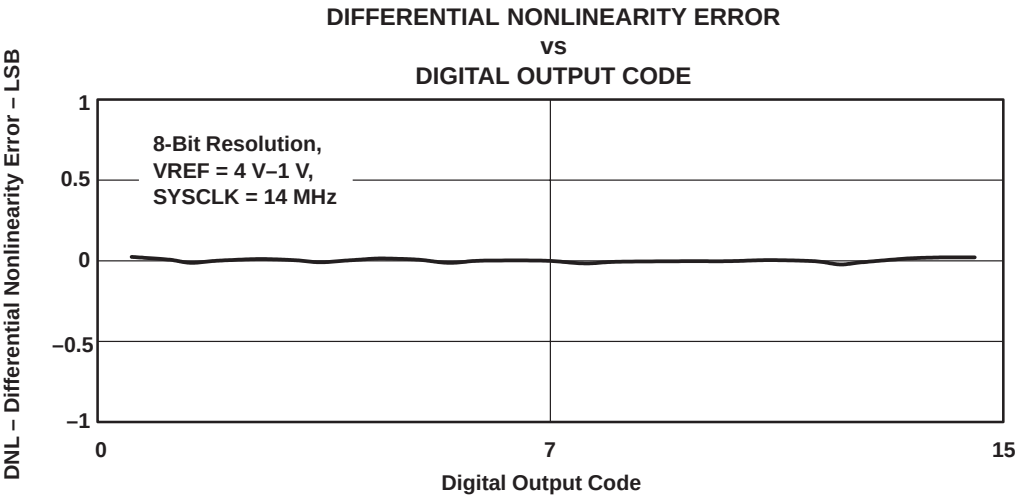


Figure 25

TYPICAL CHARACTERISTICS

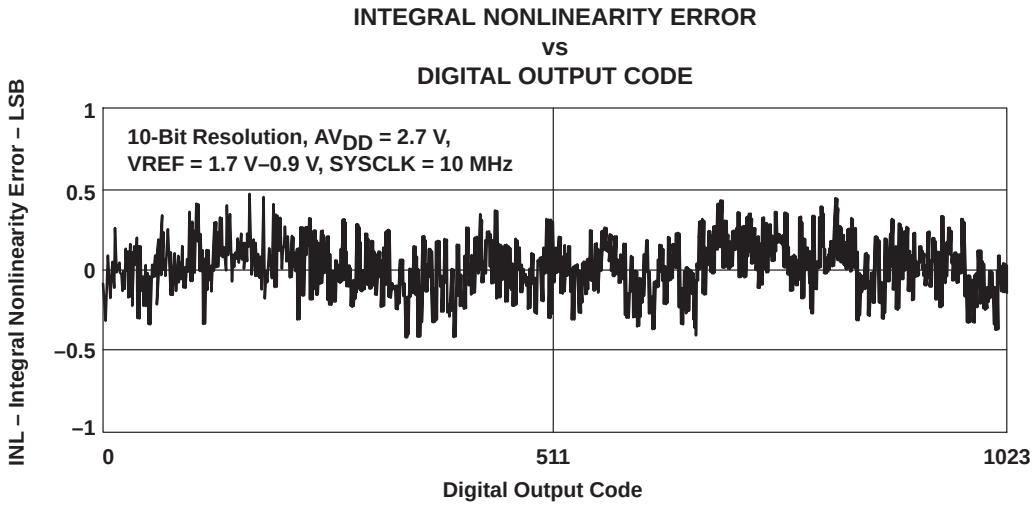


Figure 26

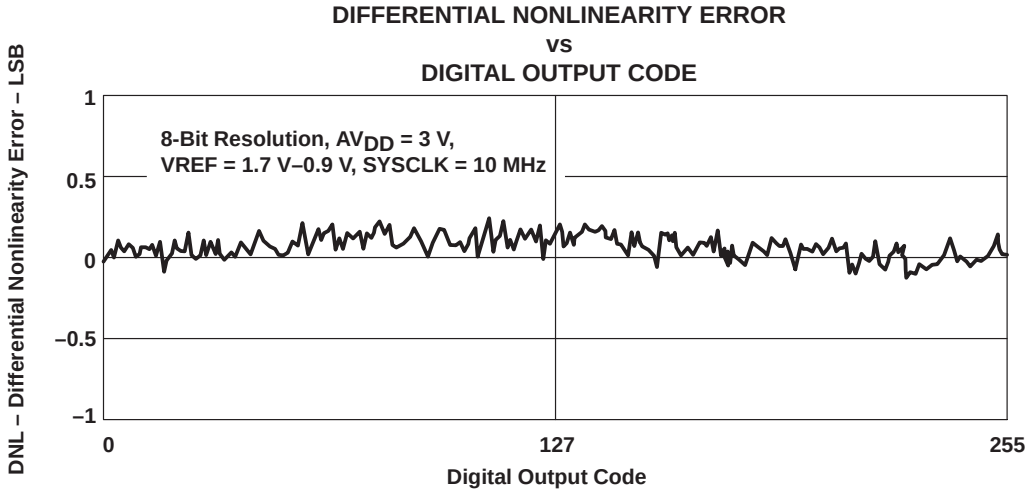


Figure 27

TYPICAL CHARACTERISTICS

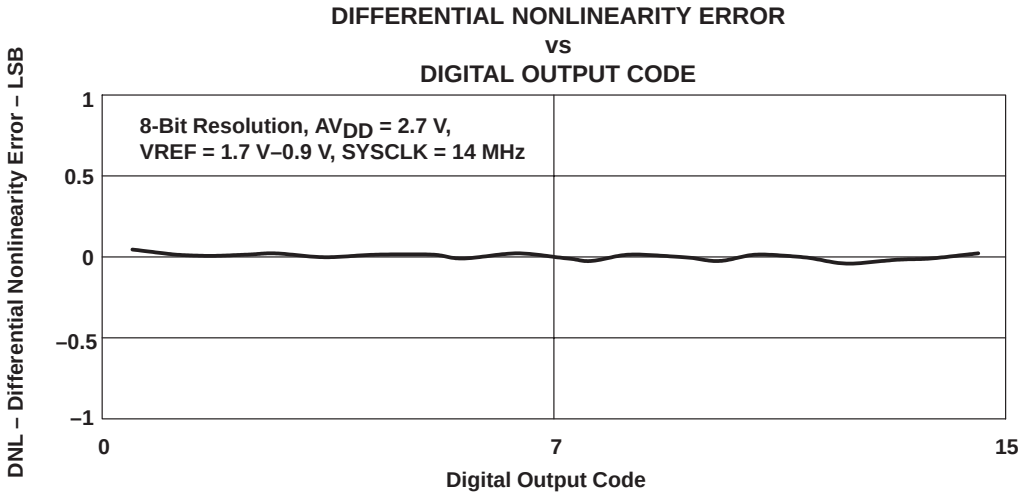


Figure 28

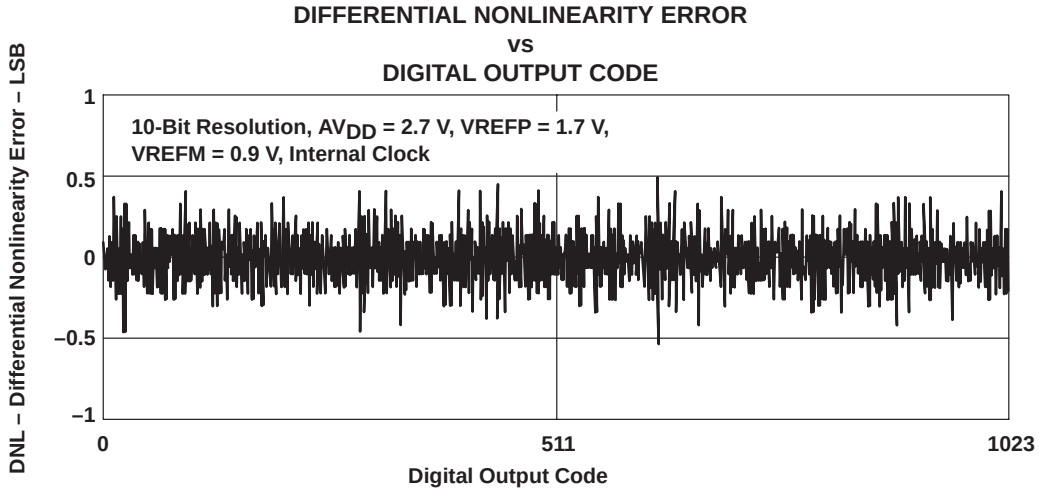


Figure 29

TYPICAL CHARACTERISTICS

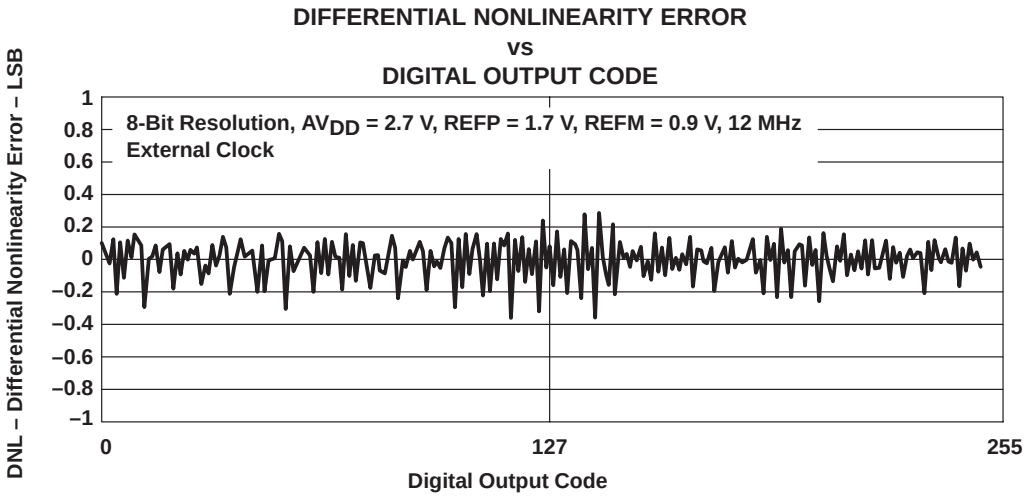


Figure 30

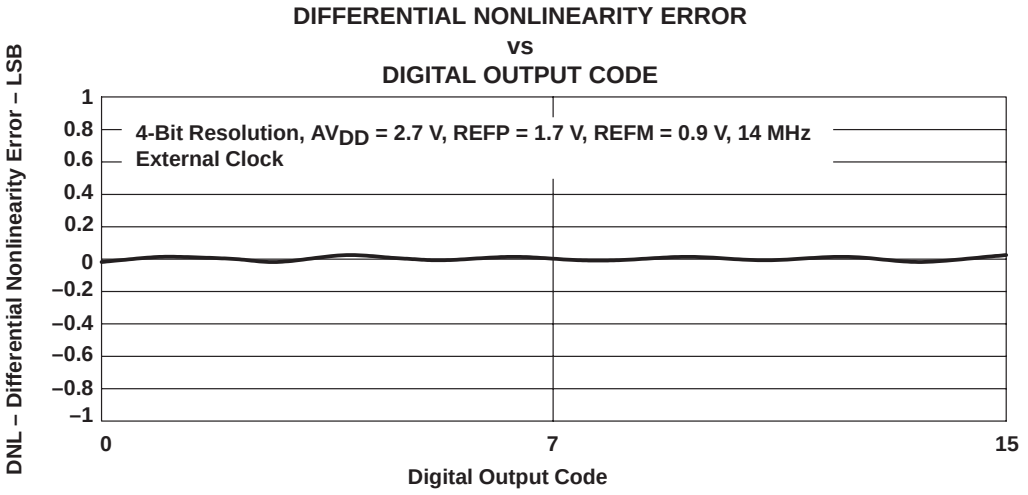


Figure 31

TYPICAL CHARACTERISTICS

TYPICAL SUPPLY CURRENT vs FREQUENCY

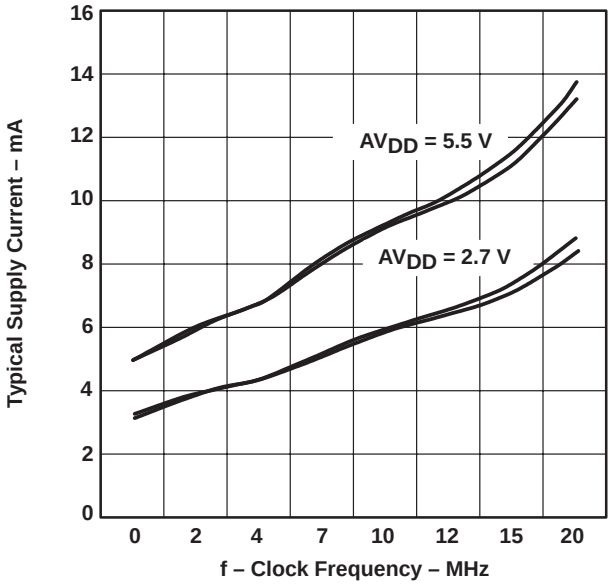


Figure 32

TYPICAL POWER DOWN CURRENT vs TEMPERATURE

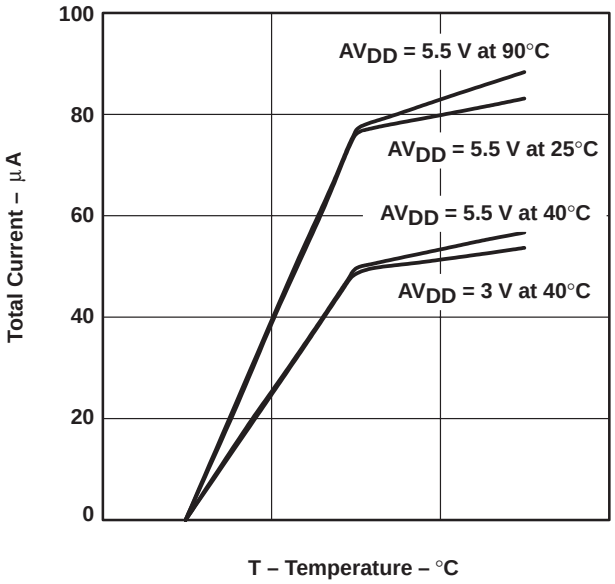


Figure 33

SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY

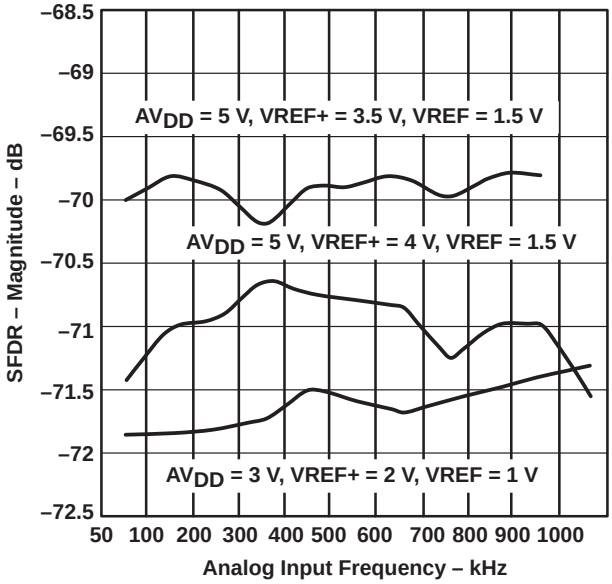


Figure 34

SIGNAL TO NOISE vs INPUT FREQUENCY

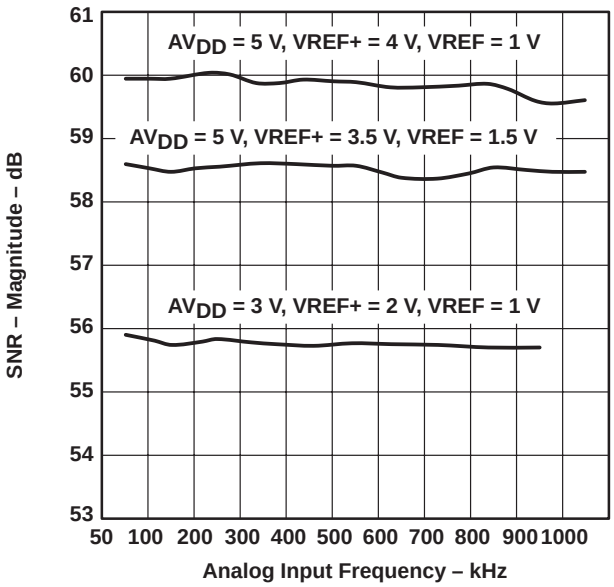


Figure 35

TYPICAL CHARACTERISTICS

SIGNAL TO NOISE HARMONIC DISTORTION
vs
INPUT FREQUENCY

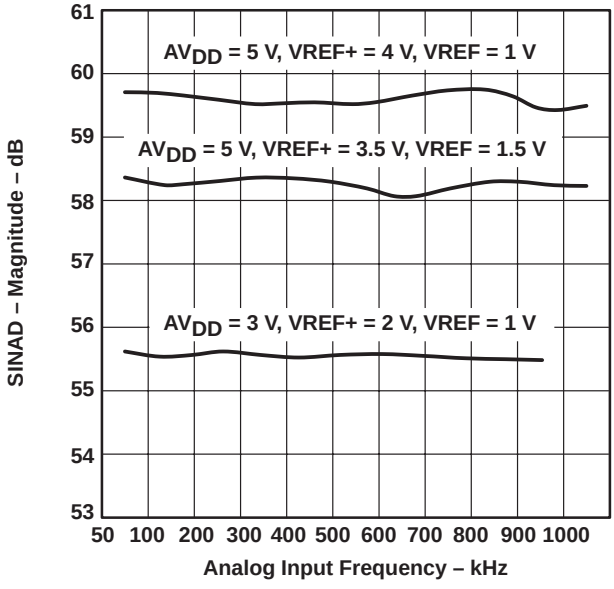


Figure 36

EFFECTIVE NUMBER OF BITS
vs
INPUT FREQUENCY

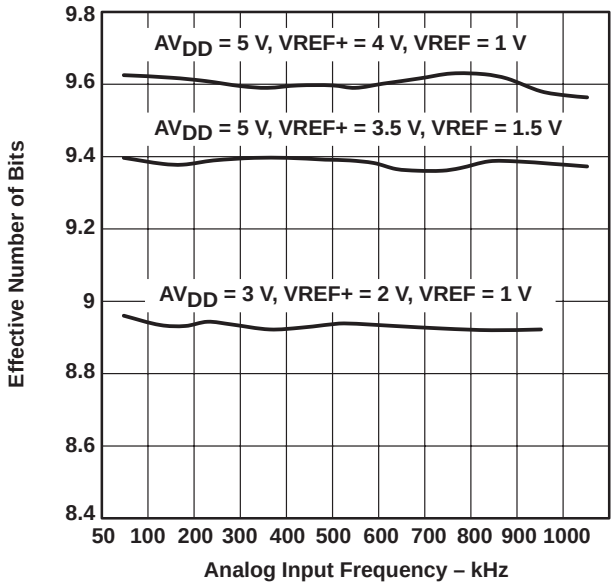


Figure 37

TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY

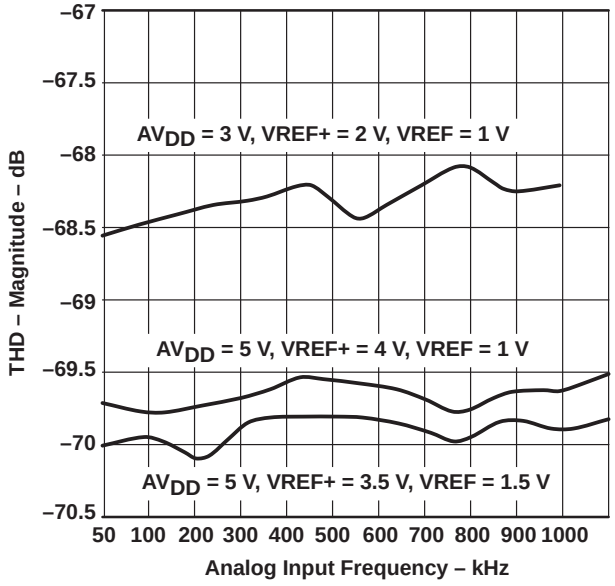
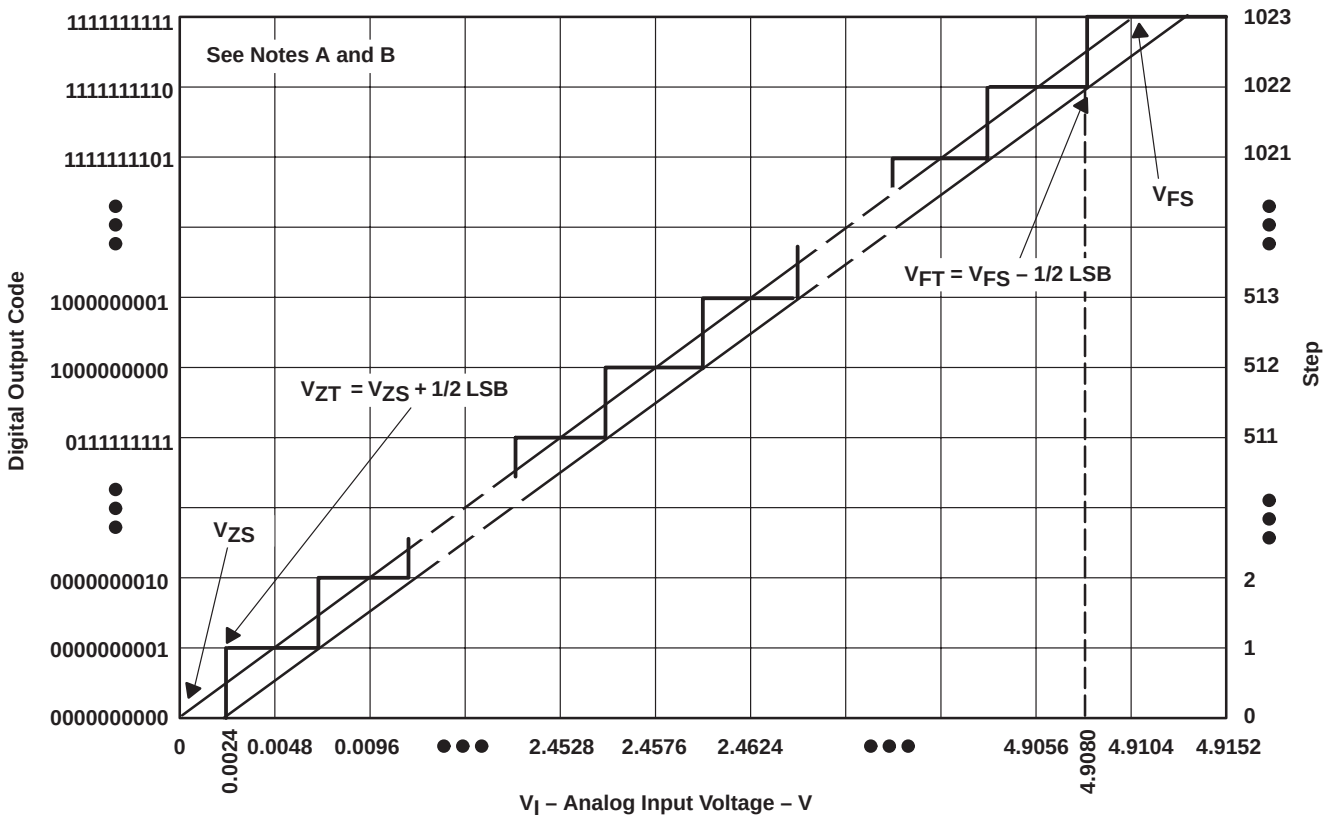


Figure 38

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V and the transition to full scale (V_{FT}) is 4.908 V. 1 LSB = 4.8 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 39. Ideal 12-Bit ADC Conversion Characteristics

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