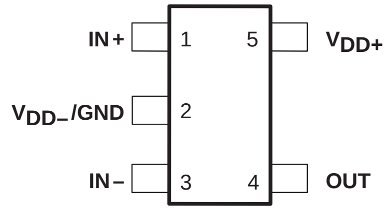
TLV2221, TLV2221Y Advanced LinCMOS™ RAIL-TO-RAIL VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Single-Supply 3-V and 5-V Operation**
- **Very Low Power . . . 110 μA Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Wide Supply Voltage Range 2.7 V to 10 V**
- **Macromodel Included**

DBV PACKAGE
(TOP VIEW)



description

The TLV2221 is a single operational amplifier manufactured using the Texas Instruments Advanced LinCMOS™ process. This device is optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with micropower dissipation levels, the input noise voltage performance has been dramatically improved using optimized design techniques for CMOS-type amplifiers. Another added benefit is that this amplifier exhibits rail-to-rail output swing. The output dynamic range can be extended using the TLV2221 with loads referenced midway between the rails. The common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ± 5 mV, allowing a minimum of 0-V to 2-V common-mode input voltage range for a 3-V power supply.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES SOT-23 (DBV)†	SYMBOL	CHIP FORM (Y)
0°C to 70°C	3 mV	TLV2221CDBV	VADC	TLV2221Y
–40°C to 85°C	3 mV	TLV2221IDBV	VADI	

† The DBV package available in tape and reel only.

The Advanced LinCMOS process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The TLV2221, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power dissipation levels combined with 3-V operation, this device works well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split power supplies makes this device an excellent choice when interfacing directly to analog-to-digital converters (ADCs). All of these features combined with its temperature performance make the TLV2221 ideal for remote pressure sensors, temperature control, active voltage-resistive (VR) sensors, accelerometers, hand-held metering devices, and many other applications.

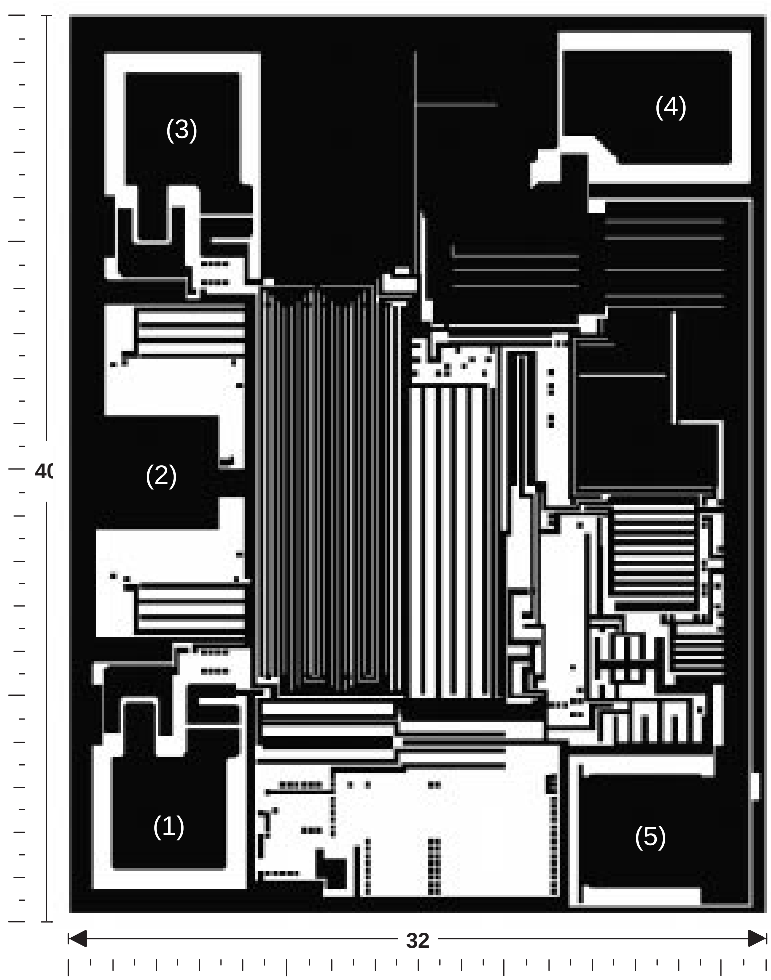
description (continued)

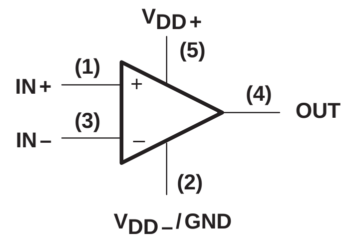
The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-PRF-38535; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

TLV2221Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2221C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

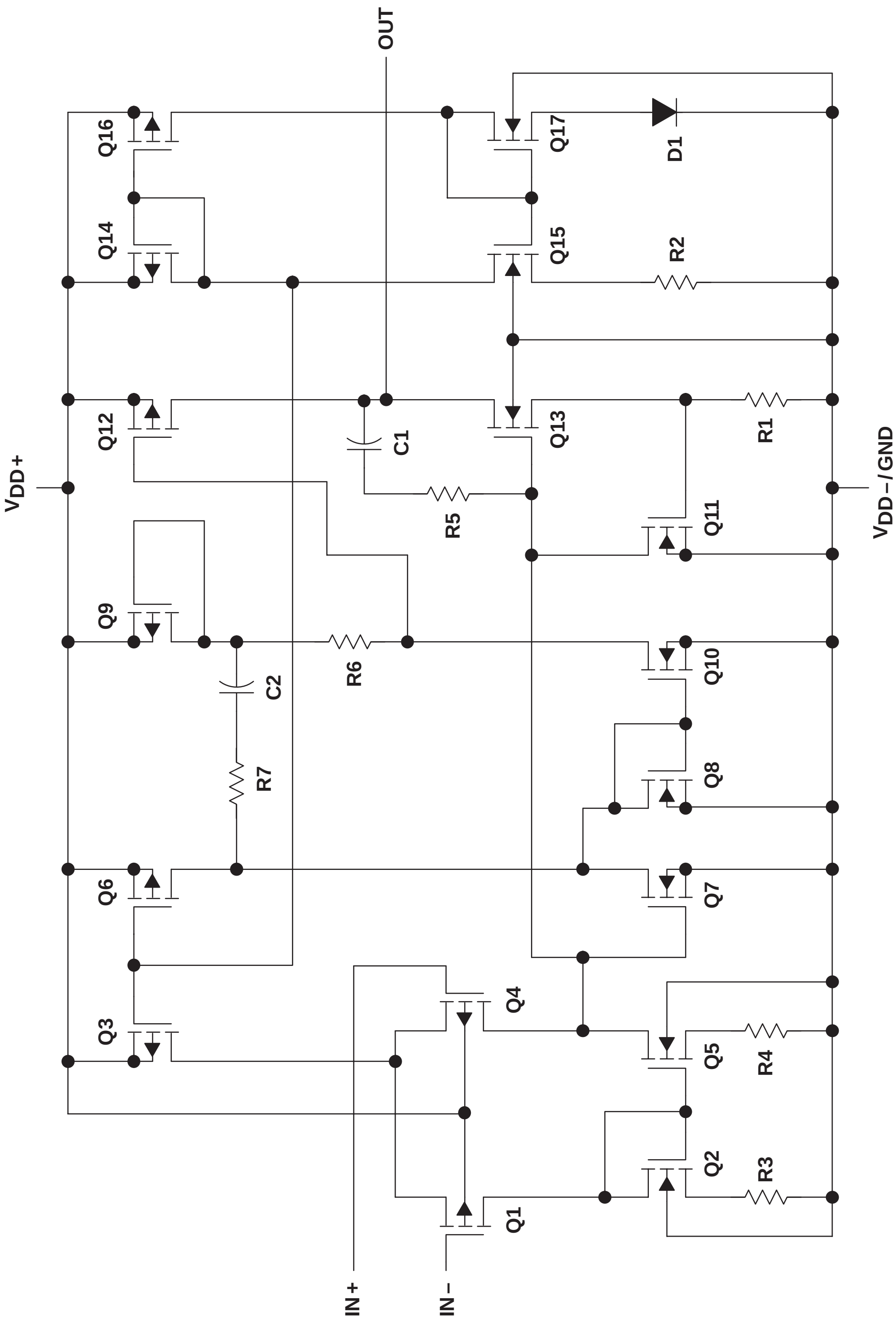
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (2) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic



COMPONENT COUNT†	
Transistors	23
Diodes	5
Resistors	11
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 12 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) . . . . . –0.3 V to V_{DD}
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of V_{DD-} . . . . . ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TLV2221C . . . . . 0°C to 70°C
TLV2221I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below V_{DD-} – 0.3 V.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

recommended operating conditions

	TLV2221C		TLV2221I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	V_{DD+} –1.3	V_{DD-}	V_{DD+} –1.3	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} –1.3	V_{DD-}	V_{DD+} –1.3	V
Operating free-air temperature, T_A	0	70	–40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2221C			TLV2221I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm1.5$ V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	Full range		0.62	3		0.62	3	mV
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1			1		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\| \le 5$ mV	25°C	0 to 2	–0.3 to 2.2		0 to 2	–0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = –100 µA		25°C		2.97			2.97		V
		I_{OH} = –400 µA		25°C		2.88			2.88		
				Full range	2.5			2.5			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 µA	25°C		15			15		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 µA	25°C		150			150		
				Full range			500			500	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 2 kΩ‡	25°C	2	3		2	3		V/mV
				Full range	1			1			
			R_L = 1 MΩ‡	25°C		250			250		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz		25°C		6			6		pF
z_o	Closed-loop output impedance	f = 10 kHz,	A_V = 10	25°C		90			90		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V,	R_S = 50 Ω	25°C	70	82		70	82		dB
				Full range	65			65			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		100	150		100	150	µA
				Full range			200			200	

† Full range for the TLV2221C is 0°C to 70°C. Full range for the TLV2221I is – 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2221C			TLV2221I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, R_L = 2 kΩ‡, C_L = 100 pF‡		25°C	0.1	0.18		0.1	0.18		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		120			120		nV/√Hz
		f = 1 kHz		25°C		20			20		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		680			680		mV
		f = 0.1 Hz to 10 Hz		25°C		860			860		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA /√Hz
THD+N	Total harmonic distortion plus noise	V_O = 1 V to 2 V, f = 20 kHz, R_L = 2 kΩ‡	A_V = 1	25°C		2.52%			2.52%		
			A_V = 10			7.01%			7.01%		
		V_O = 1 V to 2 V, f = 20 kHz, R_L = 2 kΩ§	A_V = 1	25°C		0.076%			0.076%		
			A_V = 10			0.147%			0.147%		
	Gain-bandwidth product	f = 1 kHz, R_L = 2 kΩ‡, C_L = 100 pF‡		25°C		480			480		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, A_V = 1, R_L = 2 kΩ‡, C_L = 100 pF‡		25°C		30			30		kHz
t_s	Settling time	A_V = –1, Step = 1 V to 2 V, R_L = 2 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		4.5			4.5		μs
			To 0.01%	25°C		6.8			6.8		μs
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ‡, C_L = 100 pF‡		25°C		51°			51°		
	Gain margin			25°C		12			12		dB

† Full range is –40°C to 85°C.
‡ Referenced to 1.5 V
§ Referenced to 0 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2221C MIN	TLV2221C TYP	TLV2221C MAX	TLV2221I MIN	TLV2221I TYP	TLV2221I MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	Full range		0.61	3		0.61	3	mV
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1			1		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO}\rvert$ ≤ 5 mV	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = –500 µA	25°C	4.75	4.88		4.75	4.88		V
		I_{OH} = –1 mA		4.5	4.76		4.5	4.76		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 µA	25°C		12			12		mV
		V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C		120			120		
			Full range			500			500	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 2 kΩ‡	25°C	3	5		3	5		V/mV
			Full range	1			1			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ‡	25°C		800			800		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz	25°C		6			6		pF
z_o	Closed-loop output impedance	f = 10 kHz, A_V = 10	25°C		70			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 1.5 V, R_S = 50 Ω	25°C	70	85		70	85		dB
			Full range	65			65			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		110	150		110	150	µA
			Full range			200			200	

† Full range for the TLV2221C is 0°C to 70°C. Full range for the TLV2221I is – 40°C to 85°C.
‡ Referenced to 2.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2221C			TLV2221I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 2 kΩ‡,	25°C	0.1	0.18		0.1	0.18		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		90			90		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		800			800		mV
		f = 0.1 Hz to 10 Hz		25°C		960			960		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA /√Hz
THD+N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 20 kHz, R_L = 2 kΩ‡	A_V = 1	25°C		2.45%			2.45%		
			A_V = 10			5.54%			5.54%		
		V_O = 1.5 V to 3.5 V, f = 20 kHz, R_L = 2 kΩ§	A_V = 1	25°C		0.142%			0.142%		
			A_V = 10			0.257%			0.257%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 2 kΩ‡,	25°C		510			510		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 2 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		40			40		kHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 2 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.8			6.8		μs
			To 0.01%	25°C		9.2			9.2		
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ‡,	C_L = 100 pF‡	25°C		52°			52°		
	Gain margin			25°C		12			12		dB

† Full range is –40°C to 85°C.
‡ Referenced to 2.5 V
§ Referenced to 0 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2221Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm$ = ±1.5 V, R_S = 50 Ω	V_{IC} = 0,	V_O = 0,		620		µV
I_{IO}	Input offset current					0.5		pA
I_{IB}	Input bias current					1		pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert \le$ 5 mV,	R_S = 50 Ω			–0.3 to 2.2		V
V_{OH}	High-level output voltage	I_{OH} = –100 µA				2.97		V
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 µA			15		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 µA			150		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 2 kΩ†			3		V/mV
			R_L = 1 MΩ†			250		
r_{id}	Differential input resistance					10^{12}		Ω
r_{ic}	Common-mode input resistance					10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz				6		pF
z_o	Closed-loop output impedance	f = 10 kHz,	A_V = 10			90		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 0,	R_S = 50 Ω		82		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V,	V_{IC} = 0,	No load		95		dB
I_{DD}	Supply current	V_O = 0,	No load			100		µA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2221Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm$ = ±1.5 V, R_S = 50 Ω	V_{IC} = 0,	V_O = 0,		610		µV
I_{IO}	Input offset current					0.5		pA
I_{IB}	Input bias current					1		pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert \le$ 5 mV,	R_S = 50 Ω			–0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = –500 µA				4.88		V
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA			12		mV
		V_{IC} = 2.5 V,	I_{OL} = 500 µA			120		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V	R_L = 2 kΩ†			5		V/mV
			R_L = 1 MΩ†			800		
r_{id}	Differential input resistance					10^{12}		Ω
r_{ic}	Common-mode input resistance					10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz				6		pF
z_o	Closed-loop output impedance	f = 10 kHz,	A_V = 10			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 0,	R_S = 50 Ω		85		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V,	V_{IC} = 0,	No load		95		dB
I_{DD}	Supply current	V_O = 0,	No load			110		µA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

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V_{IO}	Input offset voltage	Distribution vs Common-mode input voltage	1, 2 3, 4
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V_I	Input voltage	vs Supply voltage vs Free-air temperature	8 9
V_{OH}	High-level output voltage	vs High-level output current	10, 13
V_{OL}	Low-level output voltage	vs Low-level output current	11, 12, 14
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	15
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	16 17
V_O	Output voltage	vs Differential input voltage	18, 19
A_{VD}	Differential voltage amplification	vs Load resistance	20
A_{VD}	Large signal differential voltage amplification	vs Frequency vs Free-air temperature	21, 22 23, 24
z_o	Output impedance	vs Frequency	25, 26
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	27 28
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	29, 30 31
I_{DD}	Supply current	vs Supply voltage	32
SR	Slew rate	vs Load capacitance vs Free-air temperature	33 34
V_O	Inverting large-signal pulse response	vs Time	35, 36
V_O	Voltage-follower large-signal pulse response	vs Time	37, 38
V_O	Inverting small-signal pulse response	vs Time	39, 40
V_O	Voltage-follower small-signal pulse response	vs Time	41, 42
V_n	Equivalent input noise voltage	vs Frequency	43, 44
	Input noise voltage (referred to input)	Over a 10-second period	45
THD + N	Total harmonic distortion plus noise	vs Frequency	46
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	47 48
ϕ_m	Phase margin	vs Frequency vs Load capacitance	21, 22 51, 52
	Gain margin	vs Load capacitance	49, 50
B_1	Unity-gain bandwidth	vs Load capacitance	53, 54

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2211
INPUT OFFSET VOLTAGE**

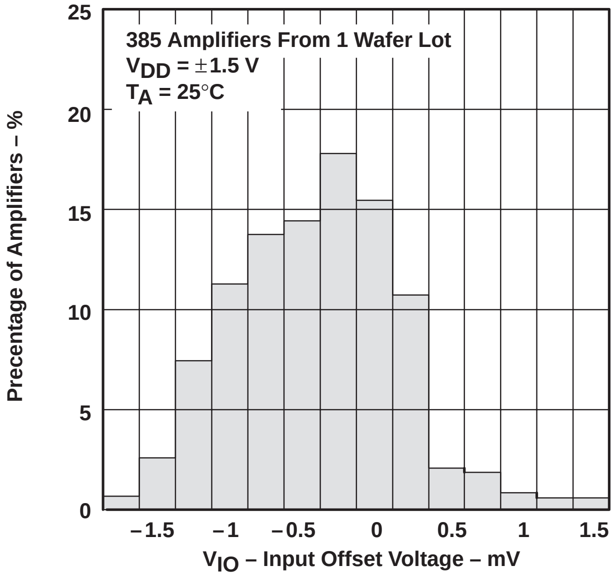


Figure 1

**DISTRIBUTION OF TLV2211
INPUT OFFSET VOLTAGE**

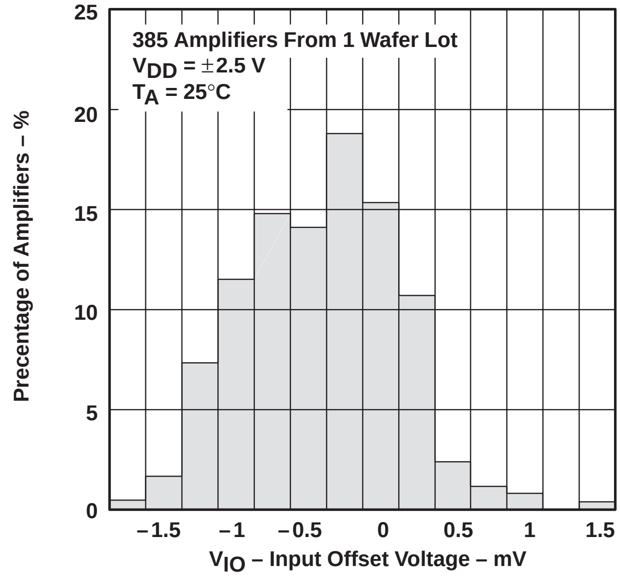


Figure 2

**INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE**

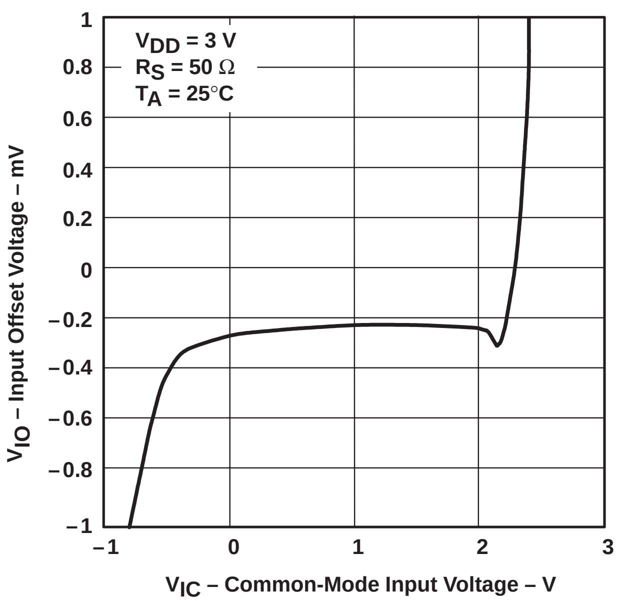


Figure 3

**INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE**

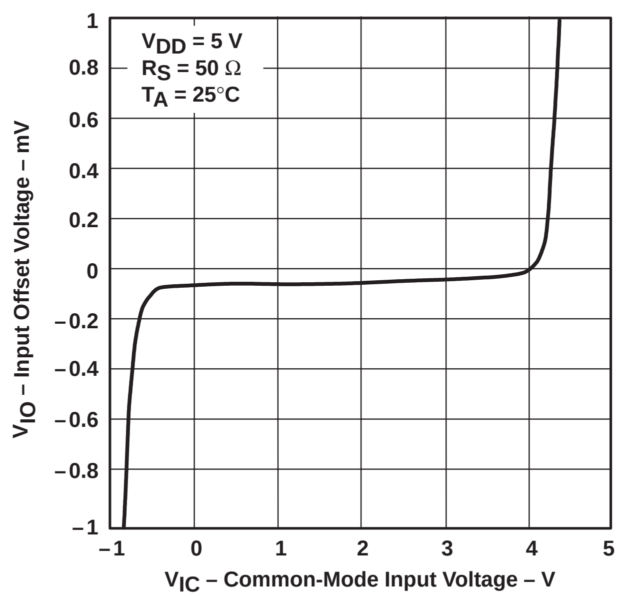


Figure 4

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2221 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

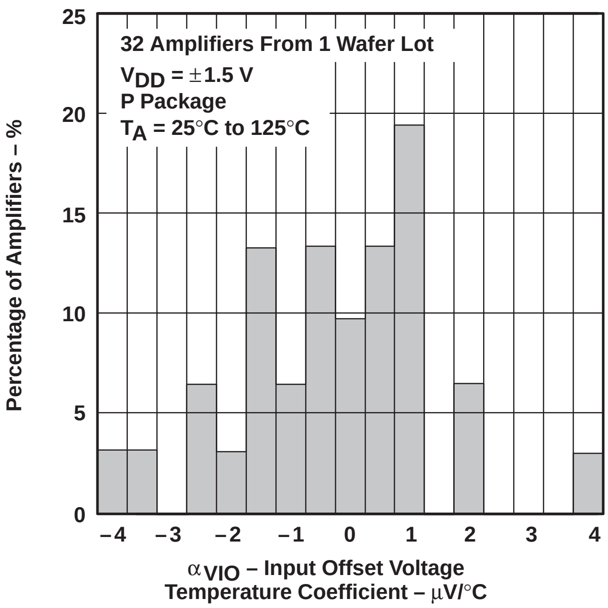


Figure 5

DISTRIBUTION OF TLV2221 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

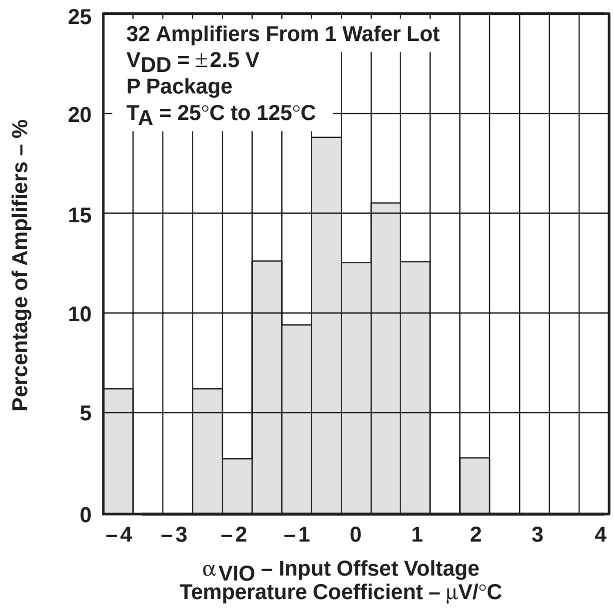


Figure 6

INPUT BIAS AND INPUT OFFSET CURRENTS
vs
FREE-AIR TEMPERATURE

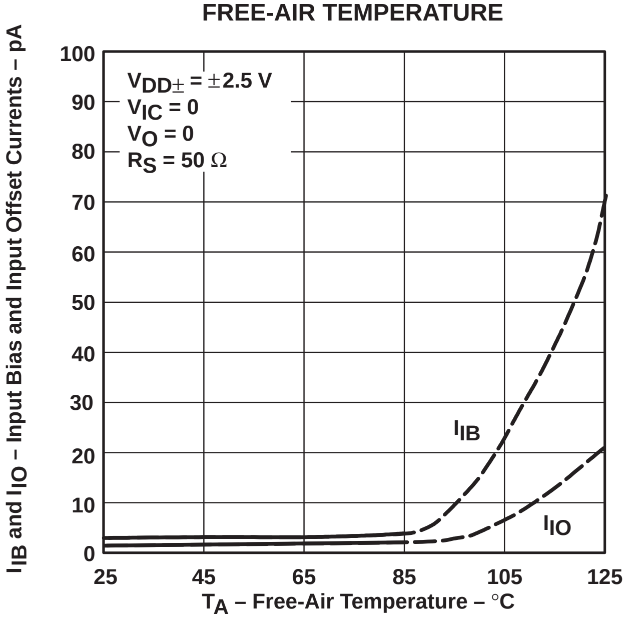


Figure 7

INPUT VOLTAGE
vs
SUPPLY VOLTAGE

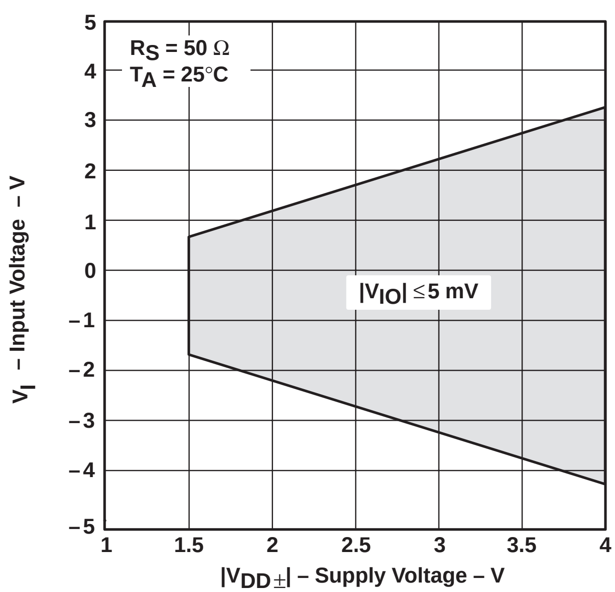


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE†‡ vs FREE-AIR TEMPERATURE

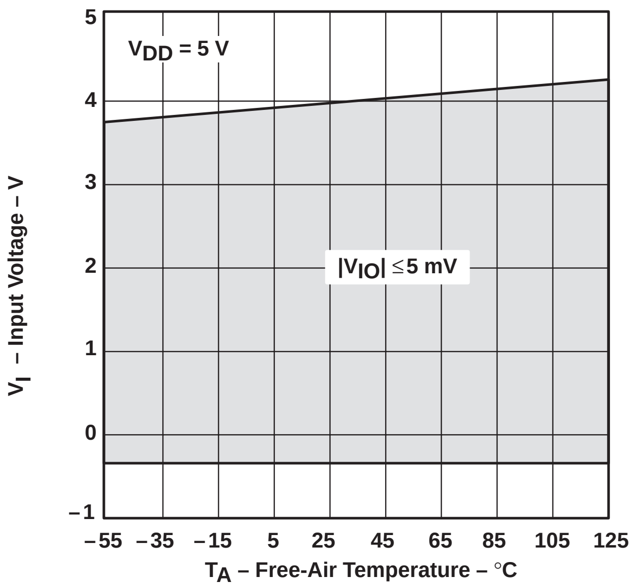


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE†‡ vs HIGH-LEVEL OUTPUT CURRENT

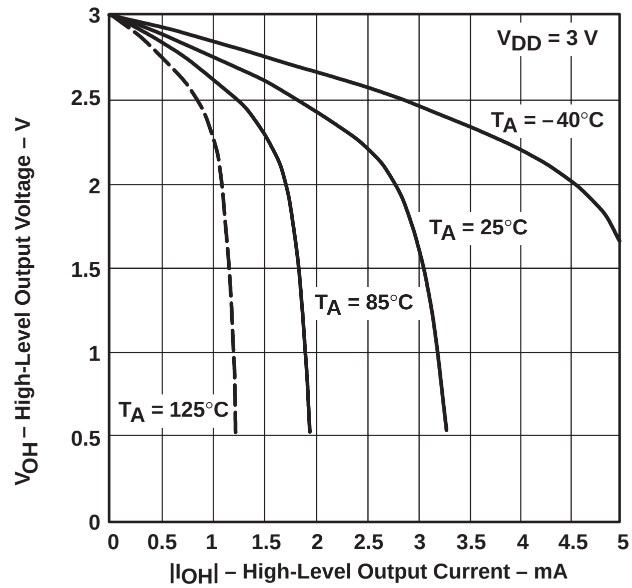


Figure 10

LOW-LEVEL OUTPUT VOLTAGE‡ vs LOW-LEVEL OUTPUT CURRENT

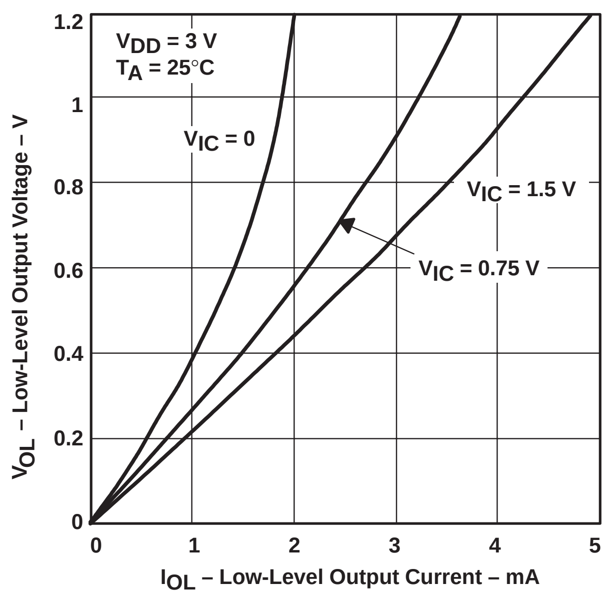


Figure 11

LOW-LEVEL OUTPUT VOLTAGE†‡ vs LOW-LEVEL OUTPUT CURRENT

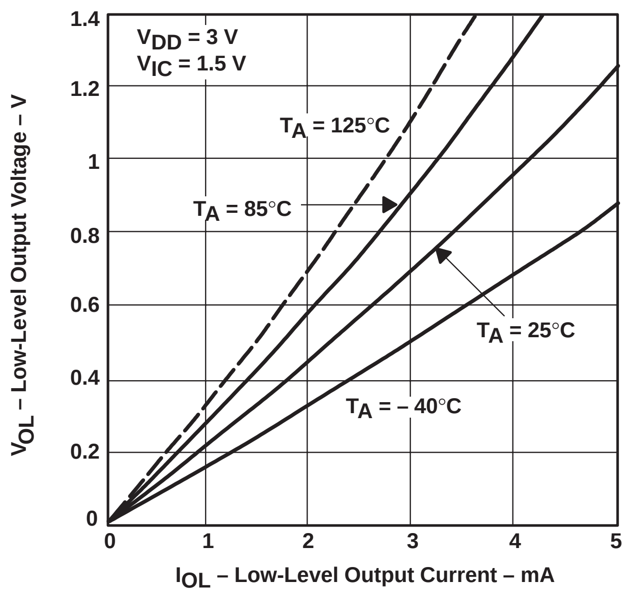


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

**HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT**

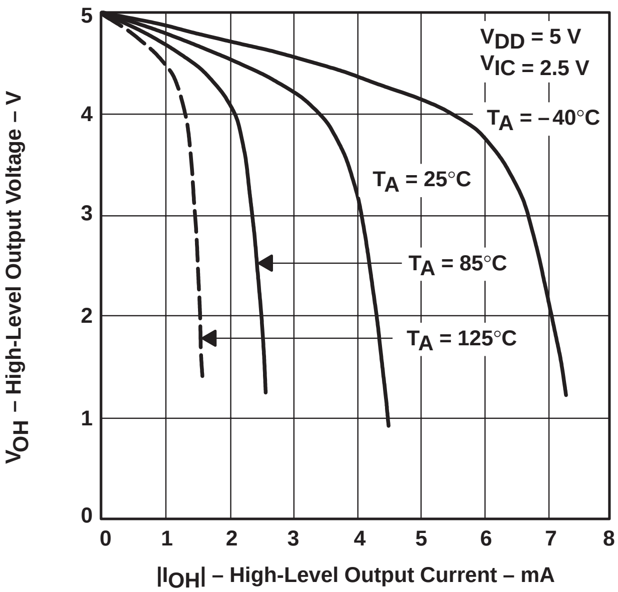


Figure 13

**LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT**

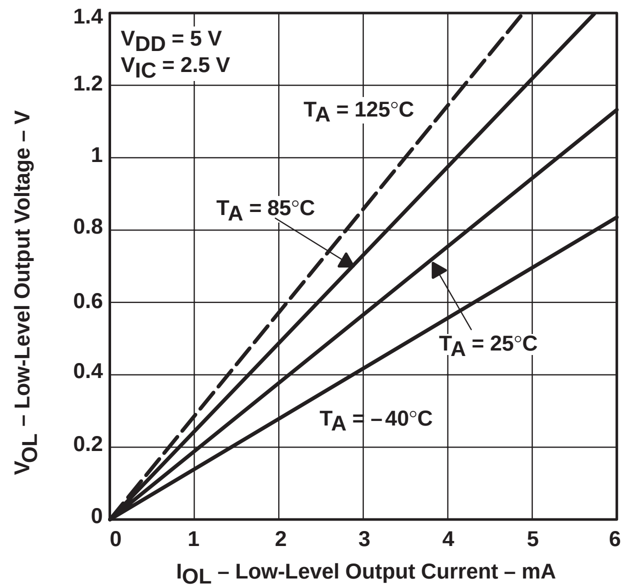


Figure 14

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡
vs
FREQUENCY**

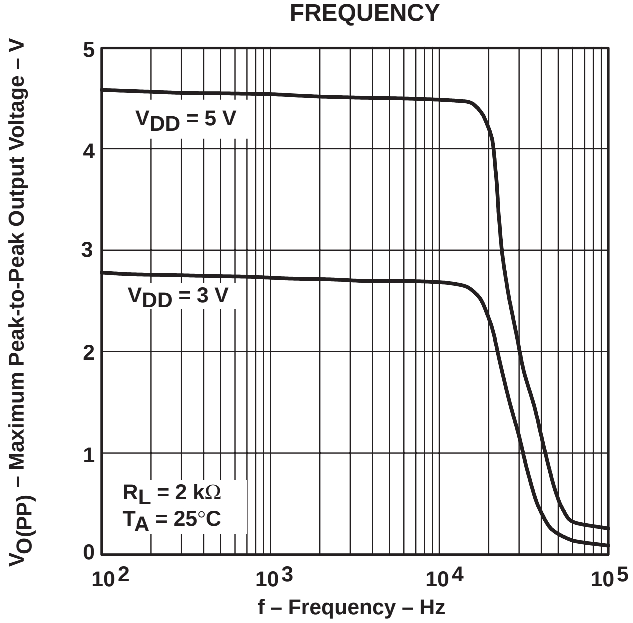


Figure 15

**SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE**

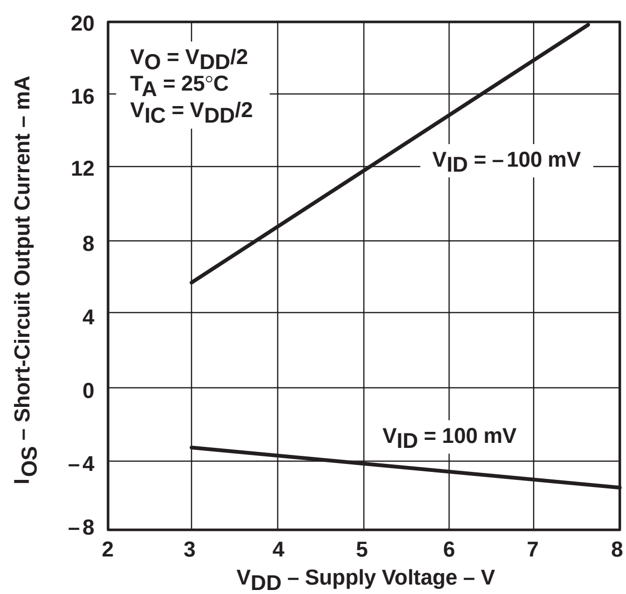


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

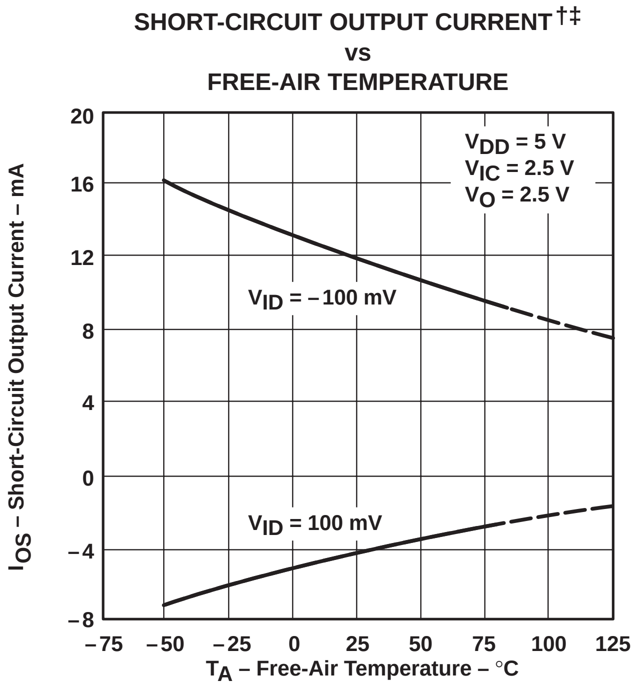


Figure 17

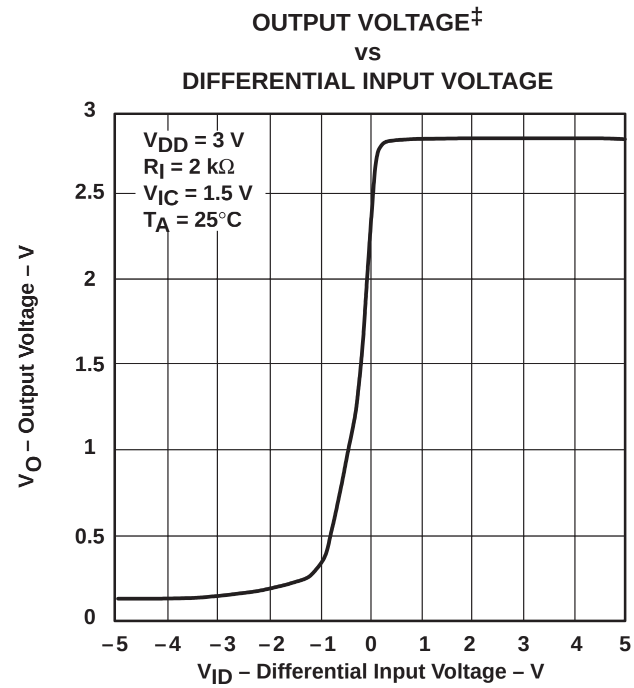


Figure 18

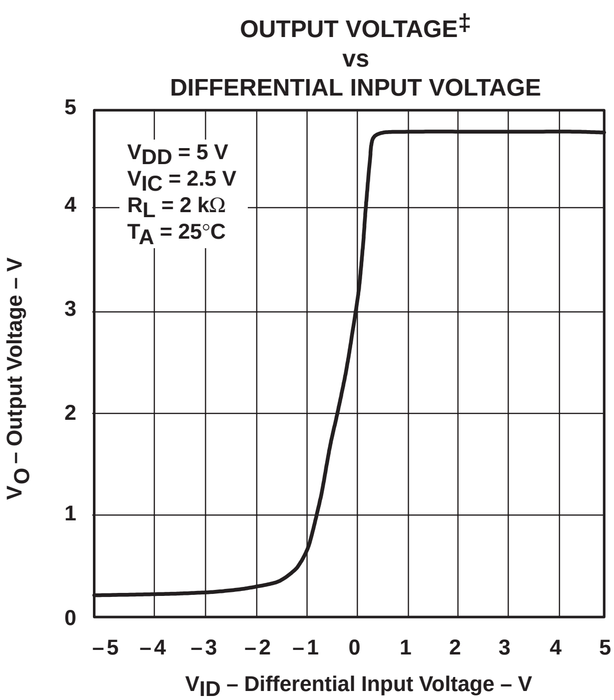


Figure 19

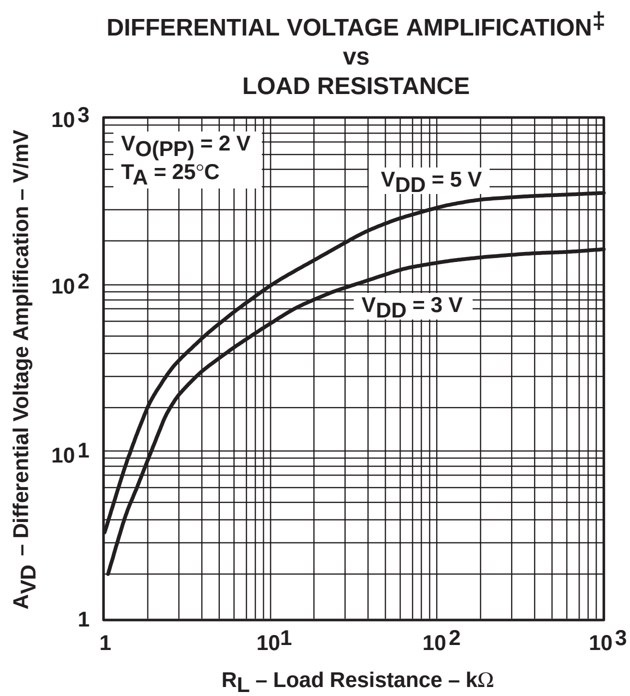


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

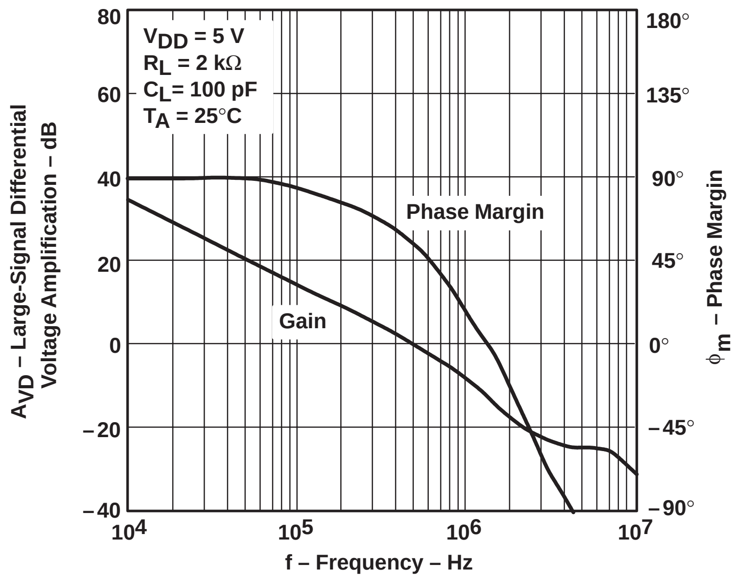


Figure 21

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN† vs FREQUENCY

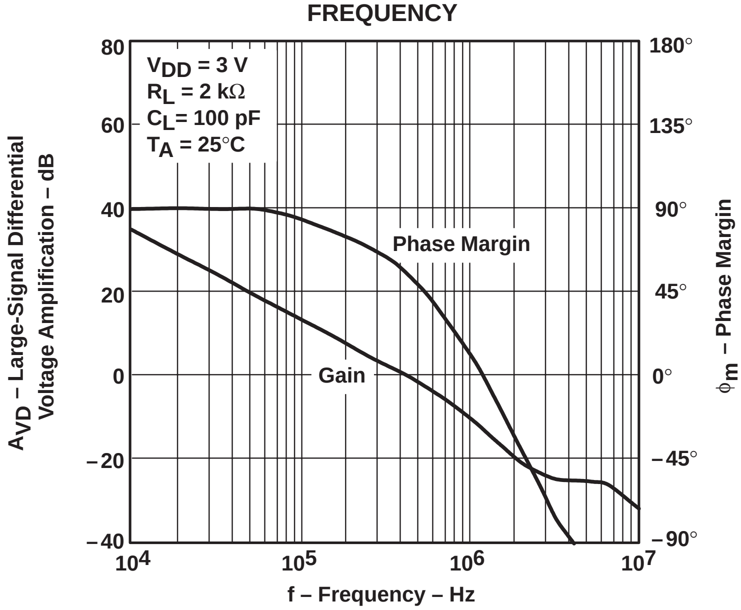


Figure 22

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

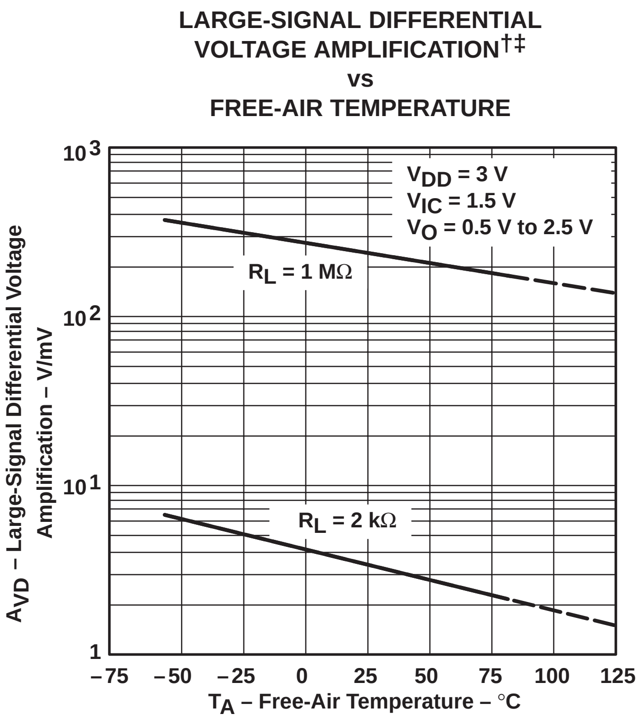


Figure 23

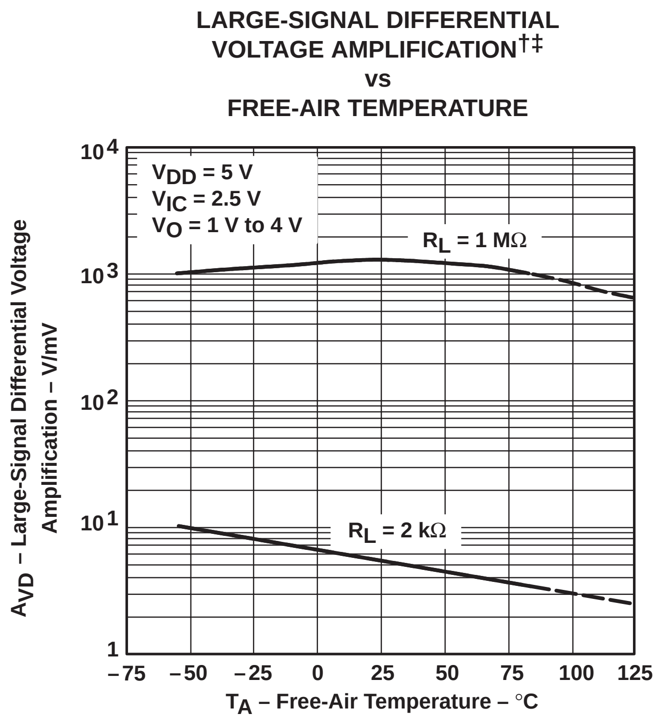


Figure 24

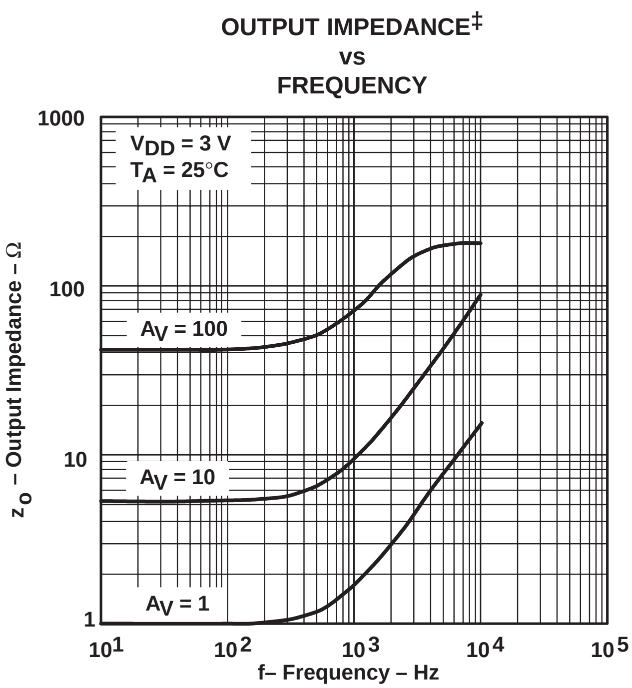


Figure 25

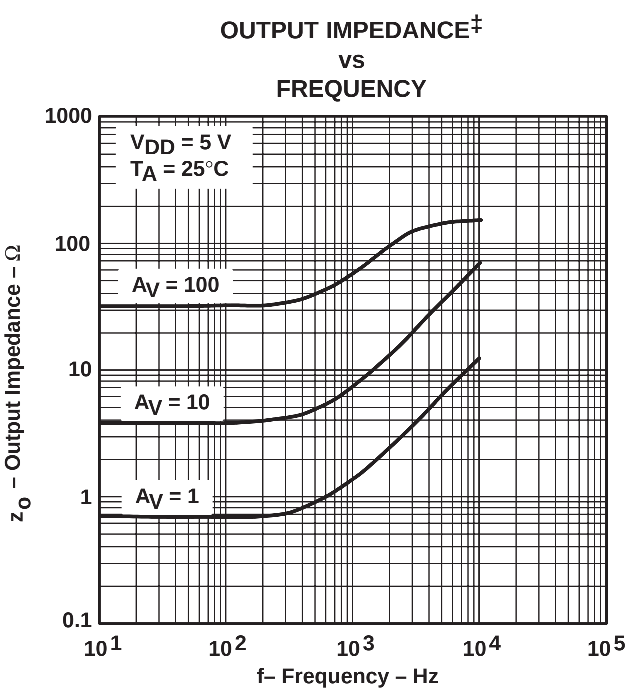


Figure 26

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO† vs FREQUENCY

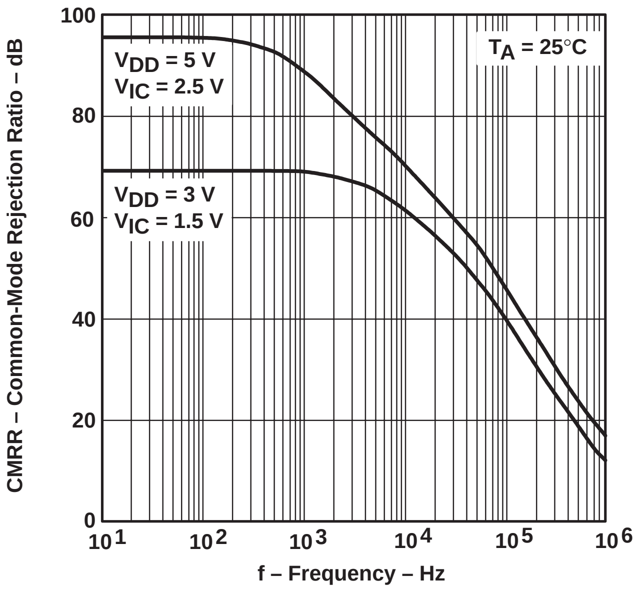


Figure 27

COMMON-MODE REJECTION RATIO†‡ vs FREE-AIR TEMPERATURE

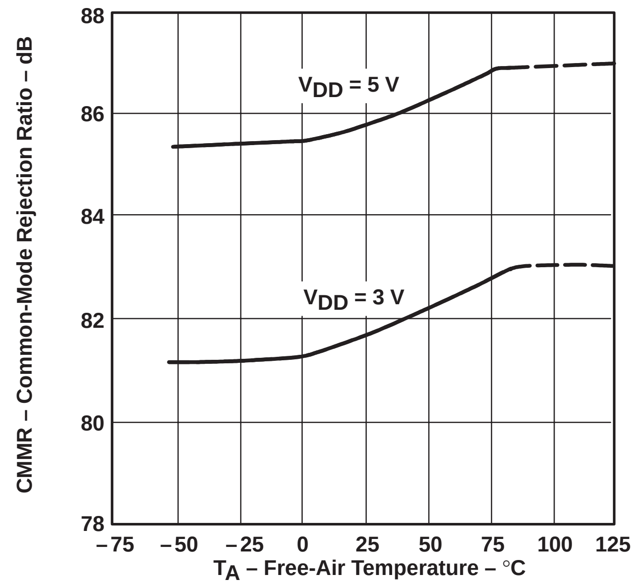


Figure 28

SUPPLY-VOLTAGE REJECTION RATIO† vs FREQUENCY

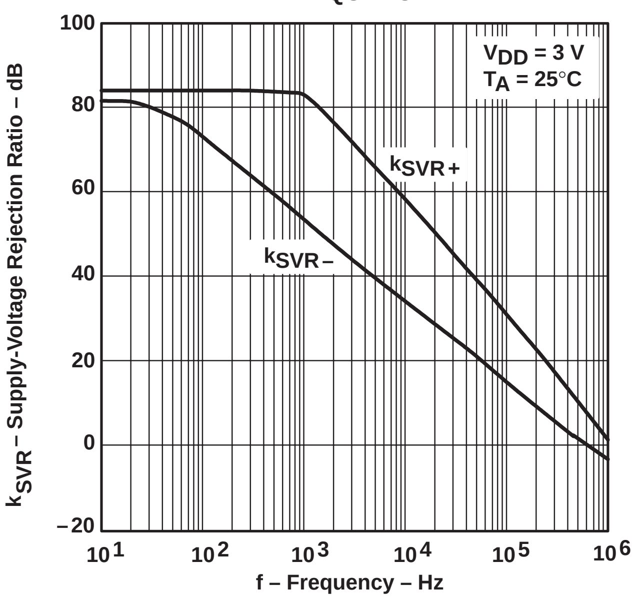


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO† vs FREQUENCY

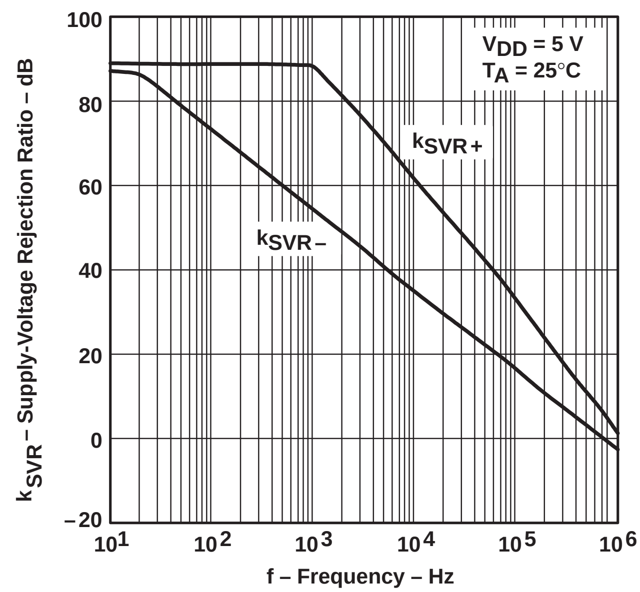


Figure 30

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

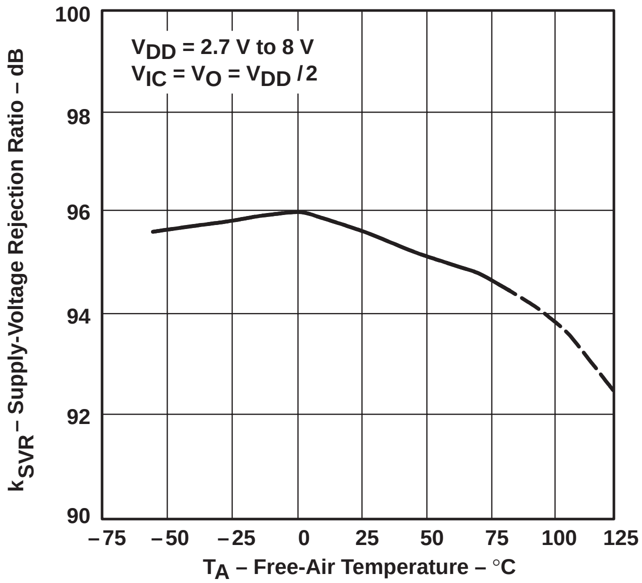


Figure 31

SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

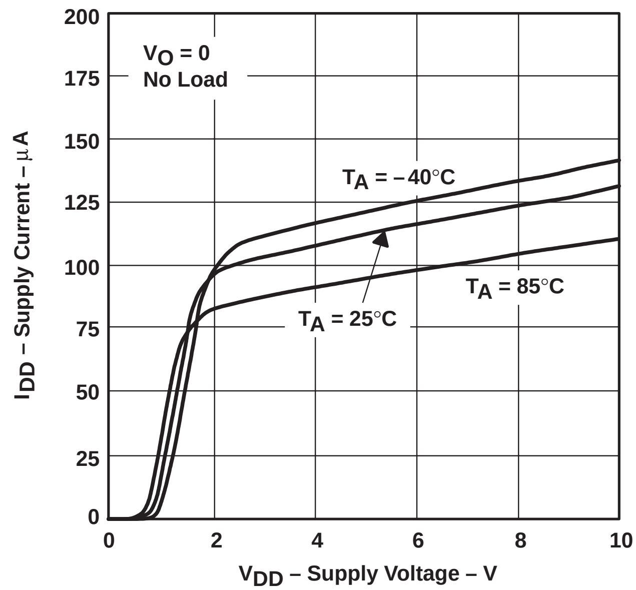


Figure 32

SLEW RATE‡
vs
LOAD CAPACITANCE

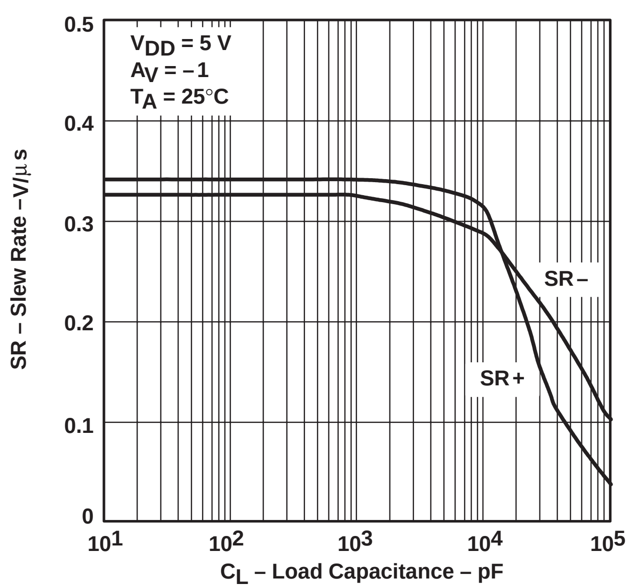


Figure 33

SLEW RATE†‡
vs
FREE-AIR TEMPERATURE

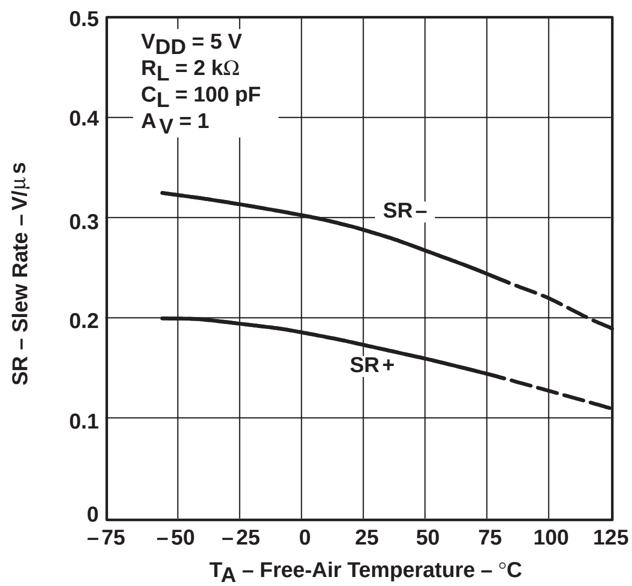


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE†

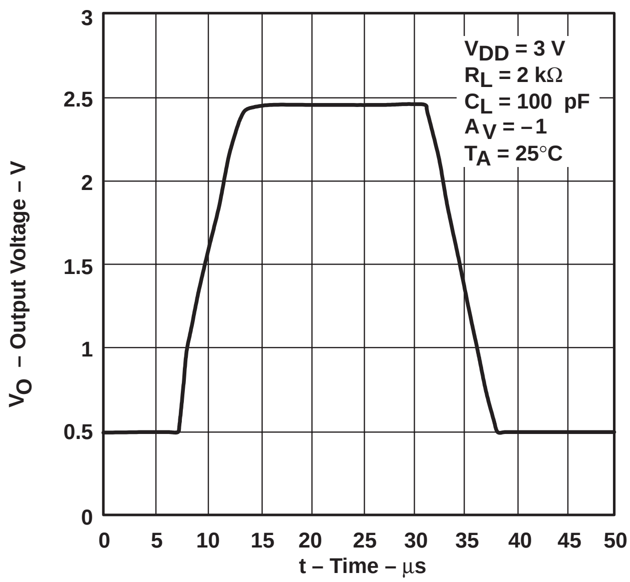


Figure 35

INVERTING LARGE-SIGNAL PULSE RESPONSE†

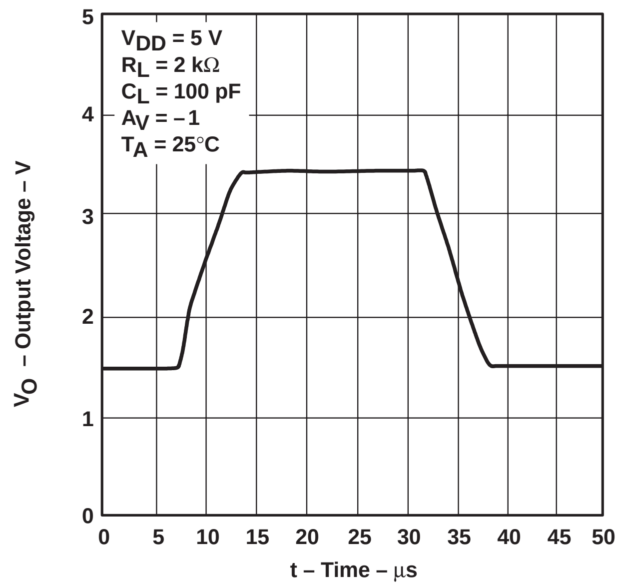


Figure 36

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

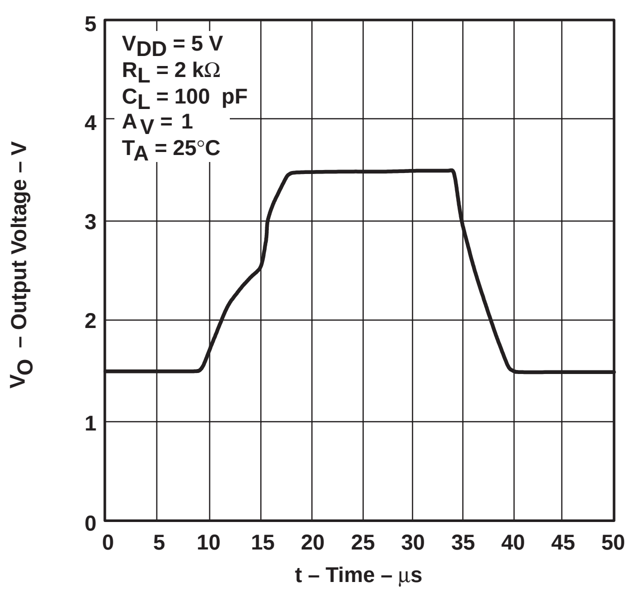


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

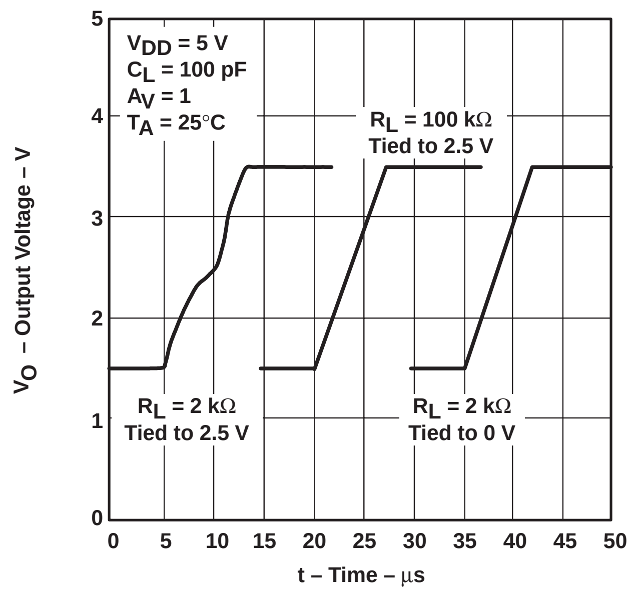


Figure 38

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE†

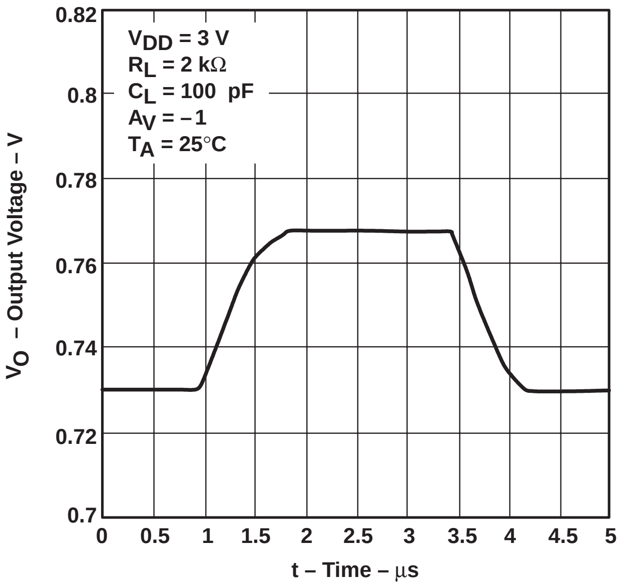


Figure 39

INVERTING SMALL-SIGNAL PULSE RESPONSE†

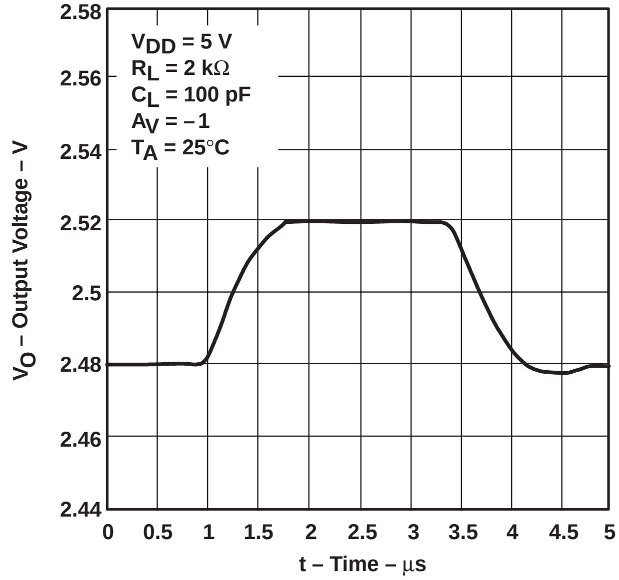


Figure 40

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

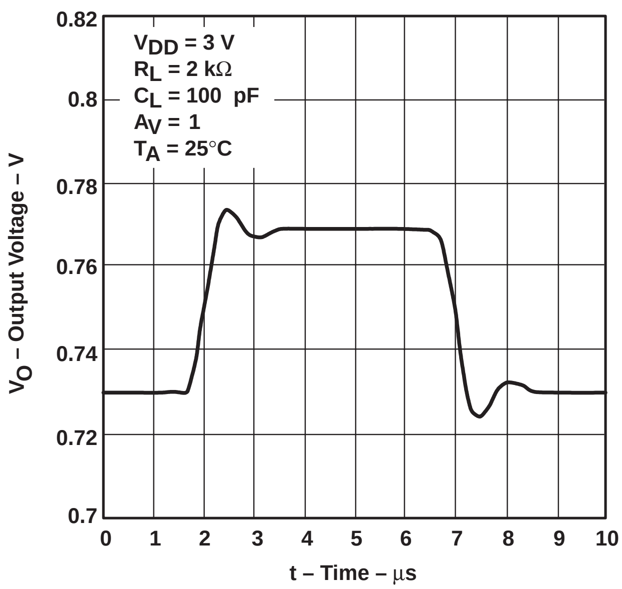


Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

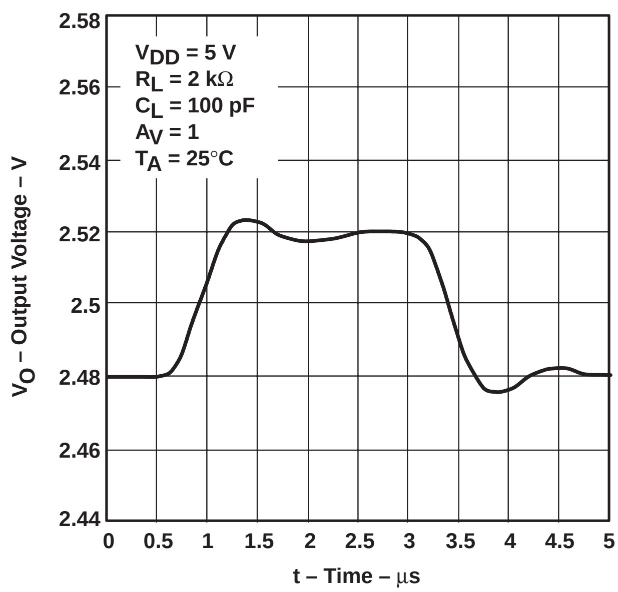


Figure 42

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE† vs FREQUENCY

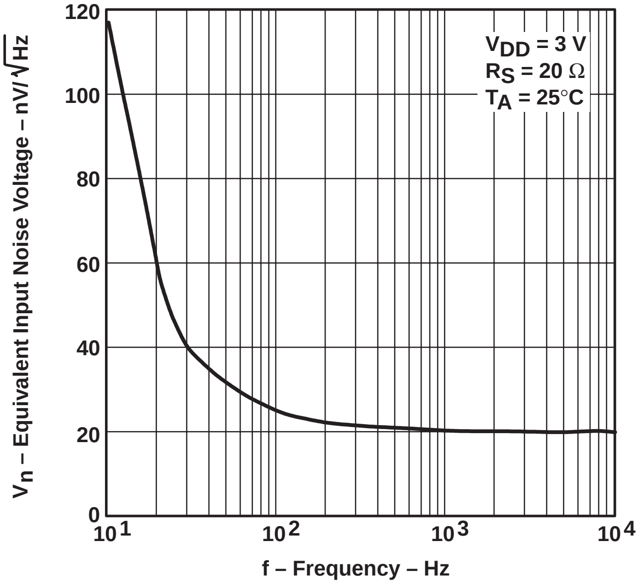


Figure 43

EQUIVALENT INPUT NOISE VOLTAGE† vs FREQUENCY

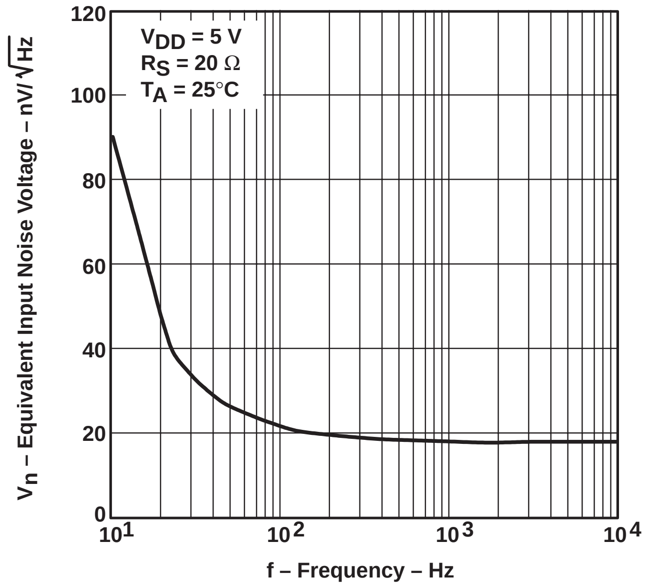


Figure 44

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD†

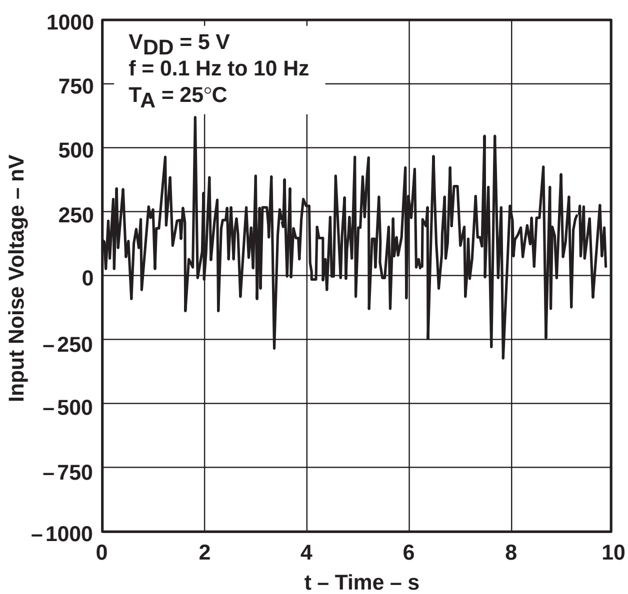


Figure 45

TOTAL HARMONIC DISTORTION PLUS NOISE† vs FREQUENCY

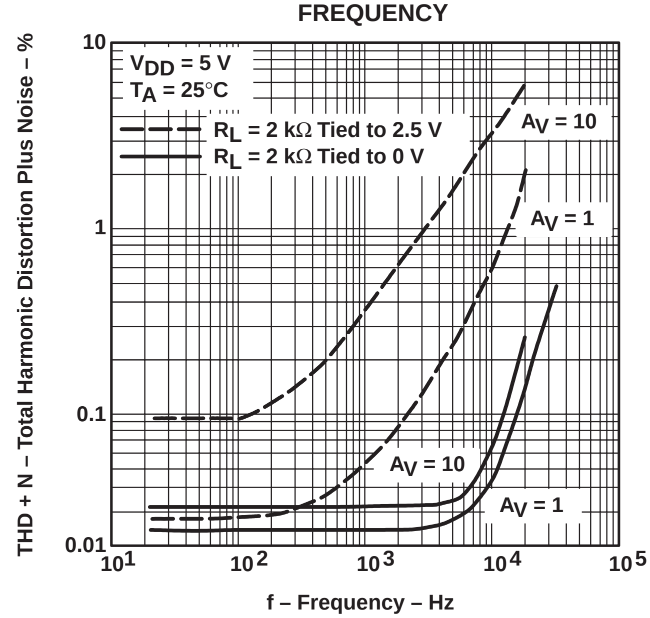


Figure 46

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE

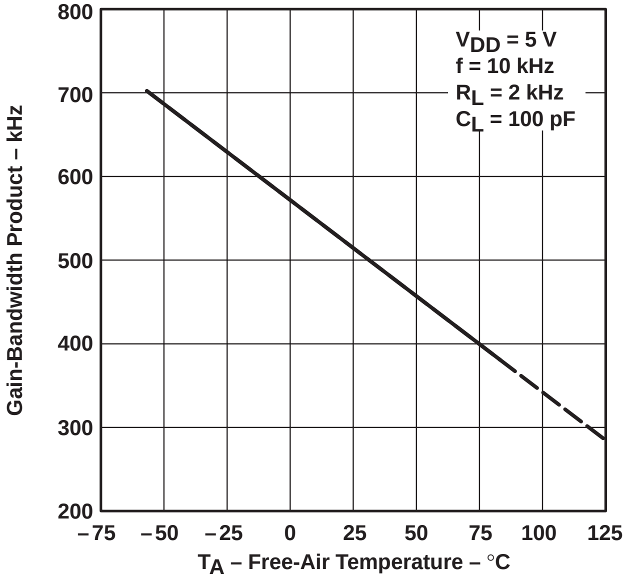


Figure 47

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

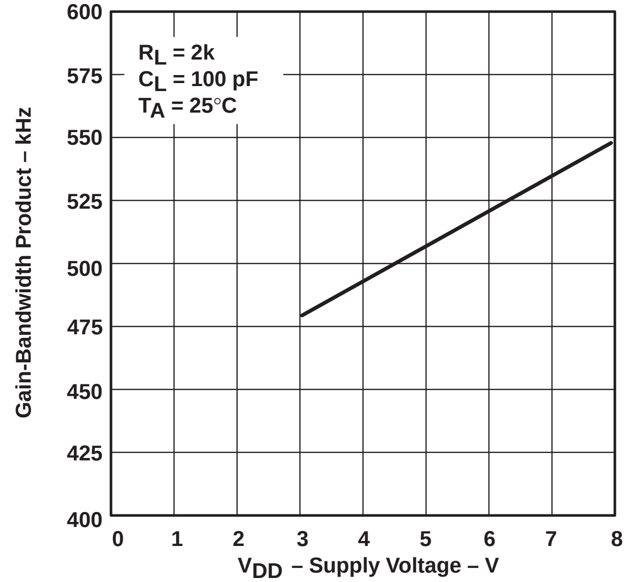


Figure 48

GAIN MARGIN
vs
LOAD CAPACITANCE

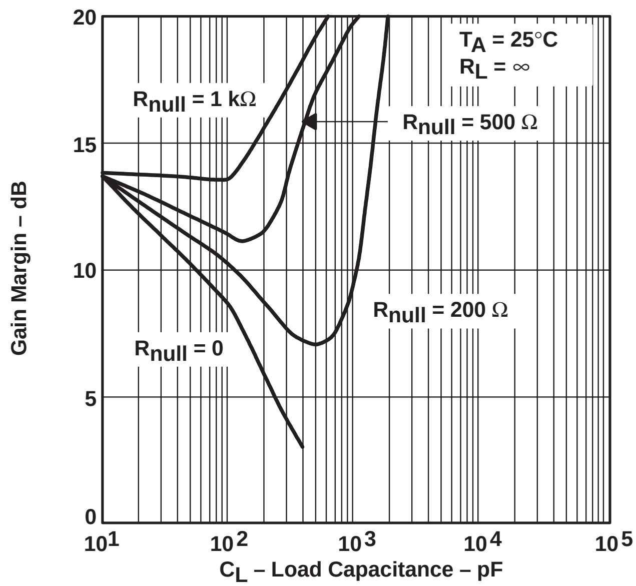


Figure 49

GAIN MARGIN
vs
LOAD CAPACITANCE

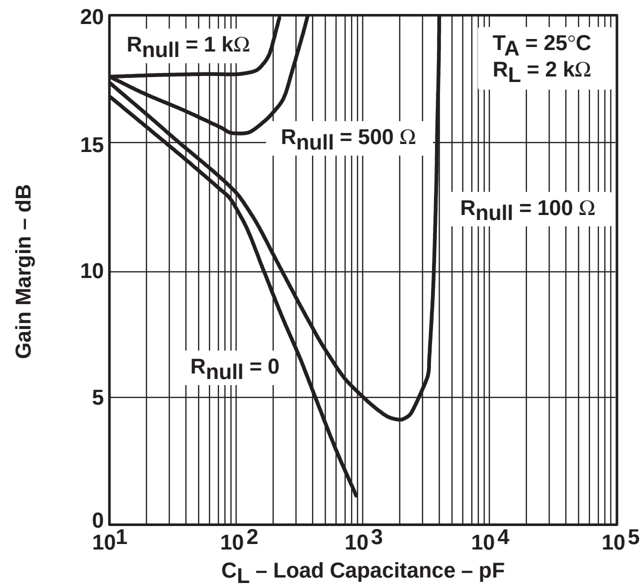


Figure 50

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

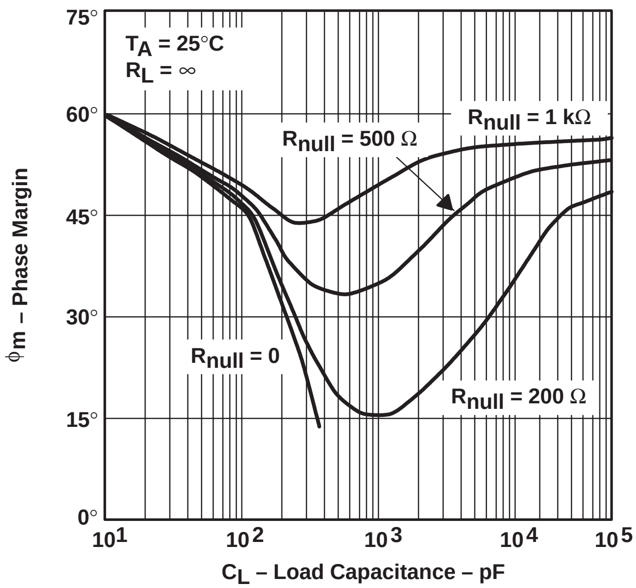


Figure 51

PHASE MARGIN
vs
LOAD CAPACITANCE

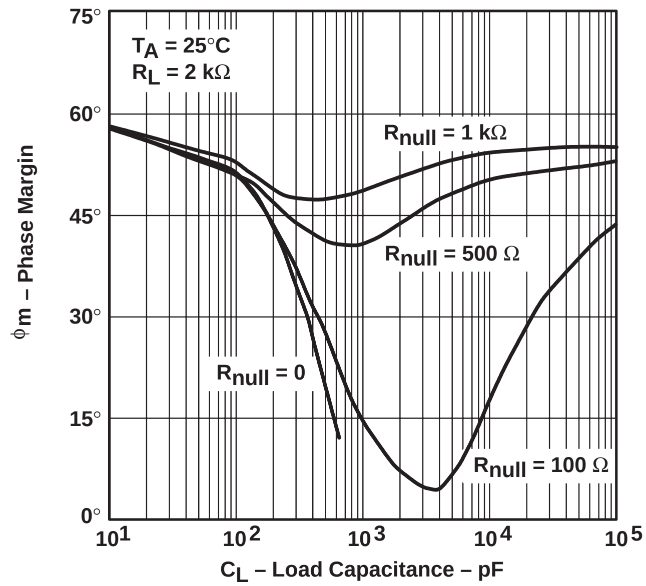


Figure 52

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

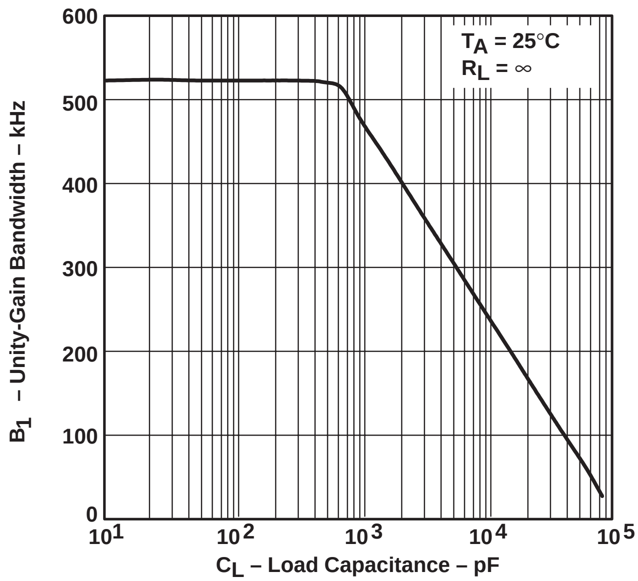


Figure 53

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

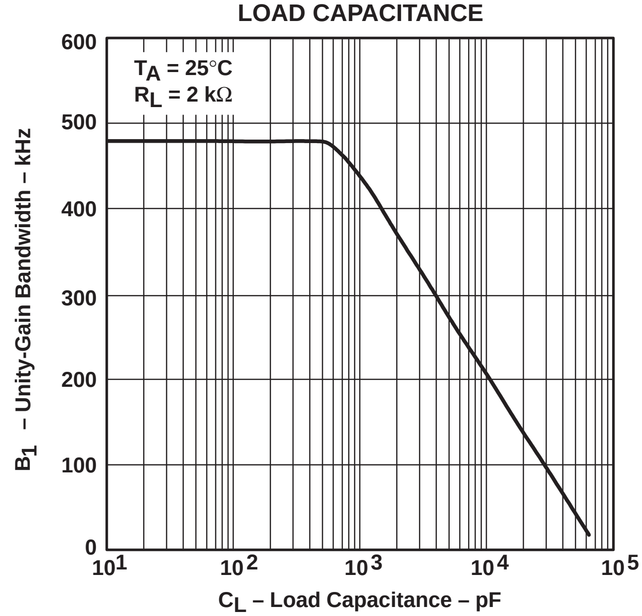


Figure 54

APPLICATION INFORMATION

driving large capacitive loads

The TLV2221 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 49 through Figure 54 illustrate its ability to drive loads greater than 100 pF while maintaining good gain and phase margins (R_{null} = 0).

A small series resistor (R_{null}) at the output of the device (Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 49 through Figure 52 show the effects of adding series resistances of 100 Ω, 200 Ω, 500 Ω, and 1 kΩ. The addition of this series resistor has two effects: the first effect is that it adds a zero to the transfer function and the second effect is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the approximate improvement in phase margin, equation (1) can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \qquad (1)$$

where :

$\Delta\phi_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (Figure 53 and Figure 54). To use equation (1), UGBW must be approximated from Figure 53 and Figure 54.

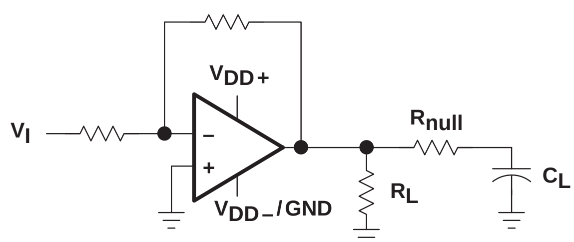


Figure 55. Series-Resistance Circuit

The TLV2221 is designed to provide better sinking and sourcing output currents than earlier CMOS rail-to-rail output devices. This device is specified to sink 500 μA and source 1 mA at V_{DD} = 5 V at a maximum quiescent I_{DD} of 200 μA. This provides a greater than 80% power efficiency.

When driving heavy dc loads, such as 2 kΩ, the positive edge under slewing conditions can experience some distortion. This condition can be seen in Figure 37. This condition is affected by three factors:

- Where the load is referenced. When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 38 illustrates two 2-kΩ load conditions. The first load condition shows the distortion seen for a 2-kΩ load tied to 2.5 V. The third load condition in Figure 38 shows no distortion for a 2-kΩ load tied to 0 V.
- Load resistance. As the load resistance increases, the distortion seen on the output decreases. Figure 38 illustrates the difference seen on the output for a 2-kΩ load and a 100-kΩ load with both tied to 2.5 V.
- Input signal edge rate. Faster input edge rates for a step input result in more distortion than with slower input edge rates.

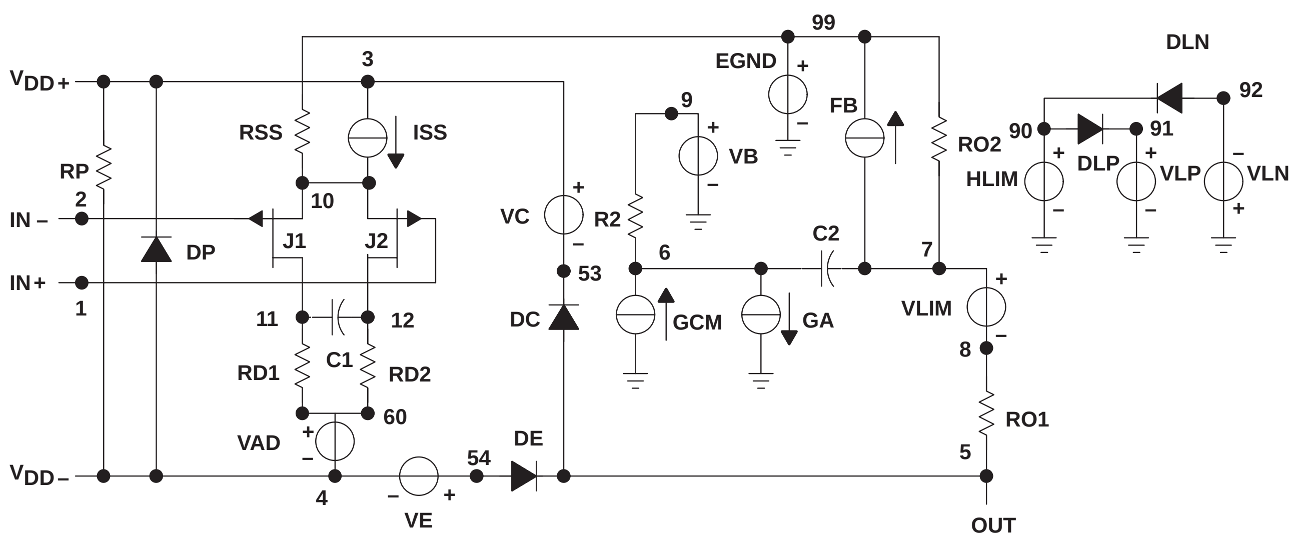
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 56 are generated using the TLV2221 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).



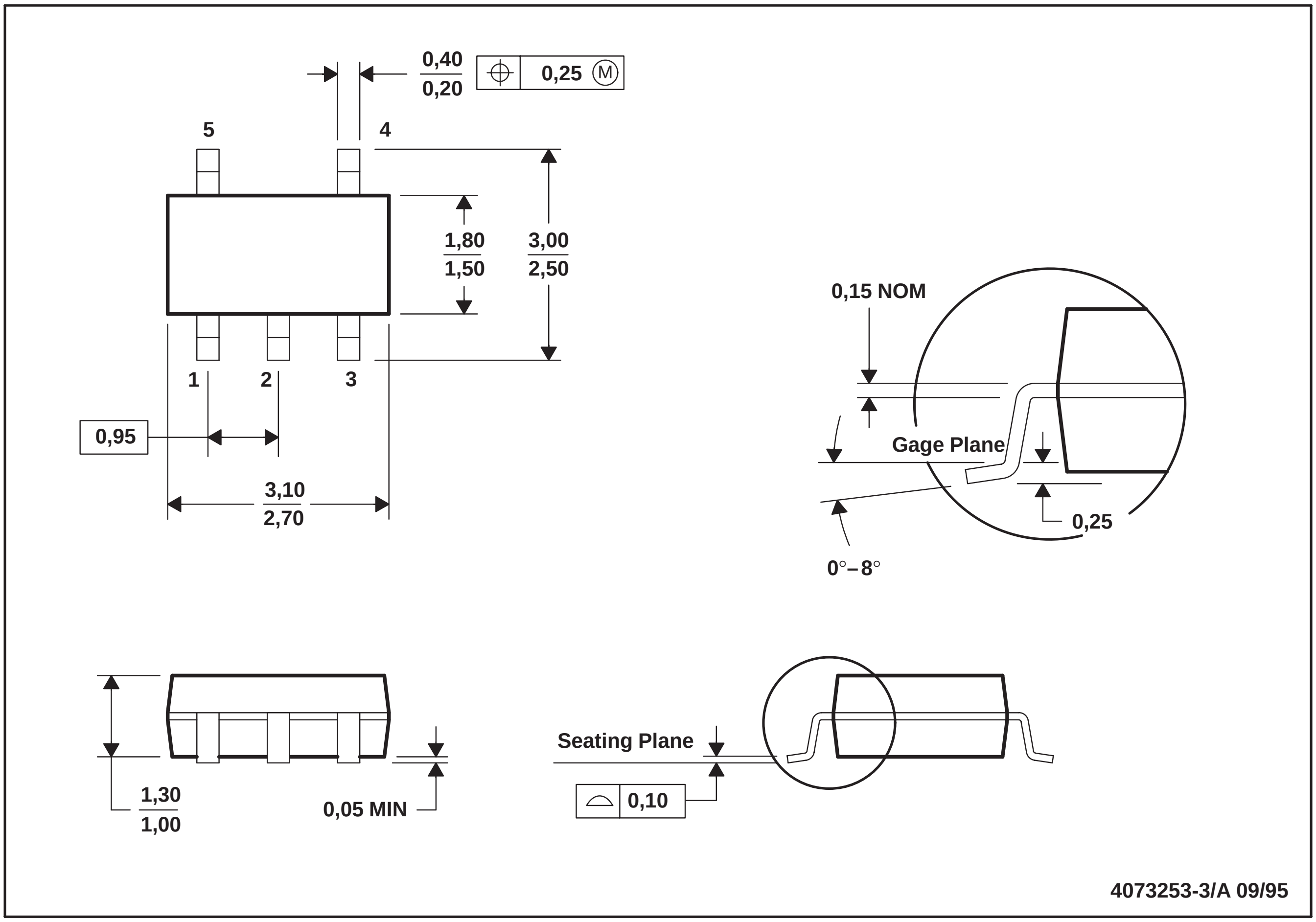

```
.SUBCKT TLV2221 1 2 3 4 5
     C1      11    12    12.53E–12
     C2      6     7     50.00E–12
     DC      5     53    DX
     DE      54    5     DX
     DLP     90    91    DX
     DLN     92    90    DX
     DP      4     3     DX
     EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
     FB      7     99    POLY (5) VB VC VE VLP
     + VLN 0 893.6E3 –90E3 90E3 90E3 –90E3
     GA      6     0     11    12 94.25E–6
     GCM     0     6     10    99 9.300E–9
     ISS     3     10    DC 9.000E–6
     HLIM    90    0     VLIM 1K
     J1      11    2     10 JX
     J2      12    1     10 JX
     R2      6     9     100.0E3
RD1     60    11    10.61E3
RD2     60    12    10.61E3
R01     8     5     35
R02     7     99    35
RP      3     4     49.50E3
RSS     10    99    22.22E6
VAD     60    4     –.5
VB      9     0     DC 0
VC      3     53    DC .666
VE      54    4     DC .666
VLIM    7     8     DC 0
VLP     91    0     DC 3.4
VLN     0     92    DC 11.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=1.527E–3
+ VTO=–.001)
.ENDS
```

Figure 56. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademark of MicroSim Corporation.

MECHANICAL INFORMATION

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

IMPORTANT NOTICE