

LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

TLV2352, TLV2352Y

SLCS011B – MAY 1992 – REVISED MARCH 1999

- **Wide Range of Supply Voltages**
2 V to 8 V
- **Fully Characterized at 3 V and 5 V**
- **Very-Low Supply-Current Drain**
120 μ A Typ at 3 V
- **Output Compatible With TTL, MOS, and CMOS**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **High Input Impedance . . . $10^{12} \Omega$ Typ**
- **Extremely Low Input Bias Current**
5 pA Typ
- **Common-Mode Input Voltage Range Includes Ground**
- **Built-In ESD Protection**

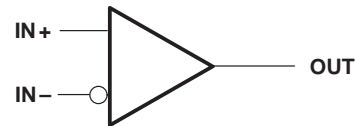
description

The TLV2352 consists of two independent, low-power comparators specifically designed for single power-supply applications and operates with power-supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 120 μ A.

The TLV2352 is designed using the Texas Instruments LinCMOS™ technology and therefore features an extremely high input impedance (typically greater than $10^{12} \Omega$), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2352I is fully characterized at 3 V and 5 V for operation from -40°C to 85°C . The TLV2352M is fully characterized at 3 V and 5 V for operation from -55°C to 125°C .

The TLV2352 has internal electrostatic-discharge (ESD)-protection circuits and has been classified with a 1000-V ESD rating using Human Body Model testing. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

symbol (each comparator)



AVAILABLE OPTIONS

T _A	V _{IO} max at 25°C	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D) [†]	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW) [‡]	PLASTIC DIP (U)	
-40°C to 85°C	5 mV	TLV2352ID	—	—	TLV2352IP	TLV2352IPWLE	—	TLV2352Y
-55°C to 125°C	5 mV	—	TLV2352MFK	TLV2352MJG	—	—	TLV2352MU	

[†] The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR).

[‡] The PW packages are only available left-ended taped and reeled (e.g., TLV2352IPWLE)



These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

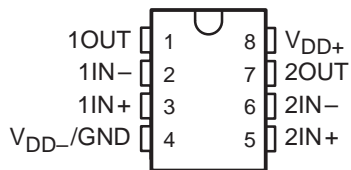
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

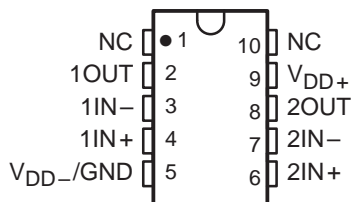
TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

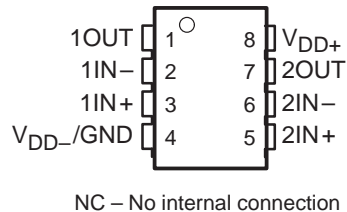
**TLV2352I . . . D OR P PACKAGE
TLV2352M . . . JG PACKAGE
(TOP VIEW)**



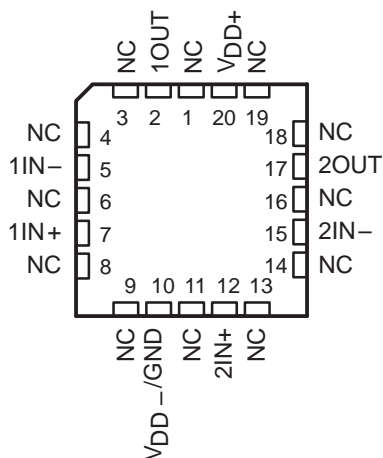
**TLV2254M
U PACKAGE
(TOP VIEW)**



**TLV2352I . . . PW PACKAGE
(TOP VIEW)**

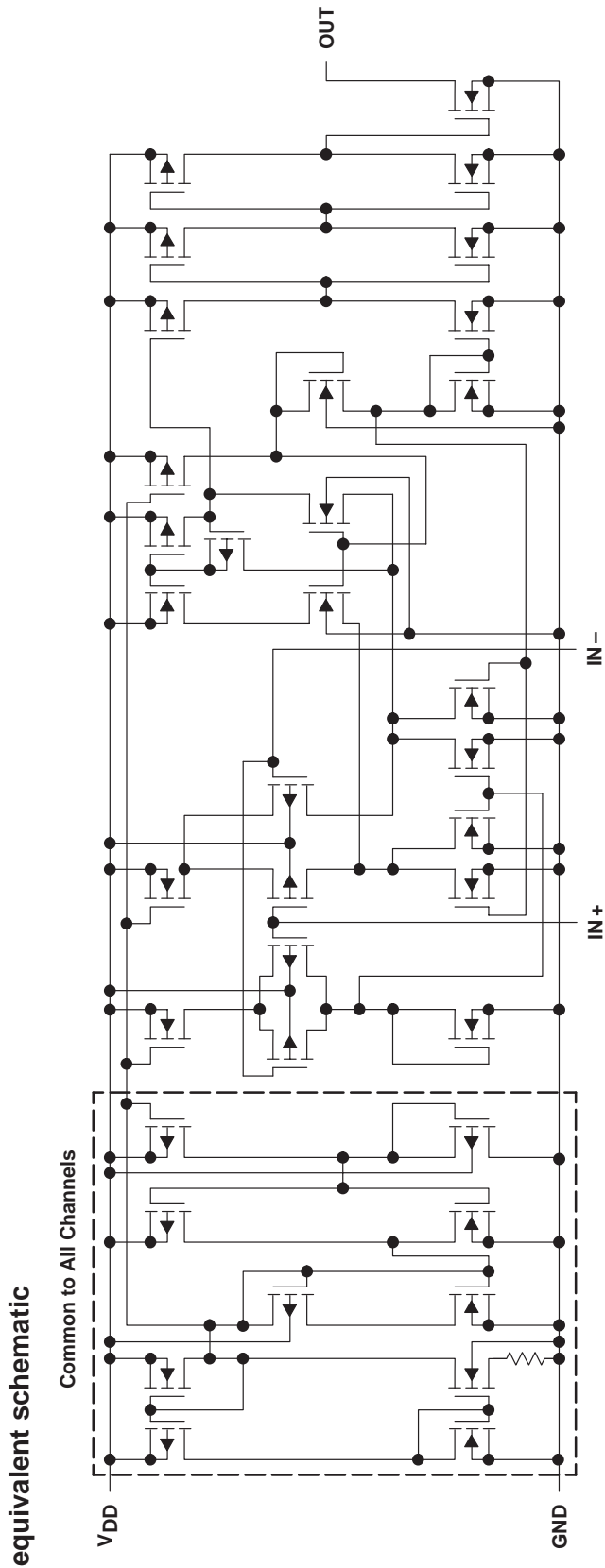


**TLV2352M
FK PACKAGE
(TOP VIEW)**



TLV2352, TLV2352Y
LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

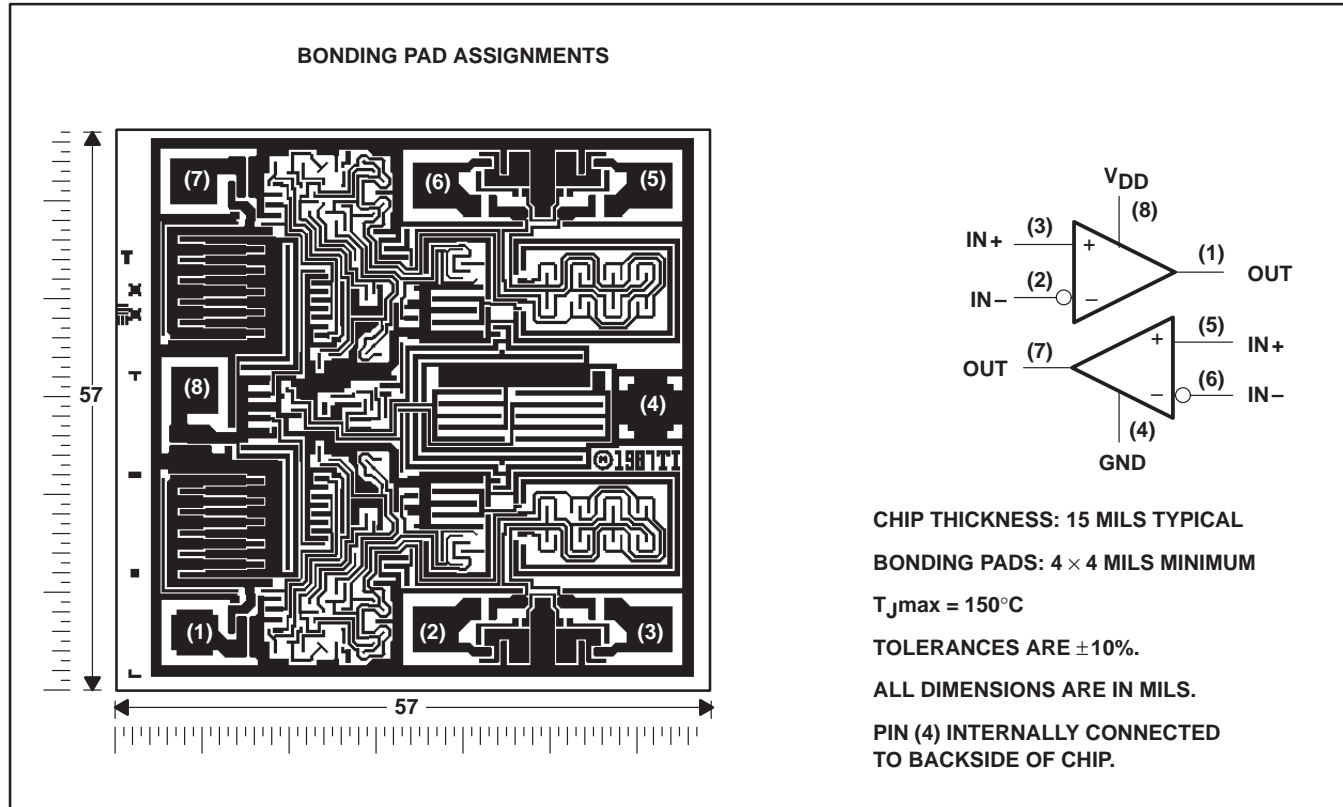


TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

TLV2352Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2352. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip can be mounted with conductive epoxy or a gold-silicon preform.



TLV2352, TLV2352Y

LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	8 V
Differential input voltage, V_{ID} (see Note 2)	± 8 V
Input voltage range, V_I	–0.3 to 8 V
Output voltage, V_O	8 V
Input current, I_I	± 5 mA
Output current, I_O	20 mA
Duration of output short-circuit current to GND (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : TLV2352I	–40°C to 85°C
TLV2352M	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, and PW Packages	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FK, JG, and U Packages	300°C

† Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 2. Differential voltages are at IN+ with respect to IN–.
 3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW	—
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	546 mW	210 mW
P	1000 mW	8.0 mW/°C	520 mW	—
PW	525 mW	4.2 mW/°C	273 mW	—
U	700 mW	5.5 mW/°C	370 mW	150 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	$V_{DD} = 3$ V	0	1.75	V
	$V_{DD} = 5$ V	0	3.75	
Operating free-air temperature, T_A	TLV2352I	–40	85	°C
	TLV2352M	–55	125	



TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

electrical characteristics at specified free-air temperature†

PARAMETER	TEST CONDITIONS	T _A ‡	TLV2352I						UNIT
			V _{DD} = 3 V			V _{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO} Input offset voltage	V _{IC} = V _{ICRmin} , See Note 4	25°C	1		5	1		5	mV
		Full range	7			7			
I _{IO} Input offset current		25°C	1			1			pA
		85°C			1			1	nA
I _{IB} Input bias current		25°C	5			5			pA
		85°C			2			2	nA
V _{ICR} Common-mode input voltage range		25°C	0 to 2			0 to 4			V
		Full range	0 to 1.75			0 to 3.75			
I _{OH} High-level output current	V _{ID} = 1 V	25°C	0.1			0.1			nA
		Full range	1			1			μA
V _{OL} Low-level output voltage	V _{ID} = -1 V, I _{OL} = 2 mA	25°C	115		300	150		400	mV
		Full range	600			700			
I _{OL} Low-level output current	V _{ID} = -1 V, V _{OL} = 1.5 V	25°C	6	16		6	16		mA
I _{DD} Supply current	V _{ID} = 1 V, No load	25°C	120		250	140		300	μA
		Full range	350			400			

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.

‡ Full range is -40°C to 85°C. IMPORTANT: See *Parameter Measurement Information*.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2352I			UNIT
		MIN	TYP	MAX	
Response time	R _L = 5.1 kΩ, C _L = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive		640	ns

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2352I			UNIT
		MIN	TYP	MAX	
Response time	R _L = 5.1 kΩ, C _L = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive		650	ns
		TTL-level input step		200	

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.



TLV2352, TLV2352Y

LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

electrical characteristics at specified free-air temperature†

PARAMETER	TEST CONDITIONS	T _A ‡	TLV2352M						UNIT
			V _{DD} = 3 V			V _{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO} Input offset voltage	V _{IC} = V _{ICRmin} , See Note 4	25°C	1		5	1		5	mV
		Full range				10			
I _{IO} Input offset current		25°C	1			1			pA
		125°C				10			nA
I _{IB} Input bias current		25°C	5			5			pA
		125°C				20			nA
V _{ICR} Common-mode input voltage range		25°C	0 to 2			0 to 4			V
		Full range	0 to 1.75			0 to 3.75			
I _{OH} High-level output current	V _{ID} = 1 V	25°C	0.1			0.1			nA
		Full range				1			μA
V _{OL} Low-level output voltage	V _{ID} = -1 V, I _{OL} = 2 mA	25°C	115		300	150		400	mV
		Full range				700			
I _{OL} Low-level output current	V _{ID} = -1 V, V _{OL} = 1.5 V	25°C	6	16		6	16	mA	
I _{DD} Supply current	V _{ID} = 1 V, No load	25°C	120		250	140		300	μA
		Full range				400			

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.

‡ Full range is -55°C to 125°C. IMPORTANT: See *Parameter Measurement Information*.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2352M			UNIT	
		MIN	TYP	MAX		
Response time	R _L = 5.1 kΩ, C _L = 100 pF§, See Note 5	100-mV input step with 5-mV overdrive			1400	ns

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2352M			UNIT	
		MIN	TYP	MAX		
Response time	R _L = 5.1 kΩ, C _L = 100 pF§, See Note 5	100-mV input step with 5-mV overdrive			1300	ns
		TTL-level input step			900	

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.



TLV2352, TLV2352Y

LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

electrical characteristics at specified free-air temperature, $T_A = 25^\circ\text{C}^\dagger$

PARAMETER	TEST CONDITIONS	TLV2352Y						UNIT
		$V_{DD} = 3\text{ V}$			$V_{DD} = 5\text{ V}$			
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = V_{ICRmin}$, See Note 4		1	5		1	5	mV
I_{IO} Input offset current			1			1		pA
I_{IB} Input bias current			5			5		pA
V_{ICR} Common-mode input voltage range		0 to 2			0 to 4			V
I_{OH} High-level output current	$V_{ID} = 1\text{ V}$		0.1			0.1		nA
V_{OL} Low-level output voltage	$V_{ID} = -1\text{ V}$, $I_{OL} = 2\text{ mA}$		115	300		150	400	mV
I_{OL} Low-level output current	$V_{ID} = -1\text{ V}$, $V_{OL} = 1.5\text{ V}$	6	16		6	16		mA
I_{DD} Supply current	$V_{ID} = 1\text{ V}$ No load		120	250		140	300	μA

[†] All characteristics are measured with zero common-mode input voltages unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with $V_{DD} = 5\text{ V}$, 2 V with $V_{DD} = 3\text{ V}$, or below 400 mV with a 10-k Ω resistor between the output and V_{DD} . They can be verified by applying the limit value to the input and checking for the appropriate output state.

TYPICAL CHARACTERISTICS

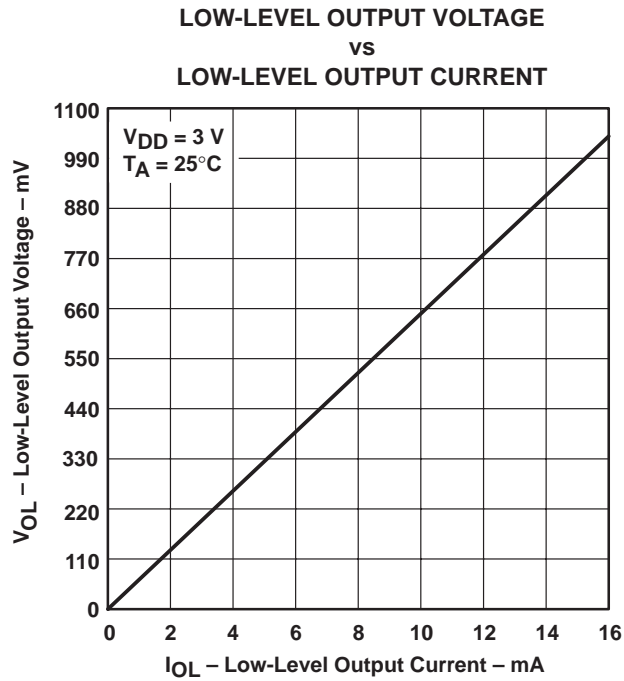


Figure 1

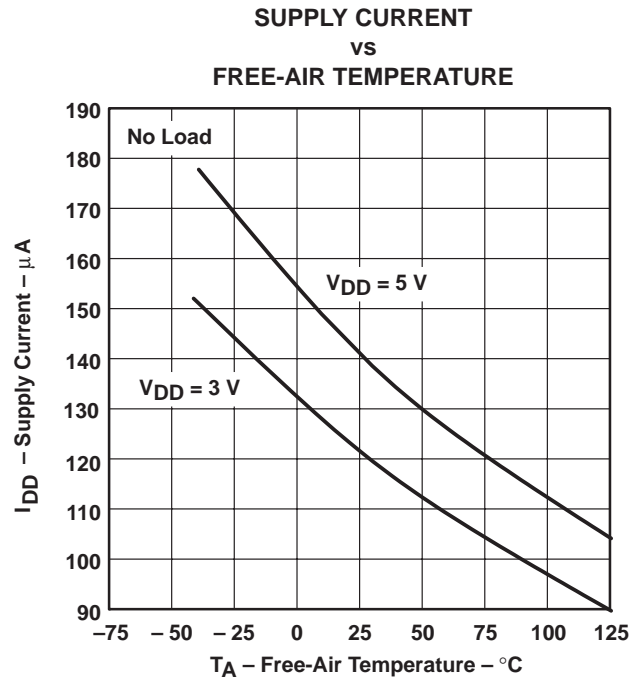


Figure 2

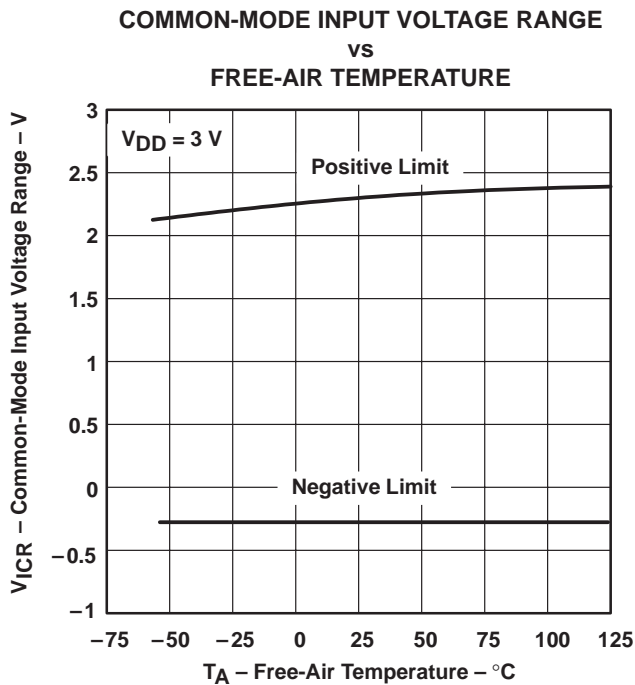


Figure 3

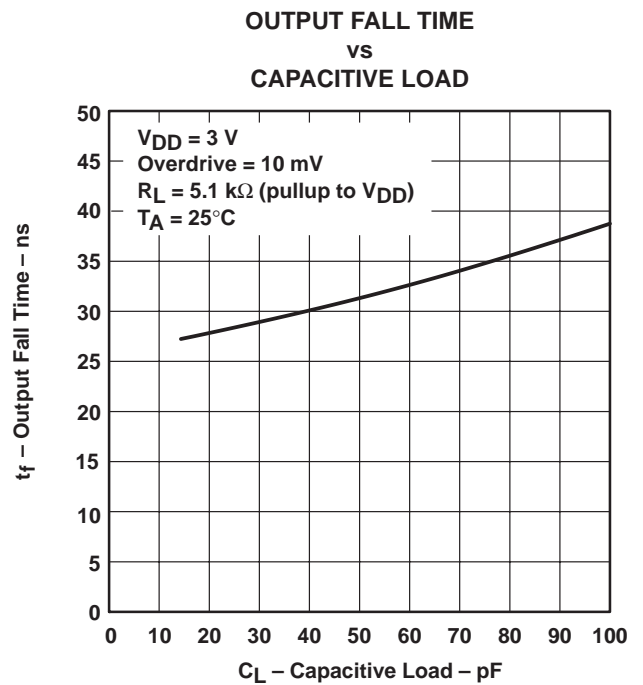


Figure 4

TYPICAL CHARACTERISTICS

HIGH-TO-LOW-LEVEL OUTPUT
 PROPAGATION DELAY
 FOR VARIOUS OVERDRIVE VOLTAGES

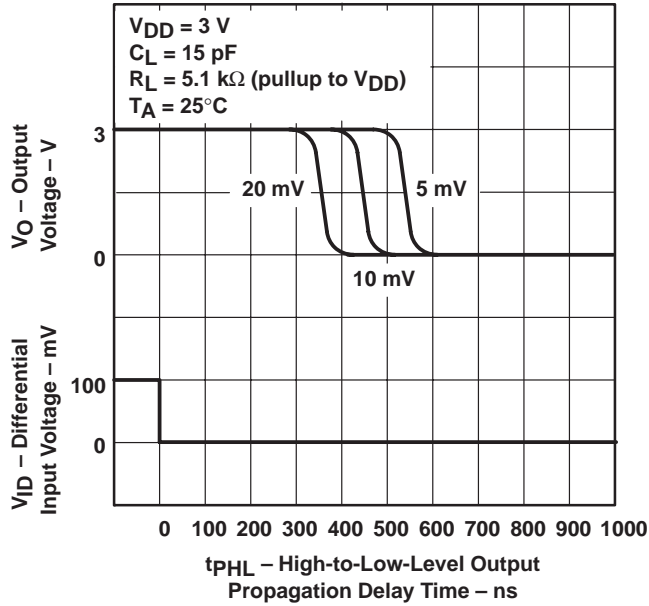


Figure 5

HIGH-TO-LOW-LEVEL OUTPUT
 PROPAGATION DELAY
 FOR VARIOUS CAPACITIVE LOADS

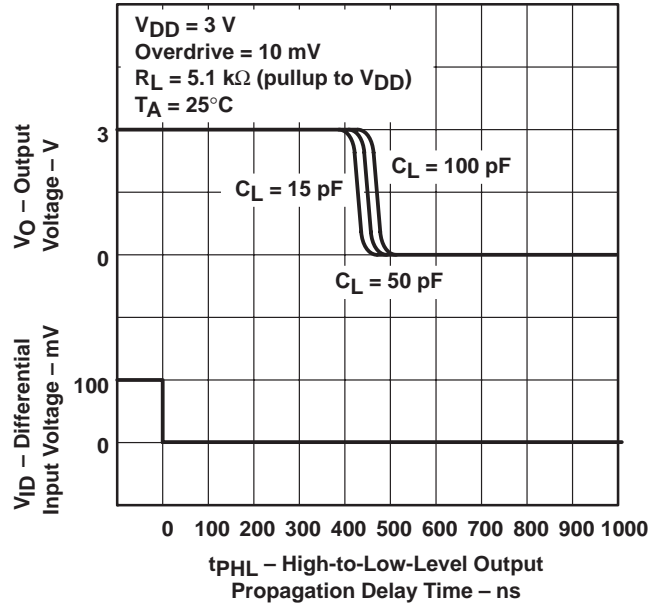


Figure 6

LOW-TO-HIGH-LEVEL OUTPUT
 PROPAGATION DELAY
 FOR VARIOUS OVERDRIVE VOLTAGES

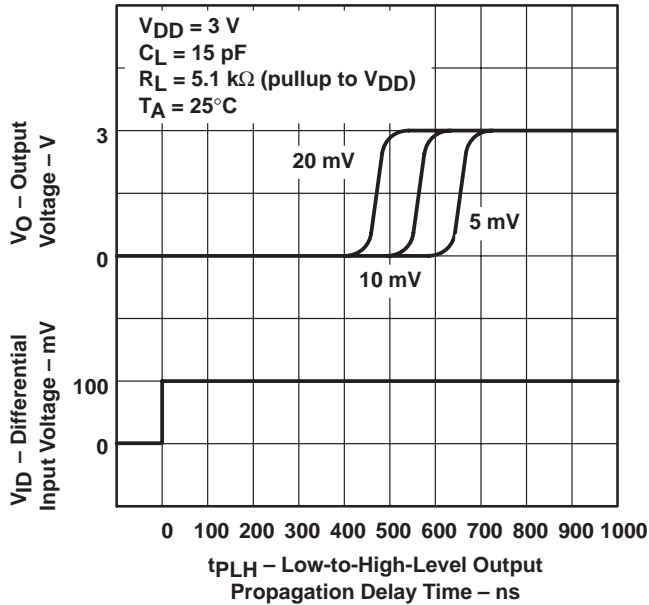


Figure 7

LOW-TO-HIGH-LEVEL OUTPUT
 PROPAGATION DELAY
 FOR VARIOUS CAPACITIVE LOADS

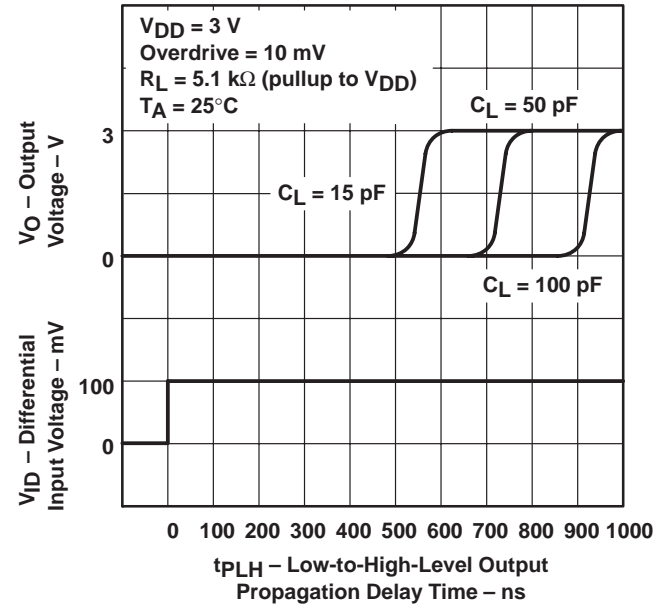


Figure 8

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLV2352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the V_{ICR} test, rather than changing the input voltages to provide greater accuracy.

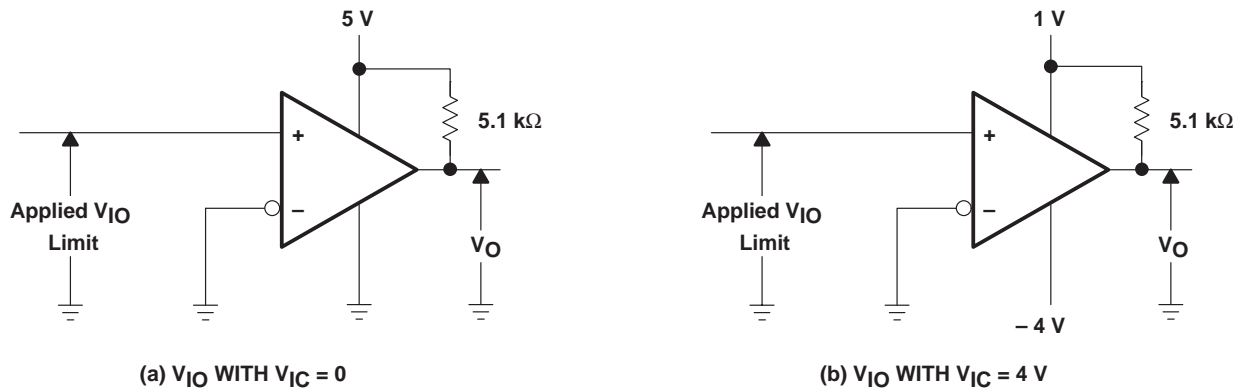
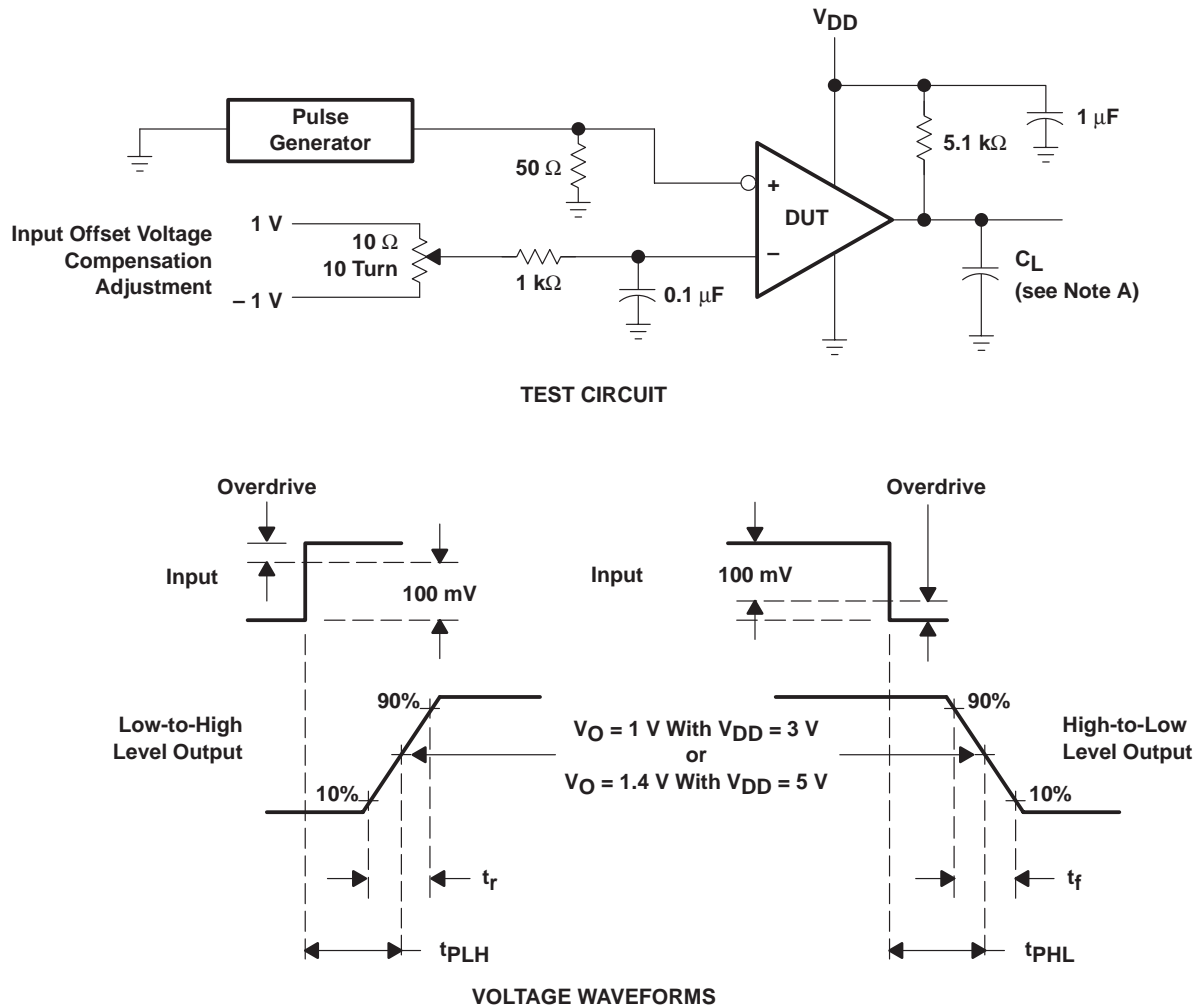


Figure 9. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes states.

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses $V_O = 1\text{ V}$ with $V_{DD} = 3\text{ V}$ or when the output crosses $V_O = 1.4\text{ V}$ with $V_{DD} = 5\text{ V}$. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 11) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change states.



NOTE A: C_L includes probe and jig capacitance.

Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

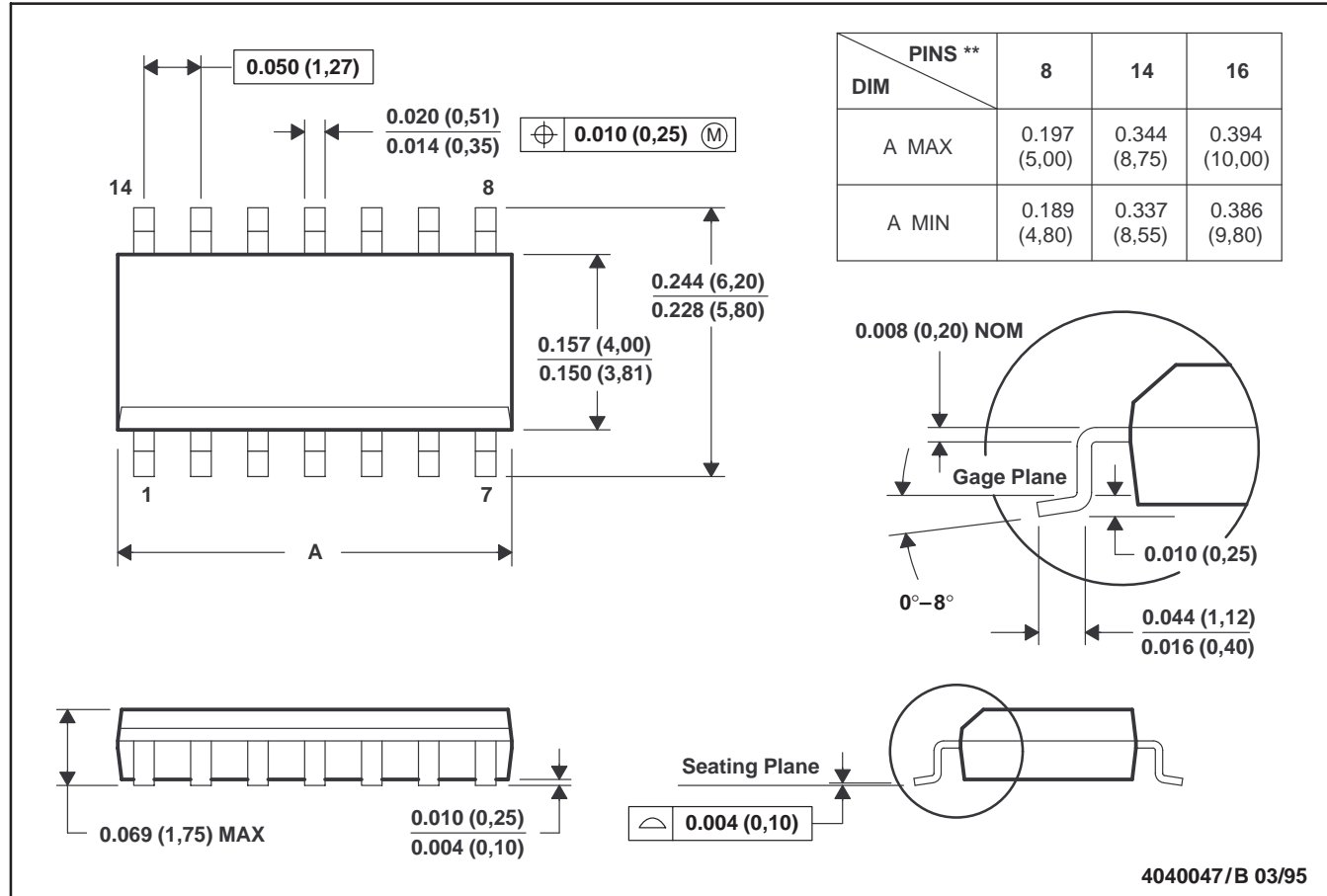
SLCS011B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 - D. Four center pins are connected to die mount pad.
 - E. Falls within JEDEC MS-012

TLV2352, TLV2352Y

LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

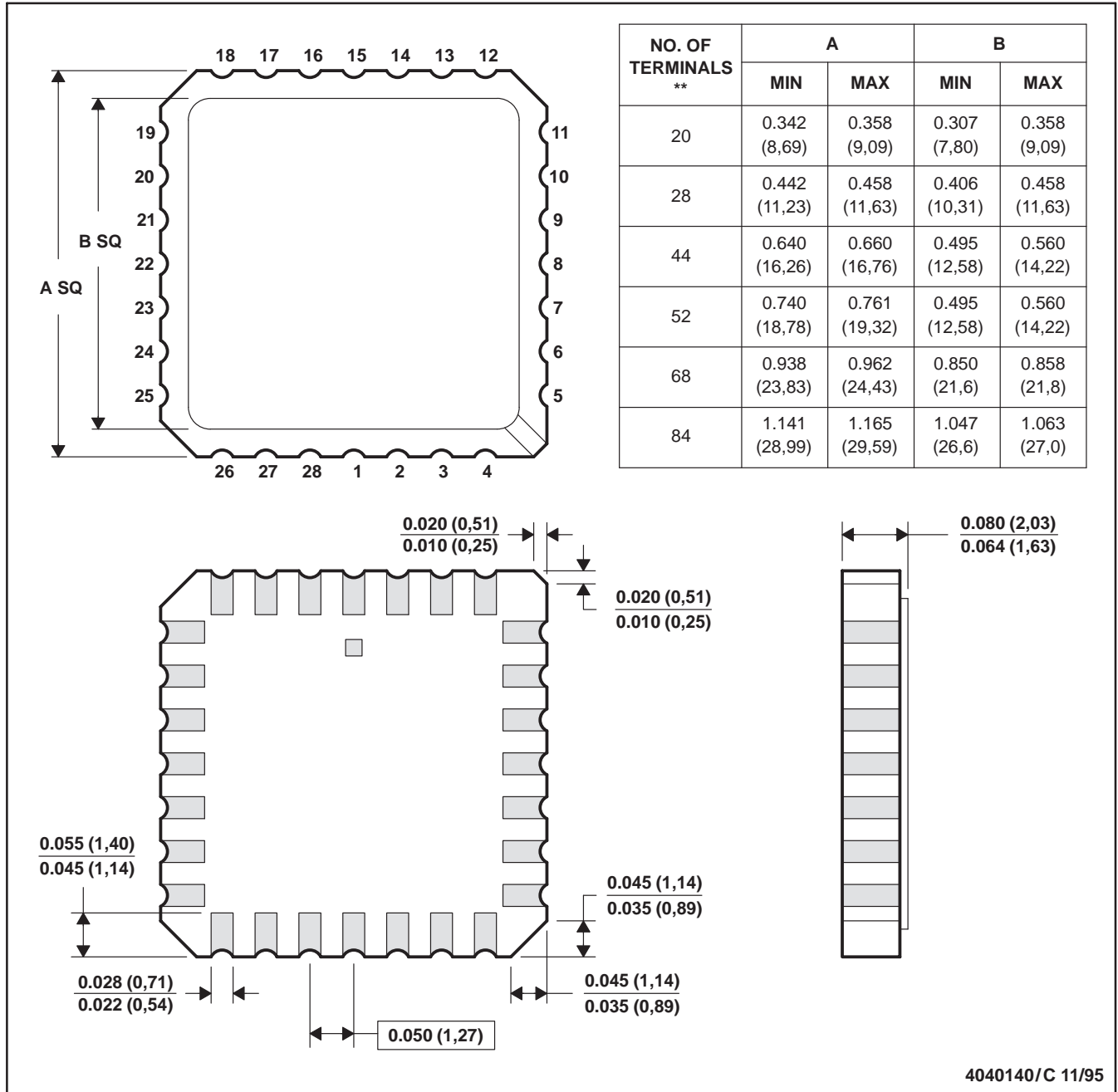
SLCS011B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

FK (S-CQCC-N)**

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

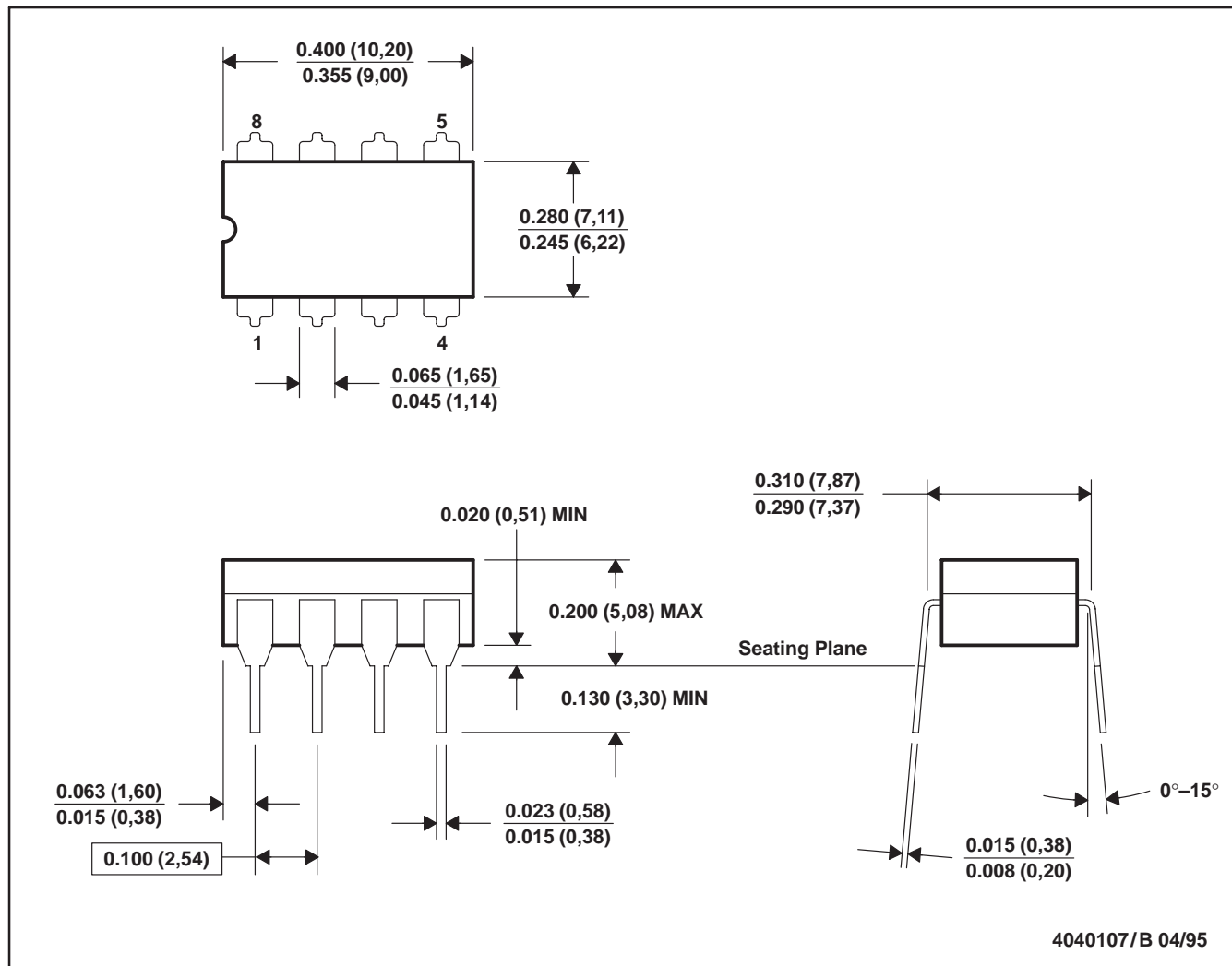
TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE PACKAGE

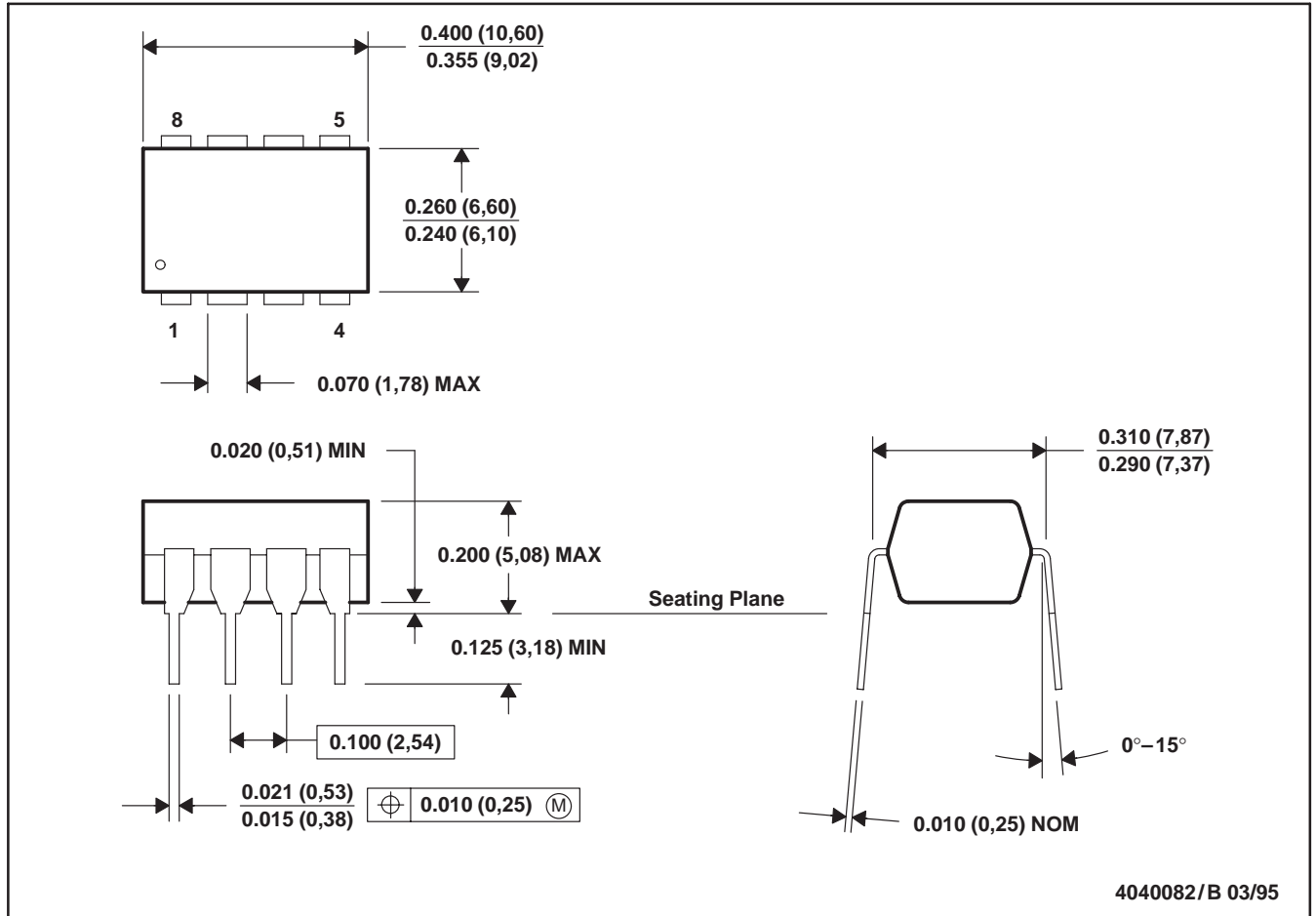


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
 E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL INFORMATION

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

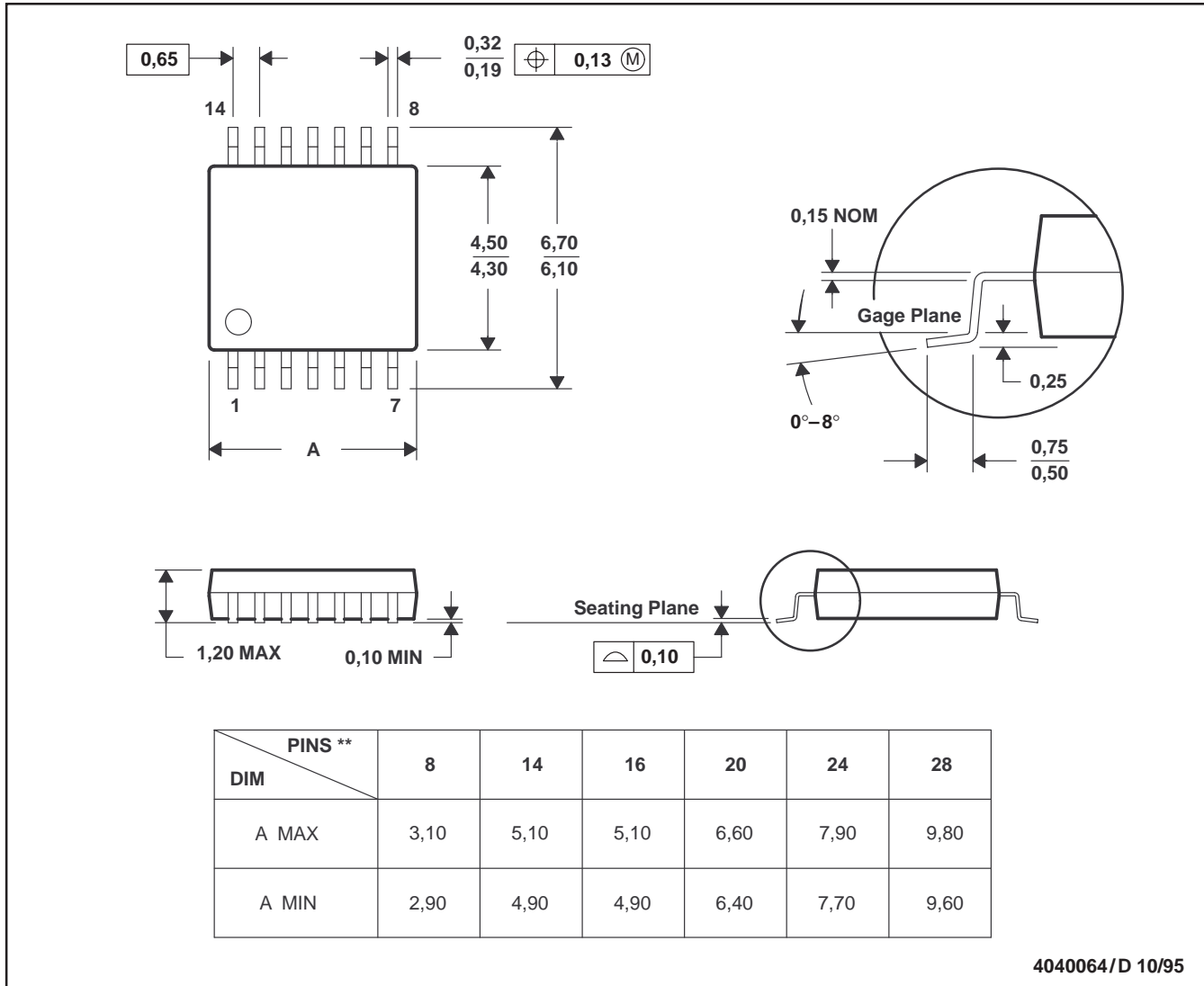
SLCS011B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

TLV2352, TLV2352Y

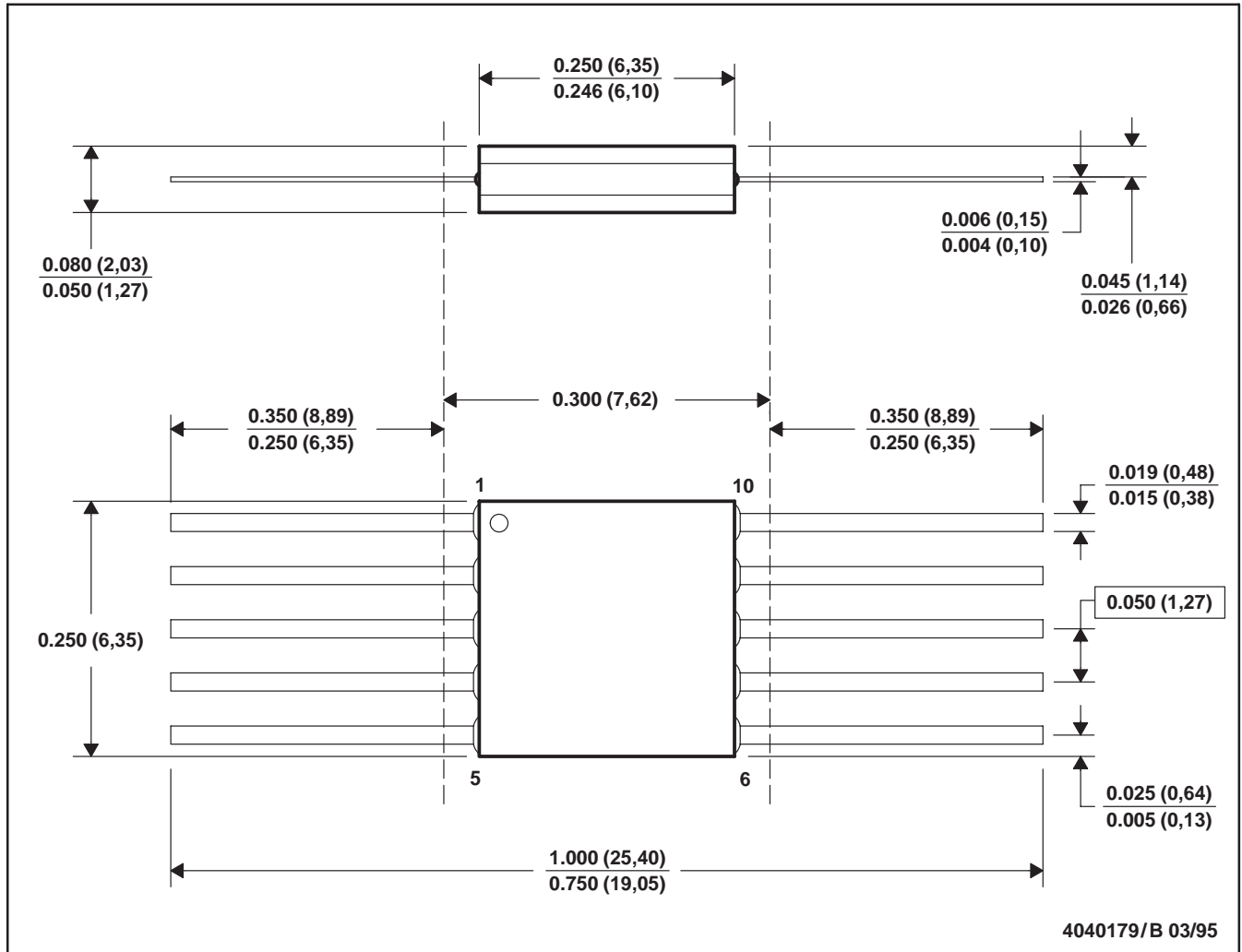
LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9688101Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9688101QHA	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9688101QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2352ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2352IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2352IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2352IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2352IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2352IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2352IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2352IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2352IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLV2352IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2352IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2352MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLV2352MJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2352MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2352MUB	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2352IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2352IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2352IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2352IPWR	TSSOP	PW	8	2000	346.0	346.0	29.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated