Description

The **TM50S116T** is organized as 2-bank x 524288-word x 16-bit(**1Mx16**), fabricated with high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

■ Package 400-mil 50-pin TSOP(II)
■ JEDEC PC133/PC100 compatible
■ Single 3.3V Power Supply
■ LVTTL Signal Compatible

■ Programmable
- CAS Latency (3 or 2 clocks)
- Burst Length (1,2,4,8 & full page)
- Burst type (Sequential & Interleave)

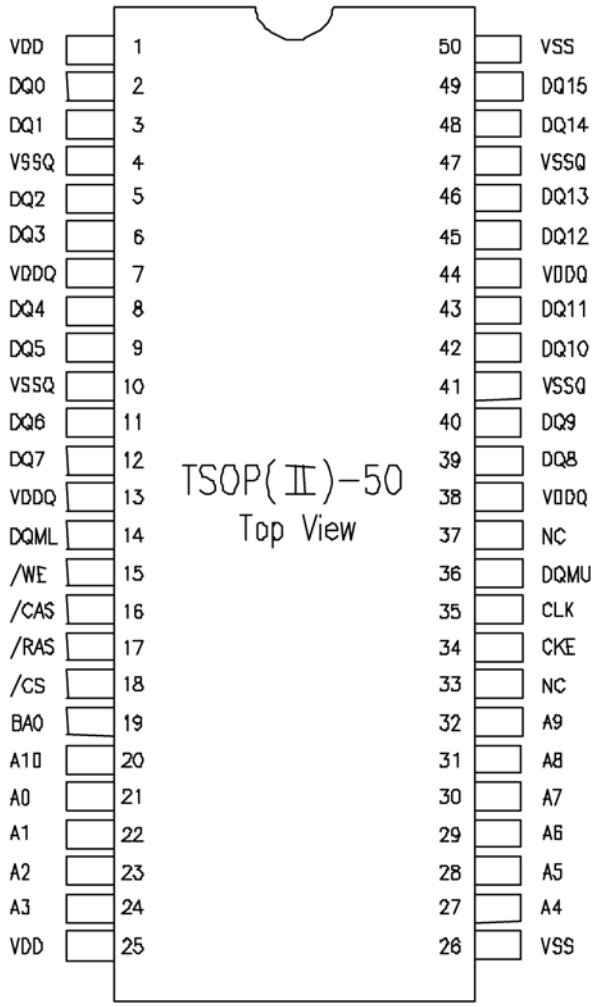
■ Auto and Self Refresh
■ 64ms refresh period (4K cycles)
■ organization
■ Pin33 and 37 are “No Connected”
■ Fully synchronous operation referenced to clock rising edge

Frequency vs. AC Parameter

Symbol	Parameter	- 6	- 7	- 75	Unit
t_{CK}	Min. clock cycle time @CL=3	6	7	7.5	ns
f_{CK}	Max. operating frequency @CL=3	166.7	143	133.3	Mhz
t_{AC}	Max. access time from CLK @CL=3	5.0	5.4	5.4	ns
t_{red}	Min. row to column delay	18	18	20	ns

Pin Description

Pin Name	Function	Pin Name	Function
CLK	Master Clock	DQML/DQMU	Output Disable(Write Mask)
CKE	Clock Enable	A0-10	Address Input
/CS	Chip Select	BA0	Bank Address
/RAS	Row Address Strobe	Vdd	Power Supply
/CAS	Column Address Strobe	VddQ	Power Supply for Output
/WE	Write Enable	Vss/VssQ	Ground
DQ0~DQ15	Data I/O	NC	No Connection



Pin Function

Pin	Name	Pin Function
CLK	System clock	Active on the positive going edge to sample all inputs.
/CS	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK,CKE and DQML/DQMU.
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0~A10	Address input	Row/column addresses are multiplexed on the same pins. Row address:A0~A10, Column address:A0~A7
BA0	Bank address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
/RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with /RAS low. Enables rows access & pre-charge.
/CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with /CAS low. Enables column access.
/WE	Write enable	Enables write operation and row pre-charge. Latches data in starting from /CAS,/WE active.
DQMU/DQML	Data I/O mask (Byte controll)	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQML/DQMU active.
$DQ_{0\sim15}$	Data input/output	Data inputs/outputs are multiplexed on the same pins.
Vdd/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	Data output power / ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC/RFU	No connection / reserved for future use	This pin is recommended to be left no connection on the device.

Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 to 4.6	V
Voltage supply relative to Vss(VssQ)	Vdd,VddQ	-0.5 to 4.6	V
Operating temperature	Topr	0 to +70	• •
Power dissipation	PD	1	W
Output Shorted current	IOS	50	mA

DC OPERATING CONDITIONS

Recommended operating conditions(Referenced to Vss=0V,T_A=0• •to 70•)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	Vdd, VddQ	3.0	3.3	3.6	V
Input Logic High Voltage	V_{IH}	2.0	-	Vdd +0.3	V
Input Logic Low Voltage	V_{IL}	-0.3	-	0.8	V
Output Logic High Voltage	V_{OH}	2.4	-	-	V
Output Logic Low Voltage	V_{OL}	-	-	0.4	V
Input/Output Leakage Current	I_{IL}, I_{OL}	-5	-	5	• A

DC Characteristics

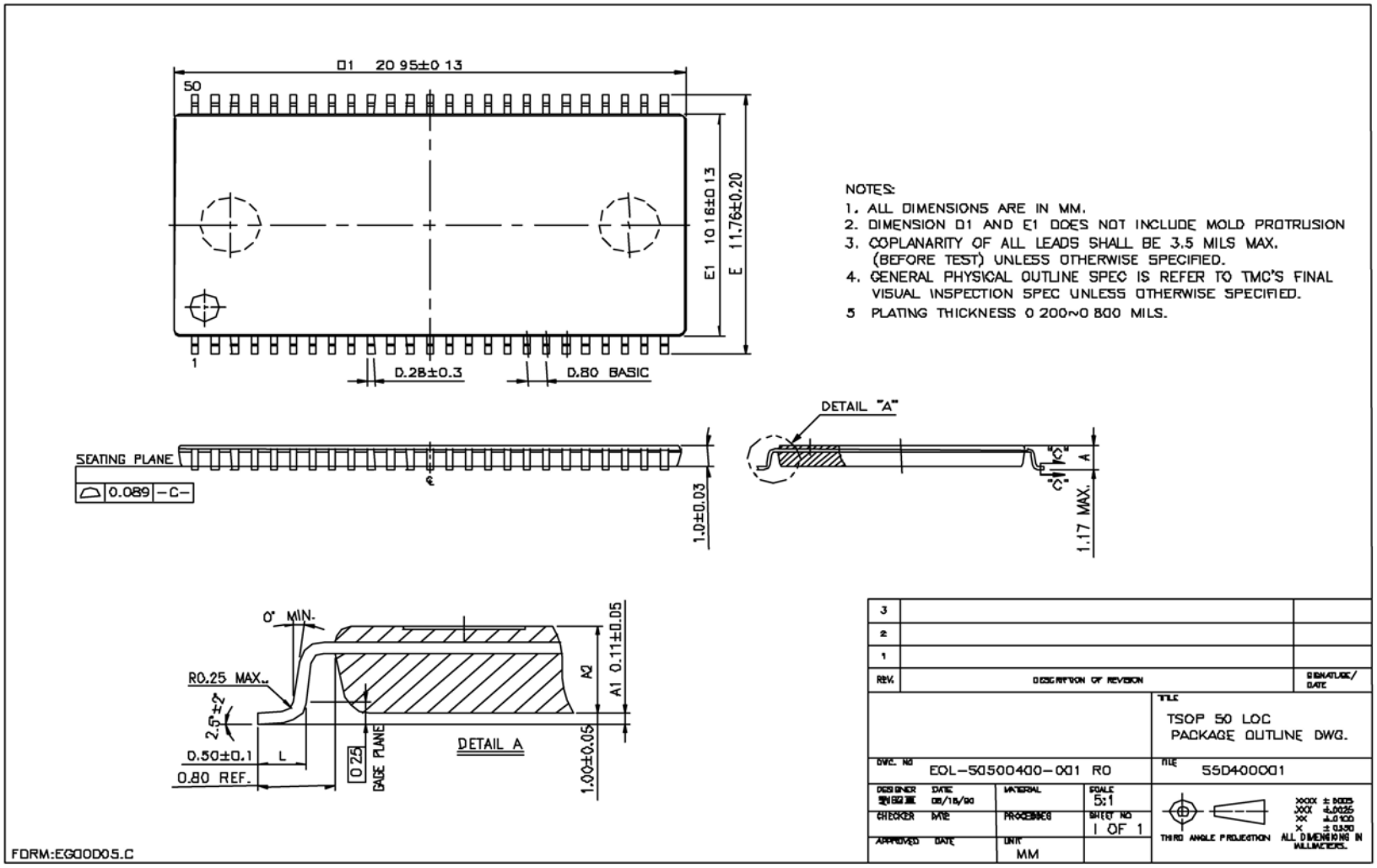
(Recommended operating condition T_A = 0• •to 70• ; unless otherwise noted.)

Parameter	Symbol	Test Conditions	Limits			Unit
			-6	-7	-75	
Operating Current (One bank active)	I_{CC1}	Burst length=1, CL=3, t_{RC} = t_{RC}(min), t_{CK} = t_{CK}(min)	95	85	85	mA
Pre-charge Standby Current in Power Down Mode	I_{CC2}P	CKE=V_{IL}(max), t_{CK} = 15ns	2			mA
	I_{CC2}PS	CKE & CLK=V_{IL}(max)	2			
Pre-charge Standby Current in Non-Power Down Mode	I_{CC2}N	CKE>=V_{IH}(min),/CS> = V_{IH} (min) , t_{CK} = 15ns	20			mA
	I_{CC2}NS	CKE>=V_{IH}(min),/CS> = V_{IH} (min), CLK<= V_{IL}(max) ,	20			
Active Standby Current in Power Down Mode	I_{CC3}P	CKE<=V_{IL}(max), t_{CK} =10ns	7			mA
	I_{CC3}PS	CKE & CLK<=V_{IL}(max)	5			
Active Standby Current in Non-Power Down Mode	I_{CC3}N	/CS=CKE=V_{IH}(min), t_{CK} =15ns	35			mA
	I_{CC3}NS	/CS=CKE=V_{IH}(min), CLK= V_{IL}(max)	35			mA
Operating Current (Burst mode)	I_{CC4}	BL=4,CL=3,All Banks Active	130	100	100	mA
Auto Refresh Current	I_{CC5}	CBR Command cycling	150	130	130	mA
Self Refresh Current	I_{CC6}	CKE<= 0.2V	2			mA

AC Characteristics

Recommended operating conditions(Vdd=VddQ=3.3V,Vss=0V,T_A= 0 to 70•)

	Symbol	Parameter	-6		-7		-75		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{CK}	Clock Cycle Time,CL=3	6.0		7.0		7.5		ns
2	f_{CK}	Clock Frequency,CL=3		166.7		143		133.3	Mhz
3	t_{AC}	Clock Access Time,CL=3		5.0		5.4		5.4	ns
4	t_{CH}	Clock High Pulse Width	2.5		2.5		2.5		ns
5	t_{CL}	Clock Low Pulse Width	2.5		2.5		2.5		ns
6	t_{IS}	Input Setup time(all inputs)	1.5		1.5		1.5		ns
7	t_{IH}	Input Hold time(all inputs)	0.8		0.8		0.8		ns
8	t_T	Transition time of clock	1.0	10	1.0	10	1.0	10	ns
9	t_{RCD}	/RAS to /CAS delay	18		18		20		ns
10	t_{RC}	Row Cycle time	60		63		67		ns
11	t_{RAS}	Row active time	42		42		45		ns
12	t_{RP}	Pre-charge time	15		18		20		ns
13	t_{RRD}	Row active to active delay	12		14		15		ns
14	t_{REF}	Refresh time	64		64		64		ms


D1 20.95±0.13
50
1
E1 10.16±0.13
E 11.76±0.20
0.28±0.3
0.80 BASIC
SEATING PLANE
0.089 -C-
1.0±0.03
DETAIL "A"
A
1.17 MAX.
0° MIN.
R0.25 MAX.
2.5°±2°
0.50±0.1
L
0.80 REF.
0.25
GAGE PLANE
DETAIL A
A2
A1 0.11±0.05
1.00±0.05
NOTES:
1. ALL DIMENSIONS ARE IN MM.
2. DIMENSION D1 AND E1 DOES NOT INCLUDE MOLD PROTRUSION
3. COPLANARITY OF ALL LEADS SHALL BE 3.5 MILS MAX. (BEFORE TEST) UNLESS OTHERWISE SPECIFIED.
4. GENERAL PHYSICAL OUTLINE SPEC IS REFER TO TMC'S FINAL VISUAL INSPECTION SPEC UNLESS OTHERWISE SPECIFIED.
5 PLATING THICKNESS 0.200~0.800 MILS.
REV.
DESCRIPTION OF REVISION
SIGNATURE/ DATE
TITLE
TSOP 50 LOC PACKAGE OUTLINE DWG.
DWG. NO
EOL-50500400-001 R0
TITLE
55D400001
DESIGNER
DATE
08/15/00
MATERIAL
SCALE
5:1
CHECKER
DATE
PROCESS
SHEET NO
1 OF 1
APPROVED
DATE
UNIT
MM
THIRD ANGLE PROJECTION
ALL DIMENSIONS IN MILLIMETERS.
FORM:EG00D05.C