CMOS 4-BIT MICROCONTROLLER

TMP42C50N, TMP42C70N
TMP42C50M, TMP42C70M

The 42C50/70 are high speed and 4-bit single chip microcomputers with added input/output ports and based on the TLCS-42 CMOS series.
The 42C50/70 are suitable for control of home appliances (such as fans, air-conditioners, refrigerators), audio equipments, games, and toys.

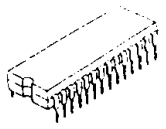
PART No.	ROM	RAM	PACKAGE	PIGGYBACK BOARD
TMP42C50N	512 x 8-bit	32 x 4-bit	SDIP28	BM4211B
TMP42C50M			SOP28	
TMP42C70N	1024 x 8-bit		SDIP28	
TMP42C70M			SOP28	

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time :
  1.0μs (at 5MHz, 4.5 to 6.0V)
  2.5μs (at 2MHz, 4.0 to 6.0V)
- ◆44 basic instructions
  - All instructions are one byte object code
  - Table look-up instructions
- ◆Stack for subroutine call : 1 level
- ◆I/O port (23 pins)
  - I/O 3ports 11pins (Note 1)
  - I/O 2ports 8pins (Note 2)
  - Output 1port 4pins

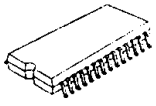
  (Note 1) Software programmable I/O ports
  (Note 2) Mask programmable I/O ports
- ◆Interval Timer (14 stages)
- ◆Hold function
  Battery/Capacitor back-up
- ◆Clock generator
  Ceramic resonator/RC oscillation (mask option)
- ◆Real Time Emulator : BM4221A

SDIP28



TMP42C50N
TMP42C70N

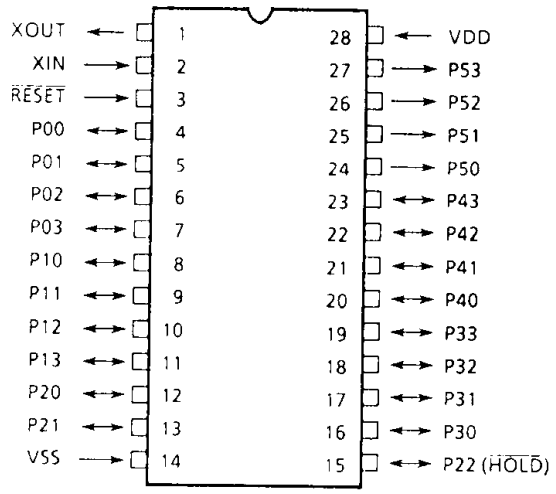
SOP28



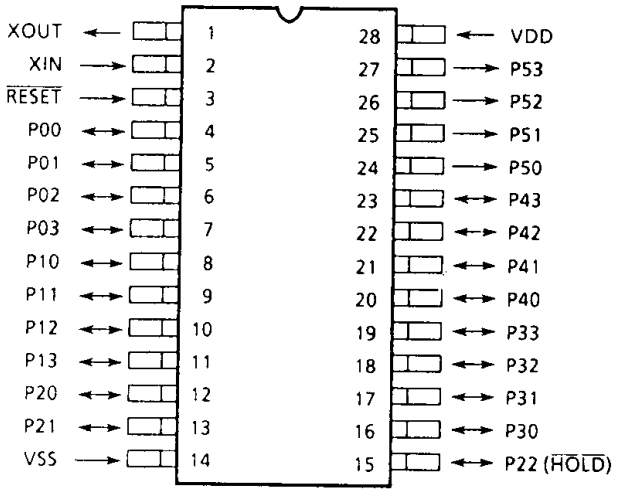
TMP42C50M
TMP42C70M

PIN ASSIGNMENTS (TOP VIEW)

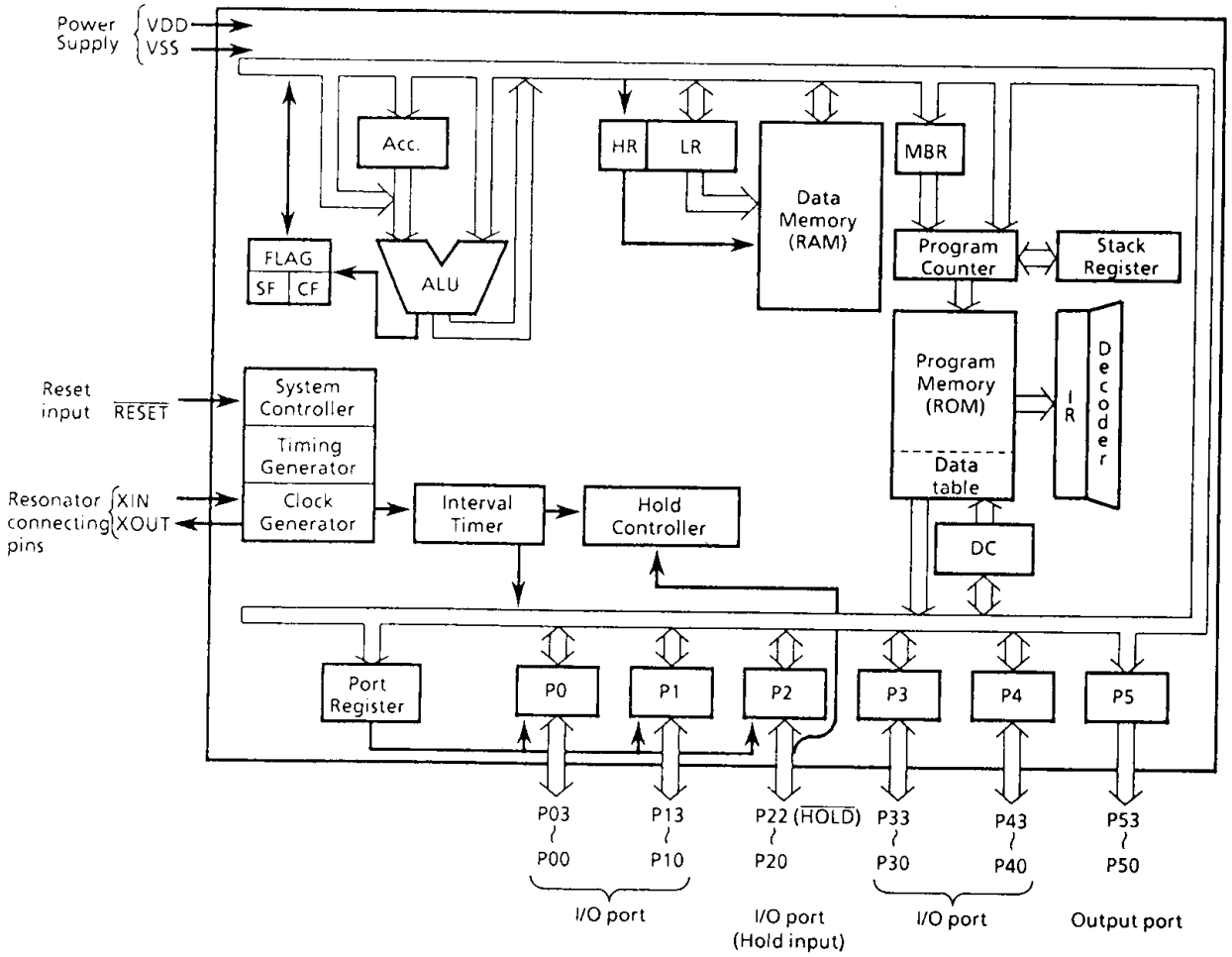
(1) SDIP28



(2) SOP28



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	INPUT/OUTPUT	FUNCTIONS
P03 - P00 P13 - P10	I/O	4- bit programmable I/O ports with latch, input/output mode can be specified by [MOV A, P] instruction.
P22 ($\overline{HOLD}$)	I/O (INPUT)	3-bit programmable I/O port with latch. The four input/output modes can be selected with an I/O control instruction [MOV A, P]. Hold request/release signal input
P21 P20	I/O	
P33 - P30 P43 - P40	I/O	4-bit I/O ports with latch. Mask options make it possible to choose any of four different combinations for each port : input, output, or input/output.
P53 - P50	OUTPUT	4-bit output port with latch
XIN	INPUT	Resonator connecting pins. For inputting external clock, XIN is used, XOUT is opened.
XOUT	OUTPUT	
$\overline{RESET}$	INPUT	Reset signal input
VDD	Power Supply	+ 5V
VSS		0V (GND)

OPERATIONAL DESCRIPTION

Due to mask options, the 42C40/60 are available as the 42C50/70 with a total of 3 additional ports (12 pins) : 2 ports that can select input/output circuit configuration and one dedicated output port. All else is exactly the same as for the 42C40/60. Refer to the 42C40/60 technical data sheet for details.

1. PERIPHERAL HARDWARE FUNCTION

1.1 I/O Ports

The 42C50/70 have 6 I/O ports (11 pins) each as follows:

① P0, P1 ; 4-bit programmable I/O
② P2 ; 3-bit programmable I/O (P22 pin is shared by hold request/release signal input pin.)
③ P3, P4 ; 4-bit I/O (mask option)
④ P5 ; 4-bit Output

The following explanation covers only ports ③ and ④ added to the 42C40/60. These ports do not have input latches, so external input data are either held externally untill read, or are read several times before processing, when necessary.

(1) Ports P3 (P33-P30), P4 (P43-P40)
Any of the four input/output circuit configurations (A, B, C, D) shown in Table 1-1 can be selected for each of the 4-bit ports as a mask option.

Mask option code	P33-P30	P43-P40
A	Push-pull output	Push-pull output
B	Sink open drain output	Push-pull output
C	Sink open drain output	Sink open drain output
D	Input with pull-up resistor	Input with pull-up resistor

Table 1-1. Mask option for Ports P3 and P4

Port P3 (Port address OP03 / IP03)

3	2	1	0
P33	P32	P31	P30

Port P4 (Port address OP04 / IP04)

3	2	1	0
P43	P42	P41	P40

Figure 1-1. Ports P3 and P4

(2) Port P5 (P53-P50)
This is a 4-bit push-pull output port with latch.
The latch is initialized to "1" during reset.

Port P5 (Port address OP05)

3	2	1	0
P53	P52	P51	P50

Figure 1-2. Port P5

1.1.1 Push-pull output

Data from the accumulator or data memory can be transferred to a latch or output from a pin by executing the output instructions [OUT A,%p] and [OUT @HL,%p].
The latch is initialized to "1" during reset.

1.1.2 Sink open drain output

To use for input, set the latch to "1" and use as a high-impedance port. External input data can then be read by executing the input instruction in that status (output transistor off).
To use for output, it is possible to change the output level by connecting an external pull-up resistor.
The latch is initialized to "1" during reset.

1.1.3 Input with pull-up resistor

This is an input-only port with a pull-up resistor. External input data can be read by executing the input instructions [IN %p, A] and [IN %p, @HL].

Note : Power consumption by the oscillation circuit and internal hardware is reduced during hold operation but power consumption by external circuit interfaces is not directly related to hold operation hardware operation, therefore, caution must be observed in system design and interface circuit design. For example, if the power supply voltage of an external circuit is dropped to 0V and the output is at high level, as for the push-pull output shown in Figure 1-6 (a), current may flow through the parasitic diodes of the external circuit in some cases. The relevant pin must be set to low level. Also, with input having a pull-up resistor as shown in Figure 1-6 (b), it is necessary to break the current path with a switch.

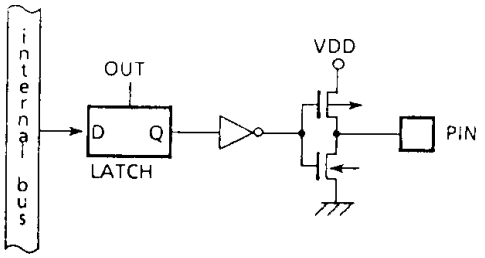


Figure 1-3. Circuitry of push-pull output port

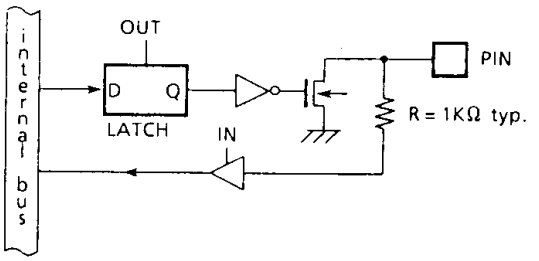


Figure 1-4. Circuitry of sink open drain output and input port

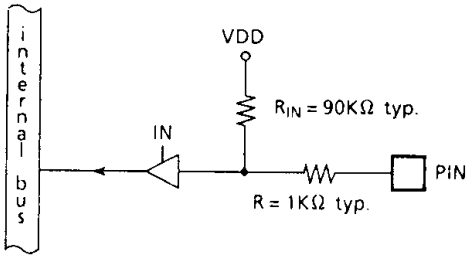
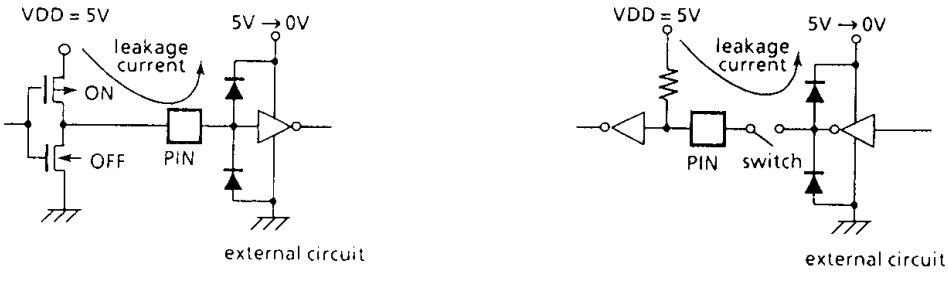


Figure 1-5. Circuitry of input port with pull-up resistor



(a) Push-pull output (b) Input with pull-up resistor

Figure 1-6. External circuit Interface during the Hold operating mode

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (VSS = 0V)

PARAMETER	SYMBOL	PIN	RATING	UNIT
Supply Voltage	V_{DD}		- 0.5 to 7	V
Input Voltage	V_{IN}		- 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain output	- 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain output	- 0.5 to 12	
Output Current (total)	ΣI_{OUT}		60	mA
Power Dissipation [T_{opr} = 85°C]	PD		300	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		- 55 to 125	°C
Operating Temperature	T_{opr}		- 40 to 85	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = - 40 to 85°C)

PARAMETER	SYMBOL	PIN	CONDITIONS	Min.	Min.	UNIT
Supply Voltage	V_{DD}			4.0	6.0	V
Input High Voltage	V_{IH1}	Except Hysteresis Input		V_{DD} × 0.7	V_{DD}	V
	V_{IH2}	Hysteresis Input		V_{DD} × 0.8		
Input Low Voltage	V_{IL1}	Except Hysteresis Input		0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis Input			V_{DD} × 0.2	
Clock Frequency	fc		V_{DD} = 4.0 to 6.0V	0.2	2.0	MHz
			V_{DD} = 4.5 to 6.0V		5.0	

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = − 40 to 85°C)

PARAMETER	SYMBOL	PIN	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis input		—	0.3	—	V
Input Current	I_{IN}	Open drain output	V_{DD} = 6V, V_{IN} = 0V	—	− 10^{-5}	− 2.0	μA
High Input Current	I_{IH}	Ports P0, P1, P2	V_{DD} = 5V, V_{IN} = 5V	15	30	80	μA
Input Resistance	R_{IN1}	$\overline{RESET}$		65	160	340	KΩ
	R_{IN2}	Input with pull-up resistor		35	90	190	
Output Leakage Current	I_{LO}	Open drain output	V_{DD} = 6V, V_{OUT} = 6V	—	10^{-5}	2.0	μA
Output High Voltage	V_{OH}	Push-pull output	V_{DD} = 5V, I_{OH} = − 5μA	4.7	4.9	—	V
Output High Current	I_{OH}		V_{DD} = 4V, V_{OH} = 2.4V	− 1.0	− 4.5	—	mA
Output Low Current	I_{OL}	Ports P0-P5	V_{DD} = 4.5V, V_{OL} = 0.4V	1.6	5.0	—	mA
Supply Current (In the Normal operating mode)	I_{DD}		V_{DD} = 6V, fc = 2MHz	—	0.8	3.0	mA
Supply Current (In the HOLD operating mode)	I_{DDH}		V_{DD} = 5V	—	0.1	5.0	μA

Note 1. Typ. values shows those at V_{DD} = 5V, T_{opr} = 25°C.

Note 2. Supply Current in the Normal operating mode: $\overline{RESET}$ pin is 0V, and XOUT pin and ports are opened in the external clock operation.

Note 3. Supply Current in the Hold operating mode : All pins other than the power supply pins (VDD, VSS) are open. This port is fixed at 0V when sink open drain pins are specified as by mask option.

A.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = − 40 to 85°C)

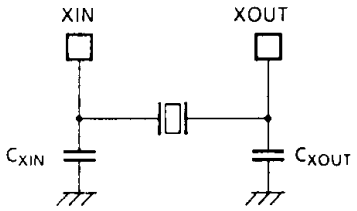
PARAMETER	SYMBOL	CONDITIONS		Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	V_{DD} = 4.0 to 6.0V		2.5	—	25	μs
		V_{DD} = 4.5 to 6.0V		1.0			
High level Clock pulse Width	t_{WCH}	V_{IN} = V_{IH}	For external clock operation	100	—	—	ns
Low level Clock pulse Width	t_{WCL}	V_{IN} = V_{IL}					

RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0V, V_{DD} = 4.0 to 6.0V, T_{opr} = – 40 to 85°C)

(1) Ceramic Resonator

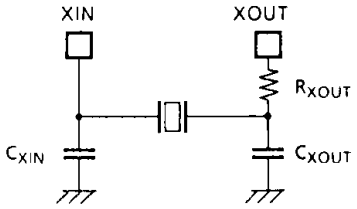
5MHz (V_{DD} = 4.5 to 6.0V)
CSA5.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF

2MHz
CSA2.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 100pF



1MHz
CSB1000D (MURATA) $C_{XIN} = C_{XOUT}$ = 330pF

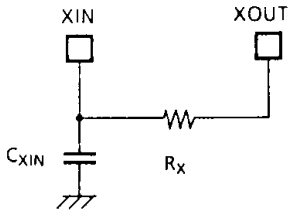
455KHz
CSB455E (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 5.6KΩ



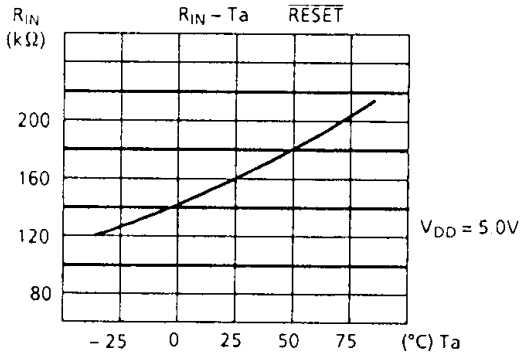
(2) RC Oscillation

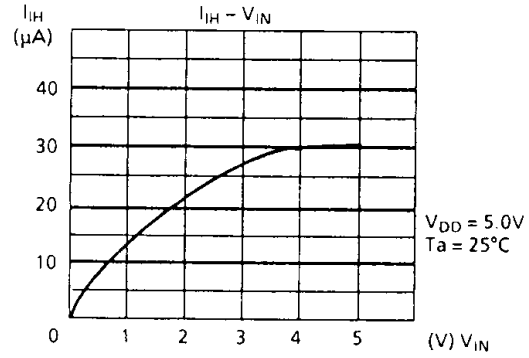
1MHz typ. R_X = 15KΩ, C_{XIN} = 100pF

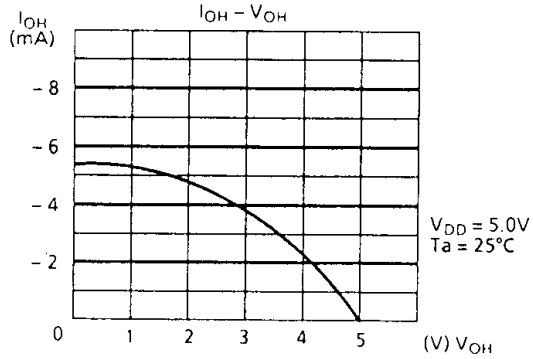
500KHz typ. R_X = 36KΩ, C_{XIN} = 100pF

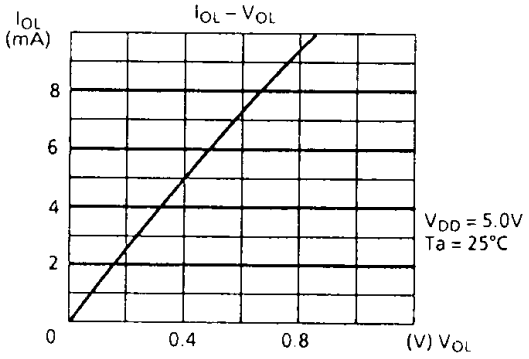


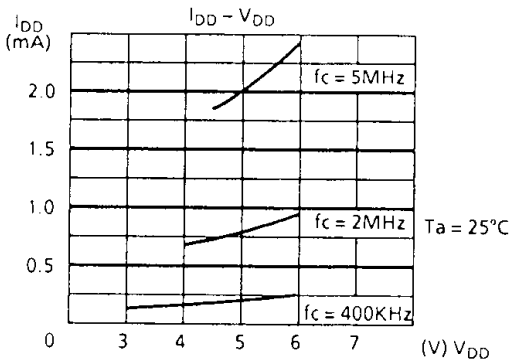
TYPICAL CHARACTERISTICS

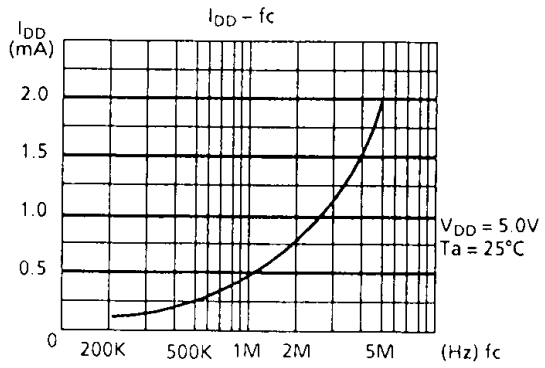


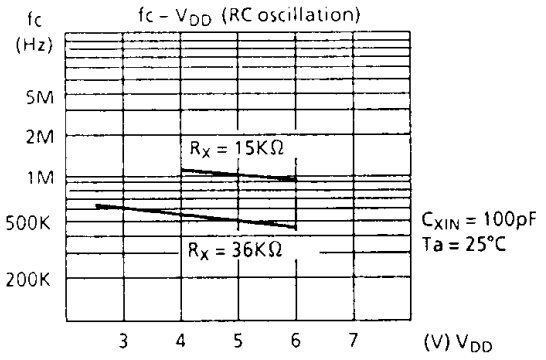


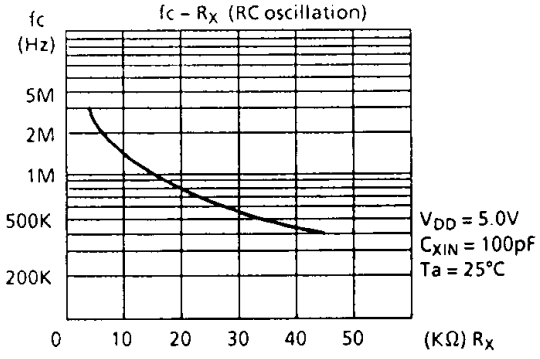


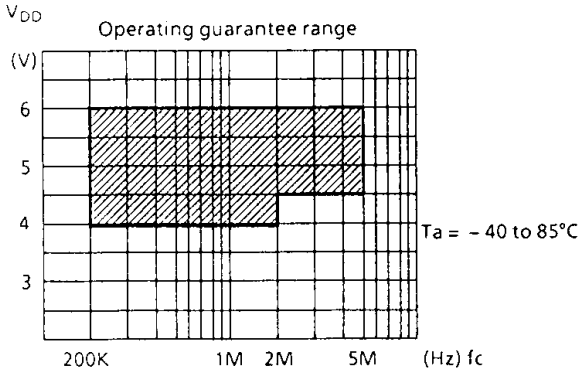







fc
(Hz)
fc - V_{DD} (RC oscillation)
5M
2M
1M
500K
200K
R_X = 15KΩ
R_X = 36KΩ
C_{XIN} = 100pF
Ta = 25°C
3
4
5
6
7
(V) V_{DD}


fc
(Hz)
fc - R_X (RC oscillation)
5M
2M
1M
500K
200K
V_{DD} = 5.0V
C_{XIN} = 100pF
Ta = 25°C
0
10
20
30
40
50
(KΩ) R_X

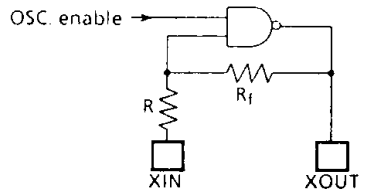
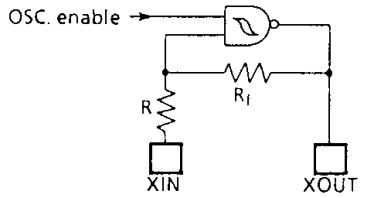
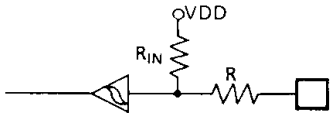

V_{DD}
Operating guarantee range
(V)
6
5
4
3
Ta = - 40 to 85°C
200K
1M
2M
5M
(Hz) fc

INPUT/OUTPUT CIRCUITRY

(1) Control pins

The input/output circuitries of the 42C50/70 control pins are shown below.

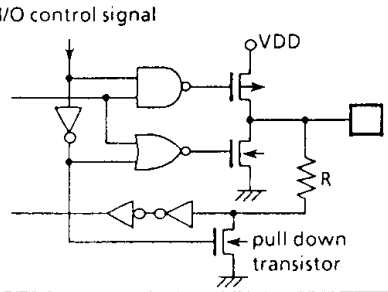
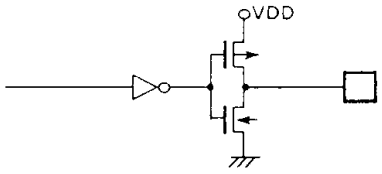
Oscillation type can be chosen by mask option either a ceramic resonator (external clock input) or an RC oscillator.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	INPUT OUTPUT	Option : Ceramic resonator or External clock input 	Resonator connecting pins R = 1KΩ (typ.) R_f = 1MΩ (typ.)
		Option : RC oscillation 	Resonator connecting pins Hysteresis input R = 1KΩ (typ.) R_f = 1MΩ (typ.)
$\overline{\text{RESET}}$	INPUT		Hysteresis input Pull-up resistor R_{IN} = 160KΩ (typ.) R = 1KΩ (typ.)

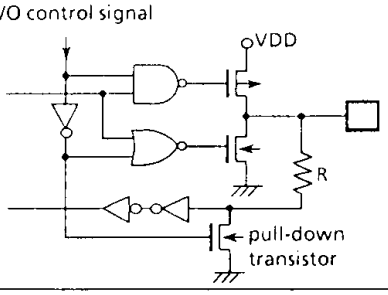
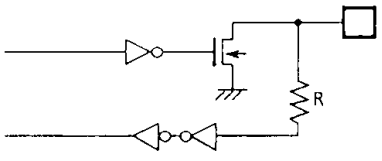
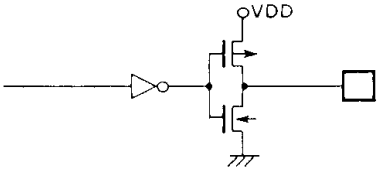
(2) I/O ports

The input/output circuitries of 42C50/70 I/O ports are shown as below, any one of the circuitries can be chosen by a code (A, B, C, D) as a mask option.

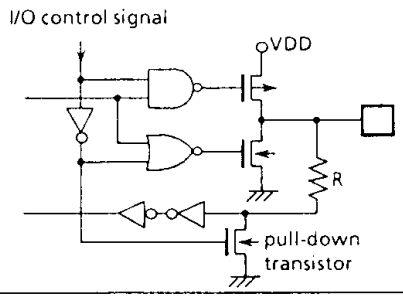
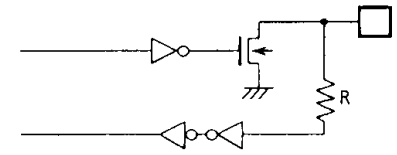
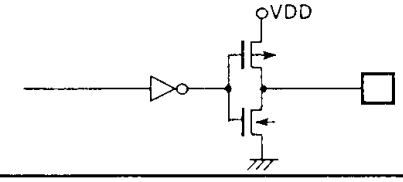
Input/Output circuitry (Code : A) Standard circuitry

PORT	I/O	CIRCUITRY	Initial state	REMARKS
P0 P1 P2	I/O		Input	Programmabe I/O port Input mode : Input with pull-down Output mode : Push-pull R = 1KΩ (typ.)
P3 P4 P5	Output		High	Push-pull output

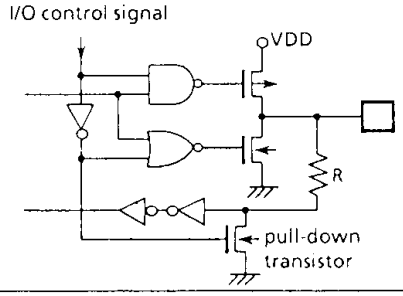
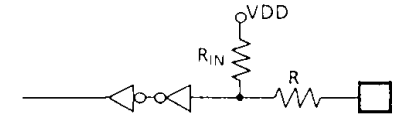
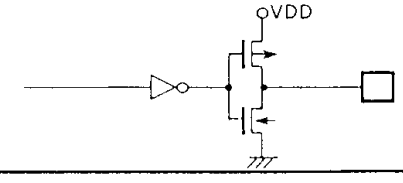
Input/Output circuity (Code : B) Port P3 of the standard circuitry is changed to a sink open drain output and input.

PORT	I/O	CIRCUITRY	Initial state	REMARKS
P0 P1 P2	I/O		Input	Programmble I/O port Input mode : Input with pull-down Output mode : Push-pull R = 1KΩ (typ.)
P3	I/O		Hi-Z (input)	Sink open drain output (R = 1KΩ typ.)
P4 P5	Output		High	Push-pull output

Input/Output circuitry (Code : C) Ports P3 and P4 of the standard circuitry are changed to sink open drain outputs and inputs.

PORT	I/O	CIRCUITRY	Initial state	REMARKS
P0 P1 P2	I/O		Input	Programmable I/O port Input mode : Input with pull-down Output mode : Push-pull output R = 1KΩ (typ.)
P3 P4	I/O		Hi-Z (Input)	Sink open drain output R = 1KΩ (typ.)
P5	Output		High	Push-pull output

Input/Output circuity (Code : D) Ports P3 and P4 of the standard circuitry are changed to inputs with pull-up resistor.

PORT	I/O	CIRCUITRY	Initial state	REMARKS
P0 P1 P2	I/O		Input	Programmable I/O port Input mode : Input with pull-down Output mode : Push-pull R = 1KΩ (typ.)
P3 P4	Input		Input	Pull-up resistor R_{IN} = 90KΩ (typ.) R = 1KΩ (typ.)
P5	Output		High	Push-pull