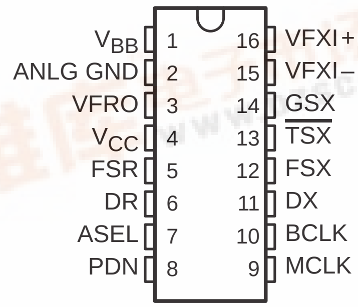
# TP3056B
# MONOLITHIC SERIAL INTERFACE COMBINED PCM CODEC AND FILTER

SLWS072A – MAY 1998 – REVISED AUGUST 1998

- **Complete PCM Codec and Filtering Systems Include:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter With (sin x)/x Correction**
  - **Active RC Noise Filters**
  - **µ-Law and A-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Autozero Circuitry**
- **µ-Law/A-Law Operation Pin-Selectable**
- **±5-V Operation**
- **Low Operating Power . . . 60 mW Typ**
- **Power-Down Mode . . . 5 mW Typ**
- **Automatic Power Down**
- **TTL- or CMOS-Compatible Digital Interface**
- **Maximizes Line Interface Card Circuit Density**

**DW OR N PACKAGE**
**(TOP VIEW)**




## description

The TP3056B monolithic serial interface combined PCM codec and filter device is comprised of a single-chip PCM codec (pulse code-modulated encoder and decoder) and analog filters. This device provides all the functions required to interface a full-duplex (2-wire) voice telephone circuit with a TDM (time-division-multiplexed) system. Primary applications include:

- Line interface for digital transmission and switching of T1/E1 carrier, PABX, and central office telephone systems
- Subscriber line concentrators
- Digital-encryption systems
- Digital voice-band data-storage systems
- Digital signal processing

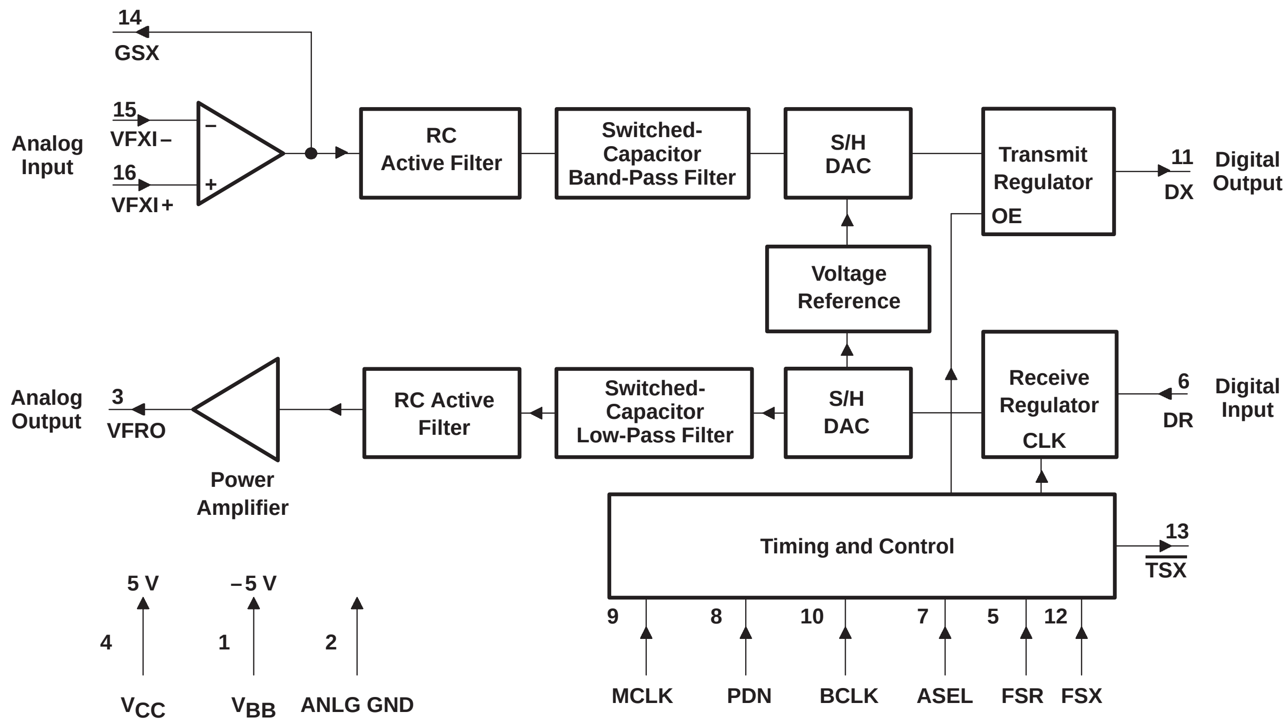
The TP3056B is designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion), and the appropriate filtering of analog signals in a PCM system. This device is intended to be used at the analog termination of a PCM line or trunk. It requires a master clock of 2.048 MHz, a transmit/receive data clock that is synchronous with the master clock (but can vary from 64 kHz to 2.048 MHz), and transmit and receive frame-sync pulses. The TP3056B contains patented circuitry to achieve low transmit channel idle noise and is not recommended for applications in which the composite signals on the transmit side are below –55 dBm0.

This device, available in 16-pin N PDIP (plastic dual-in-line package) and 16-pin DW SOIC (small outline IC) packages, is characterized for operation from 0°C to 70°C.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## functional block diagram



## Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| ANLG GND | 2 | | Analog ground. All signals are referenced to ANLG GND. |
| ASEL | 7 | I | A-law/μ-law select. When ASEL is connected to $V_{CC}$, A-law is selected. When ASEL is connected to GND or $V_{BB}$, μ-law is selected. |
| BCLK | 10 | I | Transmit/receive bit clock. BCLK shifts PCM data out on DX during transmit and shifts PCM data in through DR during receive. BCLK can vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLK. |
| DR | 6 | I | Receive data input. PCM data is shifted into DR at the trailing edge of the BCLK following the FSR leading edge. |
| DX | 11 | O | DX is the 3-state PCM data output that is enabled by FSX. Data is shifted out on the rising edge of BCLK. |
| FSR | 5 | I | Receive-frame sync pulse input. FSR enables BCLK to shift PCM data in DR. FSR is an 8-kHz pulse train (see Figures 1 and 2 for timing details). |
| FSX | 12 | I | Transmit-frame sync pulse. FSX enables BCLK to shift out the PCM data on DX. FSX is an 8-kHz pulse train (see Figures 1 and 2 for timing details). |
| GSX | 14 | O | Analog output of the transmit input amplifier. GSX is used to set gain externally. |
| MCLK | 9 | I | Transmit/receive master clock. MCLK must be 2.048 MHz. |
| PDN | 8 | I | Power down. When PDN is connected high, the device is powered down. When PDN is connected low or left floating, the device is powered up. PDN is internally tied low. |
| $\overline{TSX}$ | 13 | O | Transmit channel time-slot strobe. $\overline{TSX}$ is an open-drain output that pulses low during the encoder time slot. |
| $V_{BB}$ | 1 | | Negative power supply. $V_{BB}$ = –5 V ±5% |
| $V_{CC}$ | 4 | | Positive power supply. $V_{CC}$ = 5 V ±5% |
| VFRO | 3 | O | Analog output of the receive channel power amplifier |
| VFXI+ | 16 | I | Noninverting input of the transmit input amplifier |
| VFXI– | 15 | I | Inverting input of the transmit input amplifier |

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7 V
Supply voltage, $V_{BB}$ (see Note 1) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –7 V
Voltage range at any analog input or output . . . . . . . . . . . . . . . . . . . . . . . . . . . . $V_{CC}$ +0.3 V to $V_{BB}$ –0.3 V
Voltage range at any digital input or output . . . . . . . . . . . . . . . . . . . . . . . . . . $V_{CC}$ +0.3 V to ANLG GND –0.3 V
Continuous total dissipation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . See Dissipation Rating Table
Operating free-air temperature range: TP3056B . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . . . . . . . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|
| DW | 1025 mW | 8.2 mW/°C | 656 mW | 533 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW |

## recommended operating conditions (see Note 2)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Supply voltage, $V_{BB}$ | –4.75 | –5 | –5.25 | V |
| High-level input voltage, $V_{IH}$ | 2.2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | 0.6 | V |
| Common-mode input voltage range, $V_{ICR}$‡ | | | ±2.5 | V |
| Load resistance, GSX, $R_L$ | 10 | | | kΩ |
| Load capacitance, GSX, $C_L$ | | | 50 | pF |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

‡ Measured with CMRR > 60 dB

NOTE 2: To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.

## electrical characteristics over recommended ranges of supply voltage operating free-air temperature range, in A-law and μ-law modes (unless otherwise noted)

### supply current

| PARAMETER | | | TEST CONDITIONS | TP3056B | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP§ | MAX | |
| $I_{CC}$ | Supply current from $V_{CC}$ | Power down | No load | | 0.5 | 1 | mA |
| | | Operating | | | 6 | 9 | |
| $I_{BB}$ | Supply current from $V_{BB}$ | Power down | No load | | 0.5 | 1 | mA |
| | | Operating | | | 6 | 9 | |

§ All typical values are at $V_{CC}$ = 5 V, $V_{BB}$ = –5 V, and $T_A$ = 25°C.

## electrical characteristics at $V_{CC}$ = 5 V ±5%, $V_{BB}$ = –5 V ±5%, GND at 0 V, $T_A$ = 25°C (unless otherwise noted)

### digital interface

| PARAMETER | | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | DX | $I_H$ = -3.2 mA | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | DX | $I_L$ = 3.2 mA | | 0.4 | V |
| | | $\overline{TSX}$ | $I_L$ = 3.2 mA, Drain open | | 0.4 | |
| $I_{IH}$ | High-level input current | | $V_I = V_{IH}$ to $V_{CC}$ | | ±10 | μA |
| $I_{IL}$ | Low-level input current | All digital inputs | $V_I$ = GND to $V_{IL}$ | | ±10 | μA |
| $I_{OZ}$ | Output current in high-impedance state | DX | $V_O$ = GND to $V_{CC}$ | | ±10 | μA |

### analog interface with transmit amplifier input

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{ICR}$‡ | Common-mode input voltage range | | | | | ±2.5 | V |
| $I_I$ | Input current | VFXI+ or VFXI – | $V_I$ = –2.5 V to 2.5 V | | | ±200 | nA |
| $r_i$ | Input resistance | VFXI+ or VFXI – | $V_I$ = –2.5 V to 2.5 V | 10 | | | MΩ |
| $A_V$ | Open-loop voltage amplification | VFXI+ to GSX | | 5000 | | | |
| $B_I$ | Unity-gain bandwidth | GSX | | 1 | 2 | | MHz |
| $V_{IO}$ | Input offset voltage | VFXI+ or VFXI – | | | | ±20 | mV |
| CMRR | Common-mode rejection ratio | | | 60 | | | dB |
| $K_{SVR}$ | Supply-voltage rejection ratio | | | 60 | | | dB |

† All typical values are at $V_{CC}$ = 5 V, $V_{BB}$ = –5 V, and $T_A$ = 25°C.
‡ Measured with CMRR > 60 dB.

### analog interface with receive amplifier output

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| Receive output drive voltage | | $R_L$ = 10 kΩ | | | ±2.5 | V |
| Output resistance | VFRO | | | 1 | 3 | Ω |
| Load resistance | | VFRO = ±2.5 V | 600 | | | Ω |
| Load capacitance | VFRO to GND | | | | 500 | pF |
| Output dc offset voltage | VFRO to GND | | | | ±200 | mV |

† All typical values are at $V_{CC}$ = 5 V, $V_{BB}$ = –5 V, and $T_A$ = 25°C.

## operating characteristics, over operating free-air temperature range, $V_{CC}$ = 5 V ±5%, $V_{BB}$ = –5 V ±5%, GND at 0 V, $V_I$ = 1.2276 V, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting, in A-law and μ-law modes, (unless otherwise noted)

### filter gains and tracking errors

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Maximum peak transmit overload level | μ-law | 3.17 dBm0 | | | 2.501 | | V |
| | A-law | 3.14 dBm0 | | | 2.492 | | |
| Transmit filter gain, absolute‡ (at 0 dBm0) | | $T_A$ = 25°C | | – 0.15 | | 0.15 | dB |
| Transmit filter gain, relative to absolute‡ | | f = 16 Hz | | | | –40 | dB |
| | | f = 50 Hz | | | | –30 | |
| | | f = 60 Hz | | | | –26 | |
| | | f = 200 Hz | | –1.8 | | –0.1 | |
| | | f = 300 Hz to 3000 Hz | | –0.15 | | 0.15 | |
| | | f = 3300 Hz | | –0.35 | | 0.05 | |
| | | f = 3400 Hz | | –0.8 | | 0 | |
| | | f = 4000 Hz | | | | –14 | |
| | | f ≥ 4600 Hz (measure response from 0 Hz to 4000 Hz) | | | | –32 | |
| Absolute‡ transmit gain variation with temperature and supply voltage relative to absolute transmit gain | | | | –0.1 | | 0.1 | dB |
| Transmit gain tracking error with level | | Sinusoidal test method, Reference level = –10 dBm0 | 3 dBm0 ≥ input level ≥ –40 dBm0 | | | ±0.2 | dB |
| | | | –40 dBm0 > input level ≥ –50 dBm0 | | | ±0.4 | |
| | | | –50 dBm0 > input level ≥ –55 dBm0 | | | ±0.8 | |
| Receive filter gain, absolute‡ (at 0 dBm0) | | Input is digital code sequence for 0-dBm0 signal, $T_A$ = 25°C | | –0.15 | | 0.15 | dB |
| Receive filter gain, relative to absolute‡ | | f = 0 Hz to 3000 Hz, | $T_A$ = 25°c | –0.15 | | 0.15 | dB |
| | | f = 3300 Hz | | –0.35 | | 0.05 | |
| | | f = 3400 Hz | | –0.8 | | 0 | |
| | | f = 4000 Hz | | | | –14 | |
| Absolute‡ receive gain variation with temperature and supply voltage | | $T_A$ = full range, | See Note 3 | –0.1 | | 0.1 | dB |
| Receive gain tracking error with level | | Sinusoidal test method; reference input PCM code corresponds to an ideally encoded –10 dBm0 signal | 3 dBm0 ≥ input level ≥ –40 dBm0 | | | ±0.2 | dB |
| | | | –40 dBm0 > input level ≥ –50 dBm0 | | | ±0.4 | |
| | | | –50 dBm0 > input level ≥ –55 dBm0 | | | ±0.8 | |
| Transmit and receive gain tracking error with level (A-law, CCITT G 712) | | Pseudo-noise test method; reference input PCM code corresponds to an ideally encoded –10 dBm0 signal | 3 dBm0 ≥ input level ≥ –40 dBm0 | | | ±0.25 | dB |
| | | | –40 dBm0 > input level ≥ –50 dBm0 | | | ±0.3 | |
| | | | –50 dBm0 > input level ≥ –55 dBm0 | | | ±0.45 | |

† All typical values are at $V_{CC}$ = 5 V, $V_{BB}$ = –5 V, and $T_A$ = 25°C.
‡ Absolute rms signal levels are defined as follows: $V_I$ = 1.2276 V = 0 dBm0 = 4 dBm at f = 1.02 kHz with $R_L$ = 600 Ω.
NOTE 3: Full range for the TP3056B is 0°C to 70°C.

## operating characteristics, over operating free-air temperature range, $V_{CC}$ = 5 V ±5%, $V_{BB}$ = –5 V ±5%, GND at 0 V, $V_I$ = 1.2276 V, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting, in A-law and µ-law modes, (unless otherwise noted) (continued)

### envelope delay distortion with frequency

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|
| Transmit delay, absolute (at 0 dBm0) | f = 1600 Hz | | 290 | 315 | µs |
| Transmit delay, relative to absolute‡ | f = 500 Hz to 600 Hz | | 195 | 220 | µs |
| | f = 600 Hz to 800 Hz | | 120 | 145 | |
| | f = 800 Hz to 1000 Hz | | 50 | 75 | |
| | f = 1000 Hz to 1600 Hz | | 20 | 40 | |
| | f = 1600 Hz to 2600 Hz | | 55 | 75 | |
| | f = 2600 Hz to 2800 Hz | | 80 | 105 | |
| | f = 2800 Hz to 3000 Hz | | 130 | 155 | |
| Receive delay, absolute (at 0 dBm0) | f = 1600 Hz | | 180 | 200 | µs |
| Receive delay, relative to absolute‡ | f = 500 Hz to 1000 Hz | –40 | –25 | | µs |
| | f = 1000 Hz to 1600 Hz | –30 | –20 | | |
| | f = 1600 Hz to 2600 Hz | | 70 | 90 | |
| | f = 2600 Hz to 2800 Hz | | 100 | 125 | |
| | f = 2800 Hz to 3000 Hz | | 140 | 175 | |

† All typical values are at $V_{CC}$ = 5 V, $V_{BB}$ = –5 V, and $T_A$ = 25°C.
‡ Absolute rms signal levels are defined as follows: $V_I$ = 1.2276 V = 0 dBm0 = 4 dBm at f = 1.02 kHz with $R_L$ = 600 Ω.

### noise

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| Transmit noise, C-message weighted | µ-law | VFXI = 0 V | | 9 | 14 | dBrnC0 |
| Transmit noise, psophometric weighted (see Note 4) | A-law | VFXI = 0 V | | –78 | –75 | dBm0p |
| Receive noise, C-message weighted | µ-law | PCM code equals alternating positive and negative zero. | | 2 | 4 | dBrnC0 |
| Receive noise, psophometric weighted | A-law | PCM code equals positive zero. | | –86 | –83 | dBm0p |
| Noise, single frequency | | VFXI+ = 0 V, f = 0 kHz to 100 kHz, Loop-around measurement | | | –53 | dBm0 |

† All typical values are at $V_{CC}$ = 5 V, $V_{BB}$ = –5 V, and $T_A$ = 25°C.
NOTE 4: Measured by extrapolation from the distortion test result. This parameter is achieved through use of patented circuitry and is not recommended for applications in which the composite signals on the transmit side are below –55 dBm0.

### crosstalk

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|
| Crosstalk, transmit to receive | f = 300 Hz to 3000 Hz, DR at steady PCM code | | –90 | –75 | dB |
| Crosstalk, receive to transmit (see Note 5) | VFXI = 0 V, f = 300 Hz to 3000 Hz | | –90 | –75 | dB |

† All typical values are at $V_{CC}$ = 5 V, $V_{BB}$ = –5 V, and $T_A$ = 25°C.
NOTE 5: Receive-to-transmit crosstalk is measured with a – 50 dBm0 activation signal applied at VFXI+.

### power amplifiers

| PARAMETER | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Maximum 0 dBm0 rms level for better than ±0.1 dB linearity over the range if –10 dBm0 to 3 dBm0 | Balanced load, $R_L$, connected between VFRO and Gnd | $R_L$ = 600 Ω | 1.65 | | $V_{rms}$ |
| | | $R_L$ = 1200 Ω | 1.75 | | |
| | | $R_L$ = 30 kΩ | 2 | | |
| Signal/distortion | $R_L$ = 600 Ω | | 50 | | dB |

## operating characteristics, over operating free-air temperature range, $V_{CC}$ = 5 V ±5%, $V_{BB}$ = –5 V ±5%, GND at 0 V, $V_I$ = 1.2276 V, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting, in A-law and µ-law modes, (unless otherwise noted) (continued)

### power supply rejection

| PARAMETER | TEST CONDITIONS | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| Positive power-supply rejection, transmit | $V_{CC}$ = 5 V + 100 mVrms, VFXI+ = –50 dBm0 | f = 0 Hz to 4 kHz | A-law | 38 | | dB |
| | | | µ-law | 38 | | dBC† |
| | | f = 4 kHz to 50 kHz | | 40 | | dB |
| Negative power-supply rejection, transmit | $V_{BB}$ = –5 V + 100 mVrms, VFXI+ = –50 dBm0 | f = 0 Hz to 4 kHz | A-law | 35 | | dB |
| | | | µ-law | 35 | | dBC† |
| | | f = 4 kHz to 50 kHz | | 40 | | dB |
| Positive power-supply rejection, receive | PCM code equals positive zero, $V_{CC}$ = 5 V + 100 mVrms | f = 0 Hz to 4 kHz | A-law | 40 | | dB |
| | | | µ-law | 40 | | dBC† |
| | | f = 4 kHz to 50 kHz | | 40 | | dB |
| Negative power-supply rejection, receive | PCM code equals positive zero, $V_{BB}$ = –5 V + 100 mVrms | f = 0 Hz to 4 kHz | A-law | 38 | | dB |
| | | | µ-law | 38 | | dBC† |
| | | f = 4 kHz to 50 kHz | | 40 | | dB |
| Spurious out-of-band signals at the channel output (VFRO) | 0 dBm0, 300-Hz to 3400-Hz input applied to DR (measure individual image signals at VFRO) | | | | –30 | dB |
| | f = 4600 Hz to 7600 Hz | | | | –33 | dB |
| | f = 7600 Hz to 8400 Hz | | | | –40 | |
| | f = 8400 Hz to 100 kHz | | | | –40 | |

† The unit dBC applies to C-message weighting.

## operating characteristics, over operating free-air temperature range, $V_{CC}$ = 5 V ±5%, $V_{BB}$ = –5 V ±5%, GND at 0 V, $V_I$ = 1.2276 V, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting, in A-law and μ-law modes, (unless otherwise noted) (continued)

### distortion

| PARAMETER | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Signal-to-distortion ratio, transmit or receive half-channel‡ | Level = 3 dBm0 | | 33 | | dBC† |
| | Level = 0 dBm0 to -30 dBm0 | | 36 | | |
| | Level = –40 dBm0 | Transmit | 29 | | |
| | | Receive | 30 | | |
| | Level = –55 dBm0 | Transmit | 14 | | |
| | | Receive | 15 | | |
| Single-frequency distortion products, transmit | | | | –46 | dB |
| Single-frequency distortion products, receive | | | | –46 | dB |
| Intermodulation distortion | Loop-around measurement, VFXI+ = –4 dBm0 to –21 dBm0, Two frequencies in the range of 300 Hz to 3400 Hz | | | –41 | dB |
| Signal-to-distortion ratio, transmit half-channel (A-law) (CCITT G.714)§ | Level = –3 dBm0 | | 33 | | dB |
| | Level = –6 dBm0 to –27 dBm0 | | 36 | | |
| | Level = –34 dBm0 | | 33.5 | | |
| | Level = –40 dBm0 | | 28.5 | | |
| | Level = –55 dBm0 | | 13.5 | | |
| Signal-to-distortion ratio, receive half-channel (A-law) (CCITT G.714)§ | Level = –3 dBm0 | | 33 | | dB |
| | Level = –6 dBm0 to –27 dBm0 | | 36 | | |
| | Level = –34 dBm0 | | 34.2 | | |
| | Level = –40 dBm0 | | 30 | | |
| | Level = –55 dBm0 | | 15 | | |

† The unit dBC applies to C-message weighting.
‡ Sinusoidal test method (see Note 6)
§ Pseudo-noise test method
NOTE 6: μ-law measurements are made using a C-message weighted filter, and A-law measurements are made using a psophometric weighted filter.

## timing requirements over recommended ranges of operating conditions (see Figures 1 and 2)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{clock(M)}$ | Frequency of master clock | MCLK | | 2.048 | | MHz |
| $f_{clock(B)}$ | Frequency of bit clock, transmit | BCLK | 64 | | 2048 | kHz |
| $t_{w1}$ | Pulse duration, MCLK high | | 160 | | | ns |
| $t_{w2}$ | Pulse duration, MCLK low | | 160 | | | ns |
| $t_{r1}$ | Rise time of master clock (20% to 80%) | MCLK | | | 50 | ns |
| $t_{f1}$ | Fall time of master clock (80% to 20%) | MCLK | | | 50 | ns |
| $t_{r2}$ | Rise time of bit clock (20% to 80%), transmit | BCLK | | | 50 | ns |
| $t_{f2}$ | Fall time of bit clock (80% to 20%), transmit | BCLK | | | 50 | ns |
| $t_{su1}$ | Setup time, BCLK high (and FSX in long-frame sync mode) before MCLK ↓ (first bit clock after the leading edge of FSX) | | 100 | | | ns |
| $t_{w3}$ | Pulse duration, BCLK high, $V_{IH}$ = 2.2 V | | 160 | | | ns |
| $t_{w4}$ | Pulse duration, BCLK low, $V_{IL}$ = 0.6 V | | 160 | | | ns |
| $t_{h1}$ | Hold time, FSX or FSR low after BCLK low (long frame only) | | 0 | | | ns |
| $t_{h2}$ | Hold time, BCLK high after FSX or FSR ↑ (short frame only) | | 0 | | | ns |
| $t_{su2}$ | Setup time, FSX or FSR high before BCLK ↓ (long frame only) | | 80 | | | ns |
| $t_{su3}$ | Setup time, DR valid before BCLK ↓ | | 50 | | | ns |
| $t_{h3}$ | Hold time, DR valid after BCLK ↓ | | 50 | | | ns |
| $t_{su4}$ | Setup time, FSX or FSR high before BCLK ↓, short-frame sync pulse (1 or 2 bit-clock periods long) (see Note 7) | | 50 | | | ns |
| $t_{h4}$ | Hold time, FSX or FSR high after BCLK ↓, short-frame sync pulse (1 or 2 bit-clock periods long) (see Note 7) | | 100 | | | ns |
| $t_{h5}$ | Hold time, FSX or FSR high after BCLK ↓, long-frame sync pulse (from 3 to 8 bit-clock periods long) | | 100 | | | ns |
| $t_{w5}$ | Minimum pulse duration of FSX or FSR (frame sync pulse — low level), 64-kbps operating mode | | 160 | | | ns |

NOTE 7: For short-frame sync timing, FSR and FSX must go high while their respective bit clocks are high.

## switching characteristics over recommended ranges of operating conditions (see Figures 1 and 2)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d1}$ | Delay time, BCLK high to data valid at DX | Load = 150 pF plus 2 LSTTL loads† | 0 | 140 | ns |
| $t_{d2}$ | Delay time, BCLK high to $\overline{TSX}$ low | Load = 150 pF plus 2 LSTTL loads† | | 140 | ns |
| $t_{d3}$ | Delay time, BCLK (or 8 clock FSX in long frame only) low to data output (DX) disabled | | 50 | 165 | ns |
| $t_{d4}$ | Delay time, FSX or BCLK high to data valid at DX (long frame only) | $C_L$ = 0 pF to 150 pF | 20 | 165 | ns |

† Nominal input value for an LSTTL load is 18 kΩ.

## PARAMETER MEASUREMENT INFORMATION

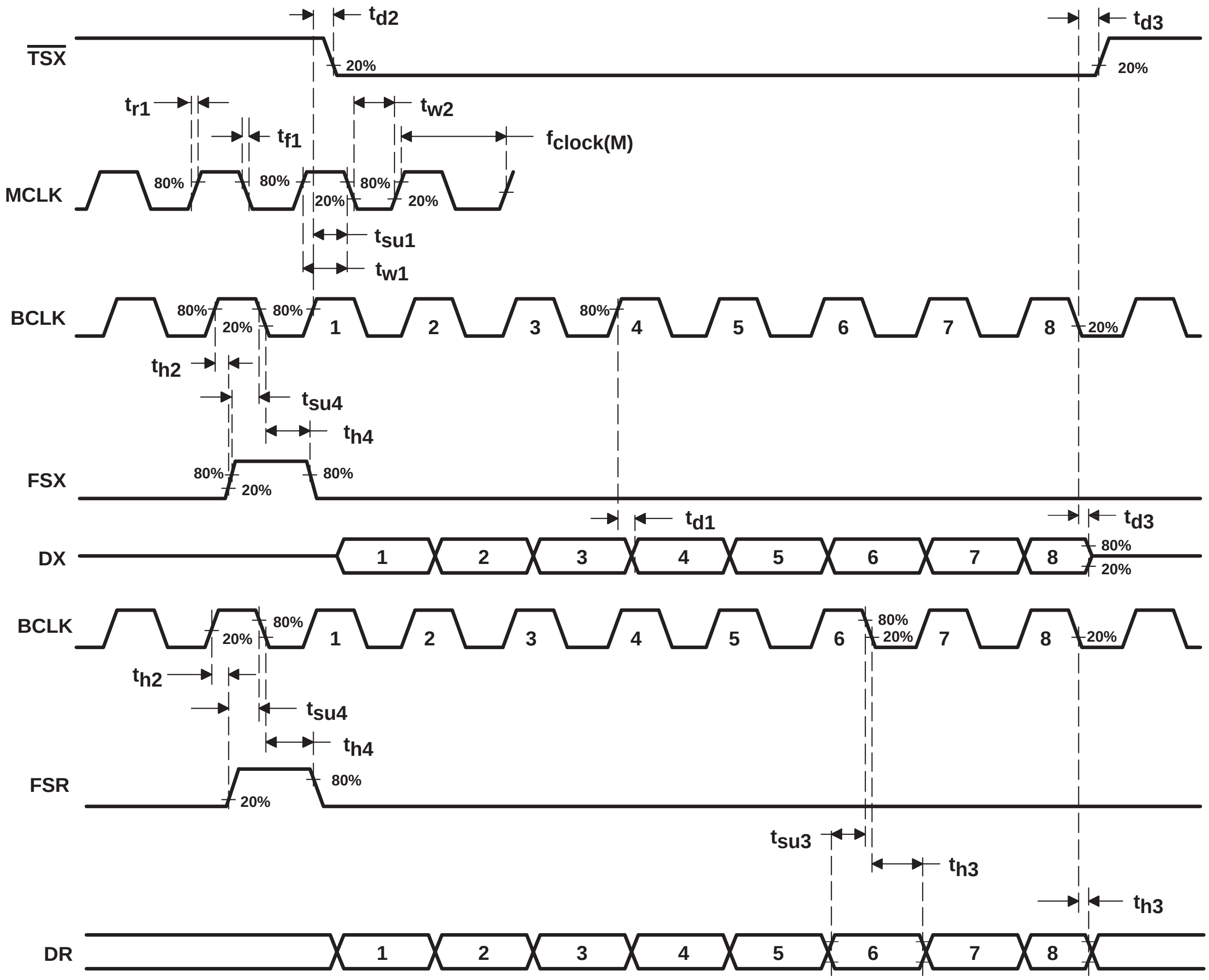



Figure 1. Short Frame Sync Timing

## PARAMETER MEASUREMENT INFORMATION

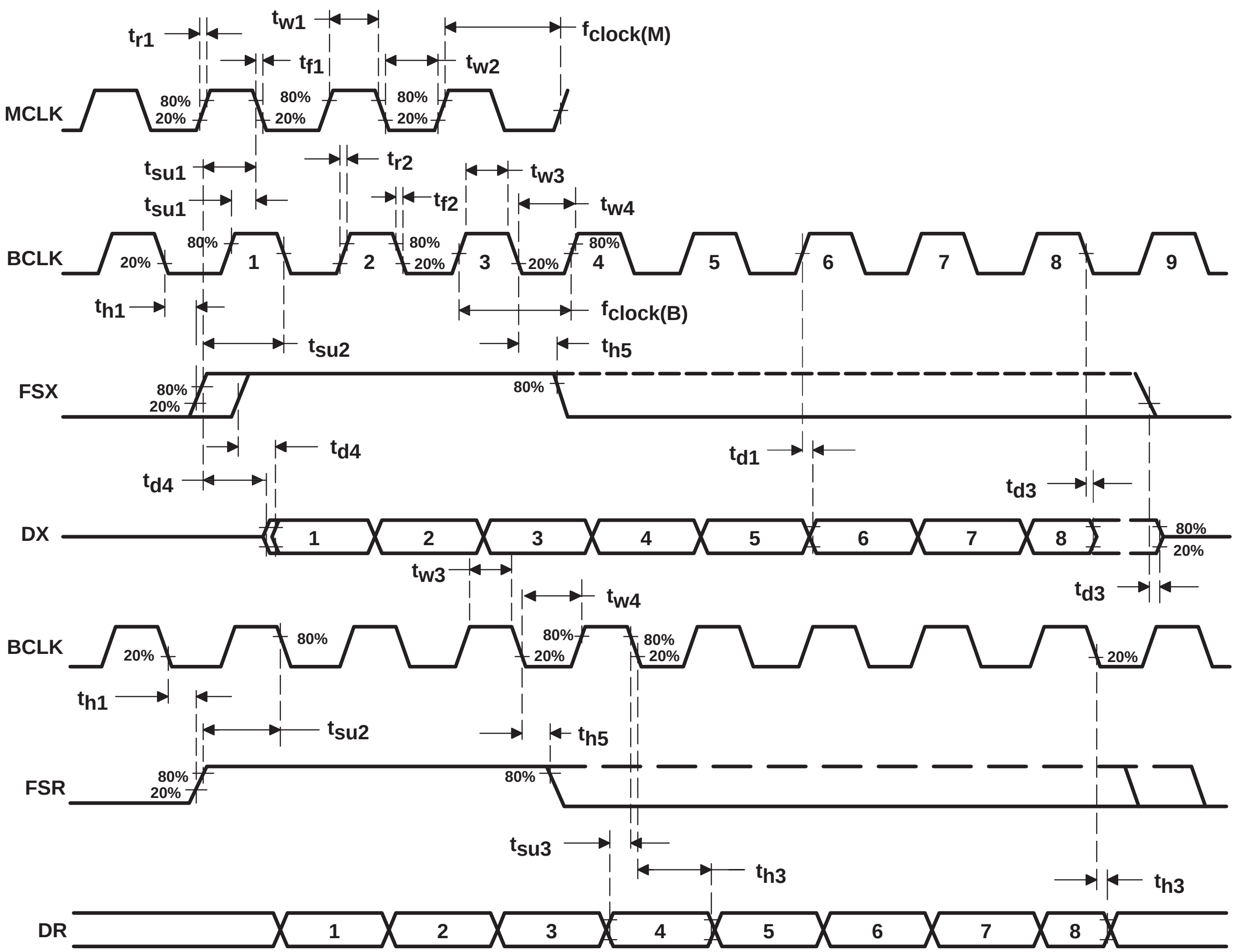



**Figure 2. Long Frame Sync Timing**

## PRINCIPLES OF OPERATION

### system reliability and design considerations

TP3056B system reliability and design considerations are described in the following paragraphs.

### latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TP3056B is heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode with a forward voltage drop of less than or equal to 0.4 V (1N5711 or equivalent) between the power supply and GND (see Figure 3). If it is possible that a TP3056B-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

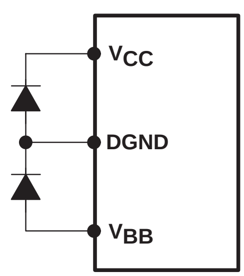



**Figure 3. Latch-Up Protection Diode Connection**

## PRINCIPLES OF OPERATION

### system reliability and design considerations (continued)

### device power-up sequence

Latch-up also can occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply $V_{BB}$ (most negative voltage).
4. Apply $V_{CC}$ (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power down condition.
8. Apply FS synchronization pulses.
9. Apply the signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

### internal sequencing

Power-on reset circuitry initializes the TP3056B device when power is first applied, placing it in the power-down mode. The DX and VFRO outputs go into the high-impedance state and all nonessential circuitry is disabled. A low level applied to the PDN terminal powers up the device and activates all internal circuits. The 3-state PCM data output, DX, remains in the high-impedance state until the arrival of the second FSX pulse.

## general operation

A 2.048-MHz clock signal applied to MCLK serves as the master clock for both the receive and the transmit directions. BCLK must have a bit clock signal applied to it, which then serves as the bit clock for both the receive and the transmit directions. BCLK can be in the range from 64 kHz to 2.048 MHz, but must be synchronous with MCLK.

The encoding cycle begins with each FSX pulse, and the PCM data from the previous cycle is shifted out of the enabled DX output on the rising edge of BCLK. After eight bit-clock periods, the 3-state DX output is returned to the high-impedance state. With an FSR pulse, PCM data is latched in via DR on the falling edge of BCLK. FSX and FSR must be synchronous with MCLK.

## PRINCIPLES OF OPERATION

### short-frame sync operation

The device can operate with either a short-frame sync pulse or a long-frame sync pulse. On power up, the device automatically goes into the short-frame mode where both FSX and FSR must be one bit-clock period long with timing relationships specified in Figure 1. With FSX high during a falling edge of BCLK, the next rising edge of BCLK enables the 3-state output buffer, outputting the sign bit at DX. The remaining seven bits are shifted out on the following seven rising edges, with the next falling edge disabling DX. With FSR high during a falling edge of BCLK, the next falling edge of BCLK latches in the sign bit. The following seven falling edges latch in the seven remaining bits.

### long-frame sync operation

Both FSX and FSR must be three or more bit-clock periods long to use the long-frame sync mode with timing relationships as shown in Figure 2. Using the transmit frame sync (FSX), the device determines whether a short- or long-frame sync pulse is being used. For 64-kHz operation, the frame-sync pulse must be kept low for a minimum of 160 ns. The rising edge of FSX or BCLK, whichever occurs later, enables the 3-state output buffer, outputting the sign bit at DX. The next seven rising edges of BCLK shift out the remaining seven bits. The falling edge of BCLK following the eighth rising edge, or FSX going low, whichever occurs later, disables DX. A rising edge on FSR, the receive-frame sync pulse, causes the PCM data at DR to be latched in on the next eight falling edges of BCLK.

### transmit section

The transmit section consists of an input amplifier, filters, and an encoding ADC. The input is an operational amplifier with provision for gain adjustment using two external resistors. The low-noise and wide-bandwidth characteristics of these devices provide gains in excess of 20 dB across the audio passband. The operational amplifier drives a unity-gain filter consisting of an RC active prefilter followed by an eighth-order switched-capacitor band-pass filter clocked at 256 kHz. The output of this filter is routed to the encoder sample-and-hold circuit. The ADC is a compressing type and converts the analog signal to PCM data in accordance with μ-law or A-law coding conventions, as selected. A precision voltage reference provides a nominal input overload voltage of 2.5 V peak.

The sampling of the filter output is controlled by the FSX frame-sync pulse; then the successive-approximation encoding cycle begins. The resulting 8-bit code is loaded into a buffer and shifted out through DX at the next FSX pulse. The total encoding delay is approximately 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign-bit integration.

### receive section

The receive section is unity gain and consists of an expanding DAC, filters, and a power amplifier. Decoding is μ-law or A-law (as selected by the ASEL terminal), and the decoded analog output signal is routed to the input of a fifth-order switched-capacitor low-pass filter. This filter is clocked at 256 kHz and corrects for the (sin x)/x attenuation caused by the 8-kHz sample/hold of the DAC. Next is a second-order RC active post-filter/power amplifier capable of driving an external 600-Ω load.

When FSR goes high, the data at DR is stepped in on the falling edge of the next eight BCLK clocks. At the end of the decoder time slot, the decoding cycle begins and 10 μs later, the decoder DAC output is updated. The decoder delay is about 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), or a total of approximately 180 μs.

## APPLICATION INFORMATION

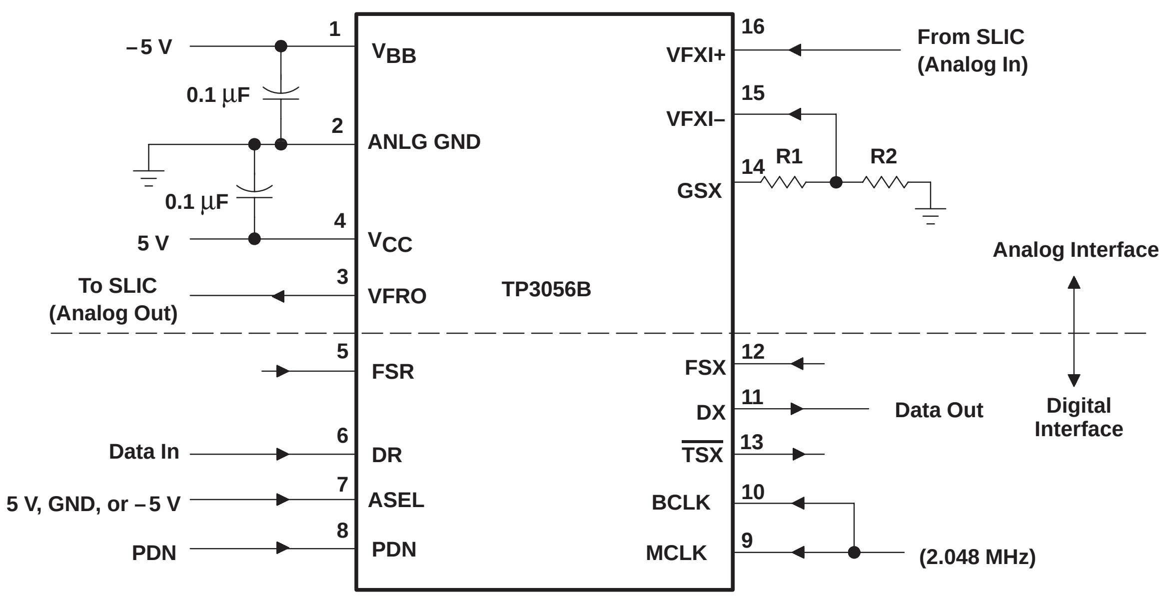
### power supplies

While the terminals of the TP3056B device is well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed-circuit board can be plugged into a hot socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the device ANLG GND terminal. This minimizes the interaction of ground return currents flowing through a common bus impedance. $V_{CC}$ and $V_{BB}$ supplies should be decoupled by connecting 0.1-µF decoupling capacitors to this common point. These bypass capacitors must be connected as close as possible to the device $V_{CC}$ and $V_{BB}$ terminals.

For best performance, the ground point of each codec/filter on a card should be connected to a common card ground in star formation rather than via a ground bus. This common ground point should be decoupled to $V_{CC}$ and $V_{BB}$ with 10-µF capacitors.

Figure 4 shows a typical TP3056B application.




NOTE A: Transmit gain = $20 \log \left(\frac{R1 + R2}{R2}\right)$, $(R1 + R2) \geq 10\ k\Omega$

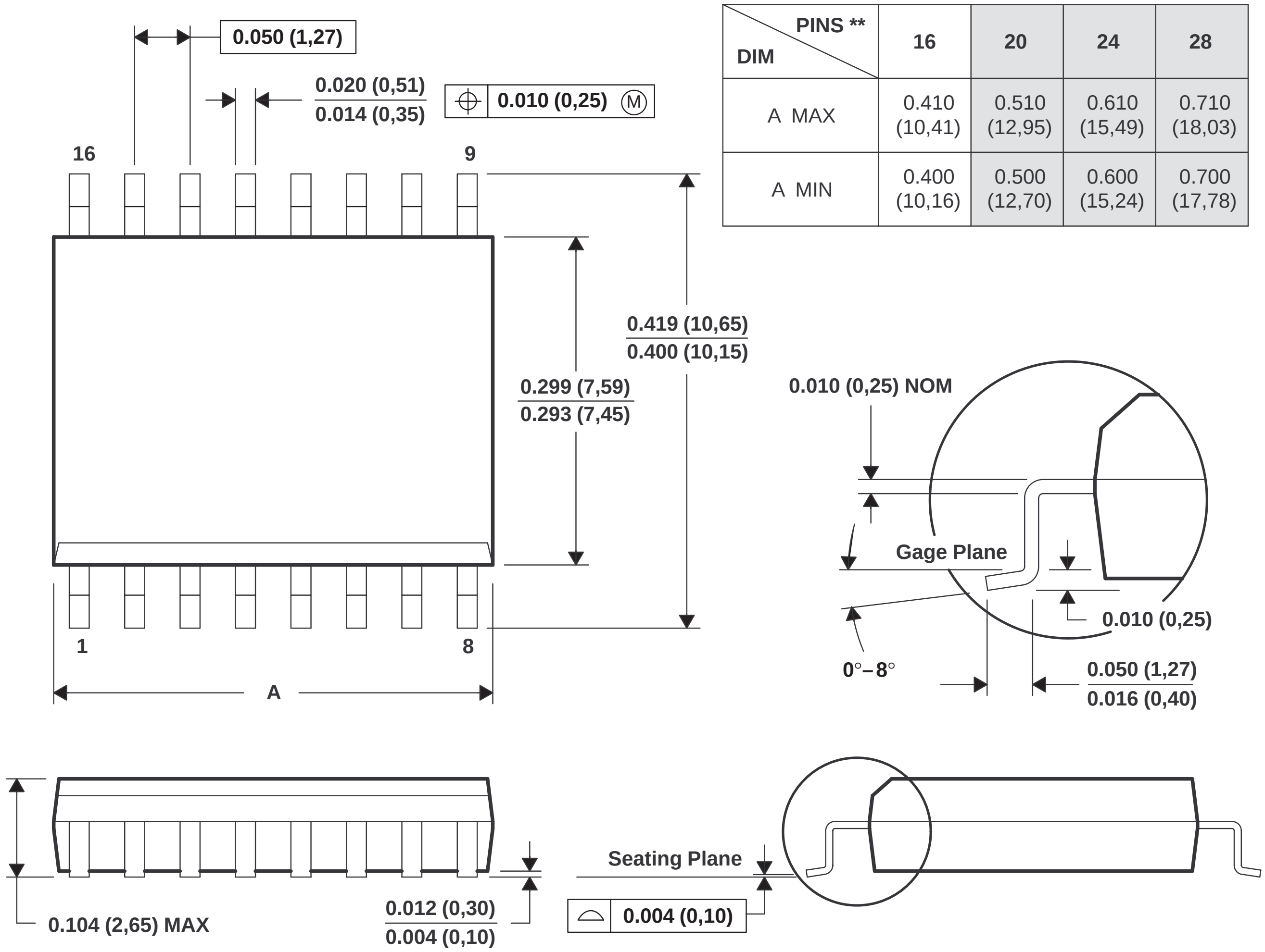
**Figure 4. Typical Synchronous Application**

## MECHANICAL DATA

**DW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**16 PIN SHOWN**

| DIM \ PINS ** | 16 | 20 | 24 | 28 |
|---|---|---|---|---|
| A MAX | 0.410 (10,41) | 0.510 (12,95) | 0.610 (15,49) | 0.710 (18,03) |
| A MIN | 0.400 (10,16) | 0.500 (12,70) | 0.600 (15,24) | 0.700 (17,78) |




4040000/B 03/95

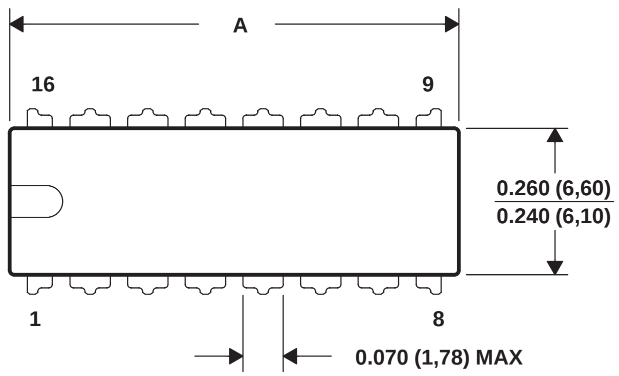
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

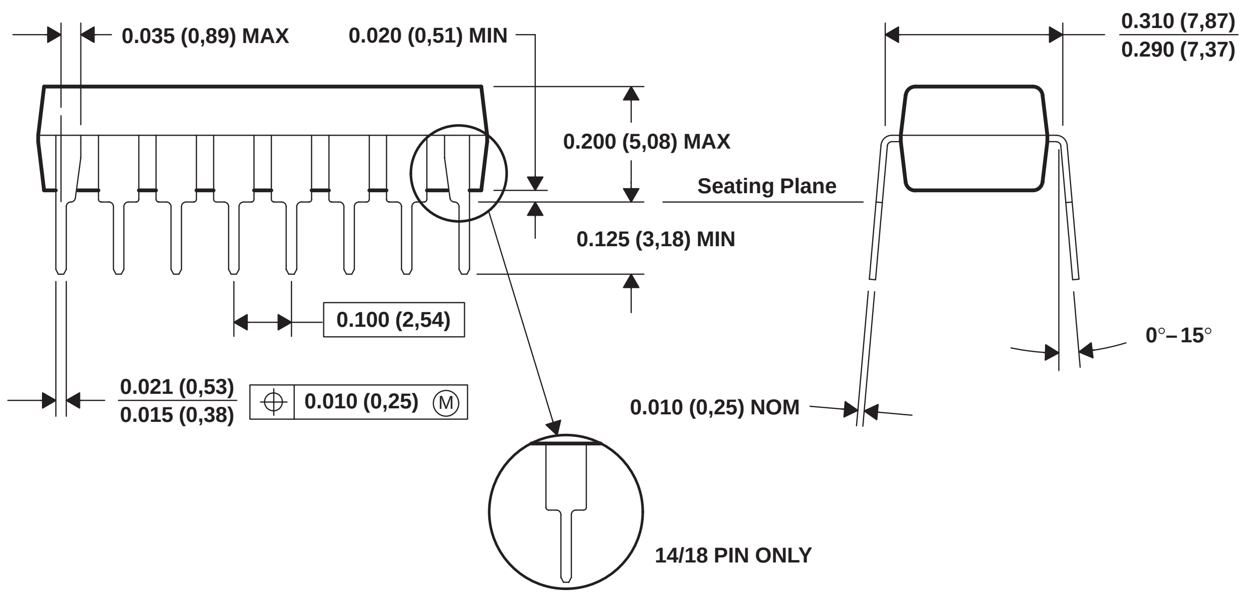
## MECHANICAL DATA

**N (R-PDIP-T**)** **PLASTIC DUAL-IN-LINE PACKAGE**

**16 PIN SHOWN**

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23.37) | 0.975 (24,77) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21.59) | 0.940 (23,88) |




4040049/C 08/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

## IMPORTANT NOTICE